SGS-THOMSON MICROELECTRONICS

STi4500
STi4510

MPEG AUDIO DECODER

ADVANCE DATA

- SINGLE-CHIP ISO/IEC 11172-3 (LAYER I & II) DECODER
- DECODES IN SINGLE CHANNEL, DUAL CHANNEL, STEREO OR JOINT STEREO MODES
- SUPPORTS ALL MPEG BIT RATES AT 32, 44.1 & 48kHz, AND FREE FORMAT AT 32 & 48kHz SAMPLING RATES
- INPUT CAN BE EITHER PACKETS OR AUDIO STREAM
- BIT OR BYTE MODE COMPRESSED DATA INPUT, WITH BURST RATE TO 20 Mbit/s
- STEREO OUTPUT LEVEL CONTROL
- 16 OR 18-BIT PCM OUTPUT, I^2S AND OTHER FORMATS
- 8-BIT MICROCONTROLLER INTERFACE
- SUPPORT FOR 1MBIT OF EXTERNAL DRAM FOR AT LEAST 1 SECOND OF SYNCHRONIZATION DELAY
- INCLUDES SYSTEM TIME CLOCK FOR HANDLING OF A/V SYNCHRONIZATION & PTS EXTRACTION FROM PACKETS
- AUTOMATIC ERROR CONCEALMENT ON CRC OR SYNCHRONIZATION ERROR DETECTION
- LOW-POWER 5V CMOS TECHNOLOGY
- PRIMARY CLOCK FREQUENCY UP TO 28MHz

APPLICATIONS

- MULTIMEDIA COMPUTER
- VIDEO CD PLAYER
- DIGITAL TV RECEIVER

DESCRIPTION

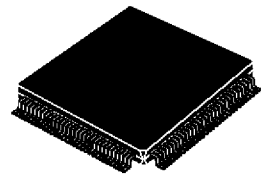
The STi4500 is a single-chip audio decompression processor compliant with layers 1 and 2 of the ISO/IEC 11172-3 (MPEG) standard. Input data is accepted at any of the MPEG-defined data rates, and PCM output is provided at 32, 44.1 or 48kHz sampling rates.

The input data may be in the form of packets or an audio elementary stream. In the former case the STi4500 extracts the audio packet data. The input rate can be either constant or in bursts up to 20 Mbit/s. Data can be input either in bytes through the microcontroller interface or through a dedicated serial port.

The PCM audio output, selectable to be either 16 bits or 18 bits, supports all popular formats including I^2S.

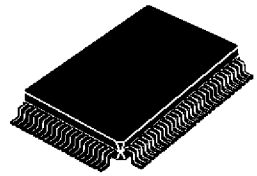
The 8-bit microcontroller interface gives access to control and status registers. A set of maskable interrupts are available for critical status and error indication.

An external 256K x 4 (or 1M x 4) DRAM can be optionally used for up to one second of data stream buffering. This is also used to enhance error concealment performance and synchronization robustness



PQFP120
(Plastic Package)

ORDER CODE : STi4500



PQFP100
(Plastic Package)

ORDER CODE : STi4510

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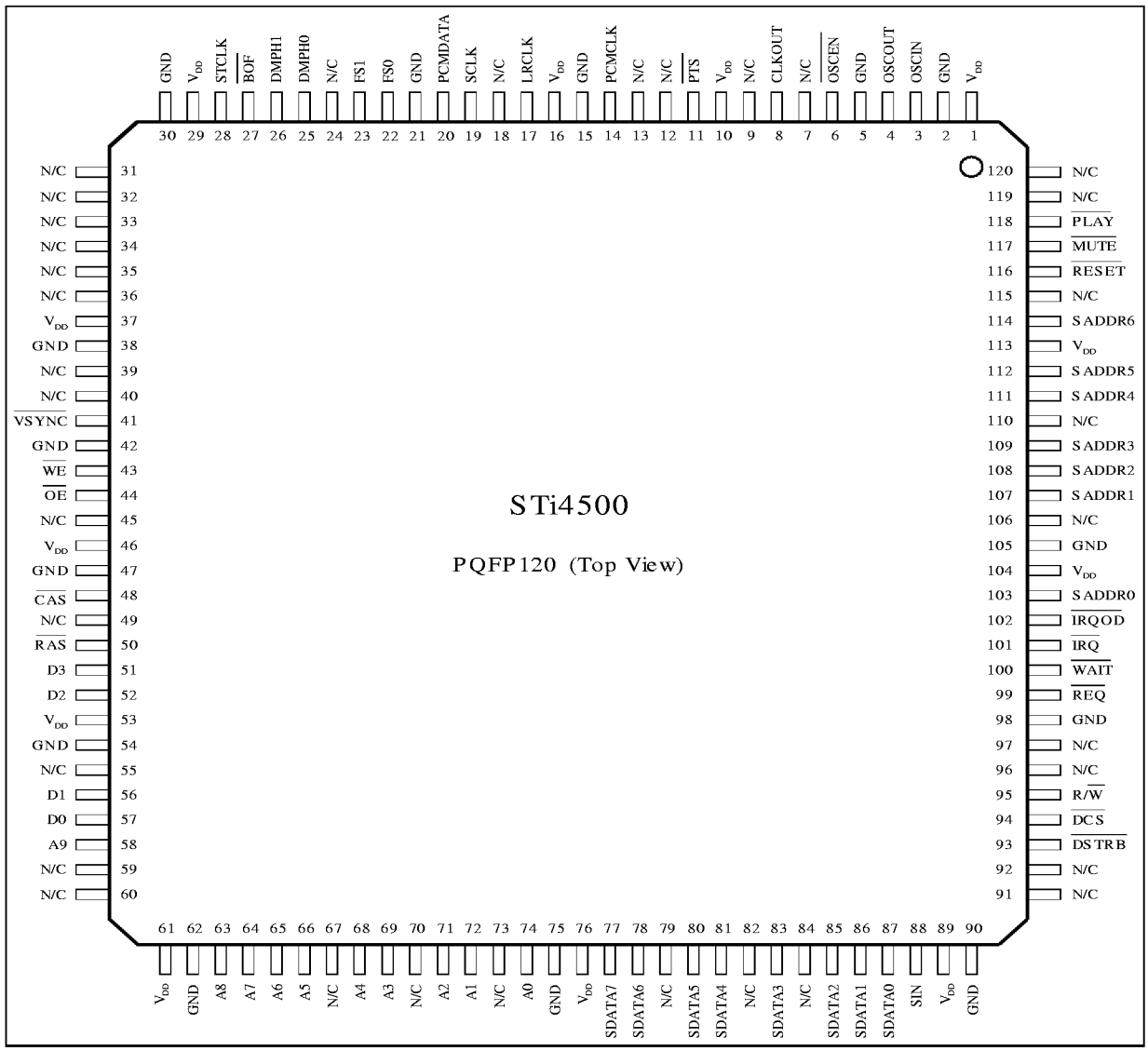
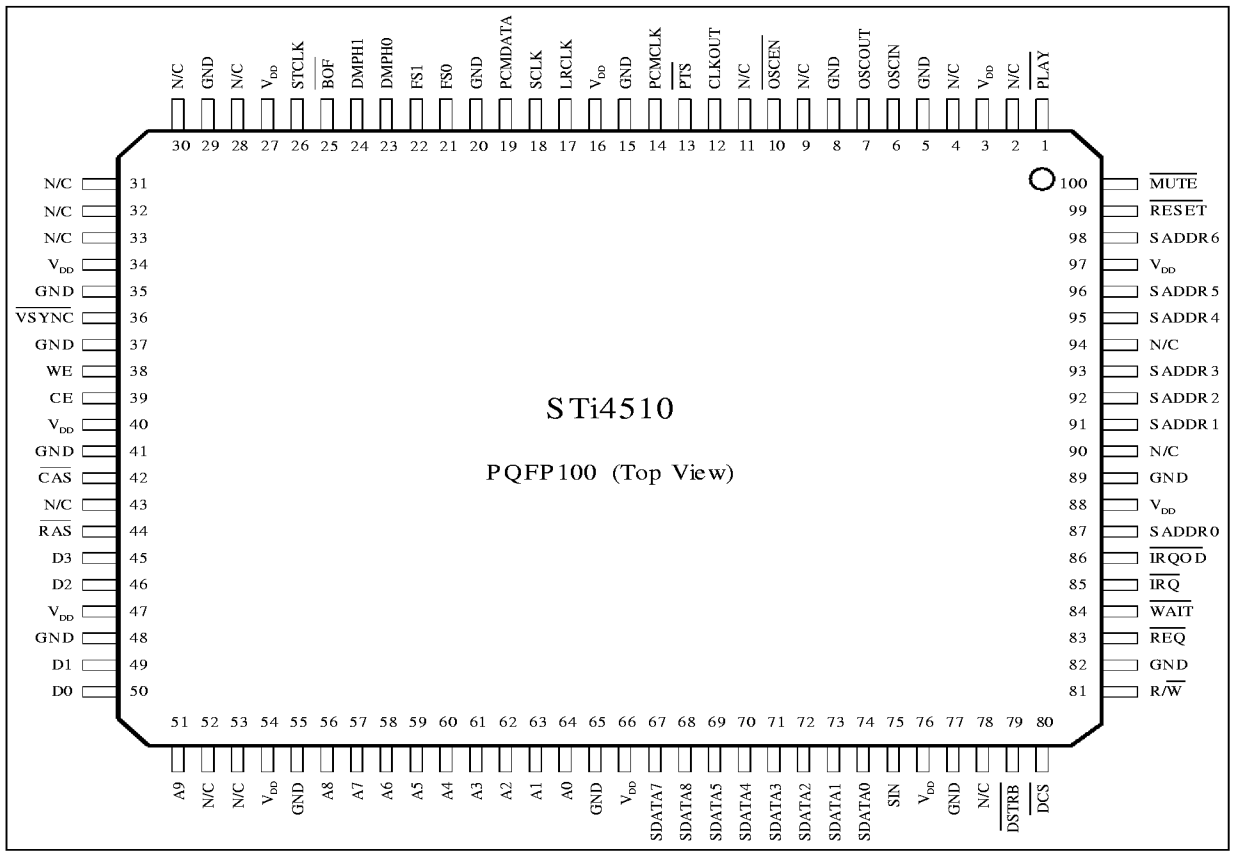
I - PIN INFORMATION

I.1 - Pin Connections (STi4500) (PQFP120)



I - PIN INFORMATION (continued)

I.1 - Pin Connections (STi4510) (PQFP100)



4510-01.EPS

I.2 - Pin Description

STi4500	STi4510	Name	Type	Function
SYSTEM SERVICES AND NON-FUNCTIONAL PINS				
1,10,16,29,37,46,53, 61,76,89,104,113	3,12,16,27,34,40, 47,54,66,76,88,97	V_{DD}		Power Supply
2,5,15,21,30,38,47, 54,62,75,90,98,105	5,8,15,20,29,35,41, 48,55,65,77,82,89	GND		Ground
3	6	OSCIN	I	24MHz clock input or crystal connection
4	7	OSCOUT		Crystal connection
8	11	CLKOUT	O	Buffered 24MHz clock output
6	9	$\overline{OSCEN}$	In	Buffered clock output enable
116	99	$\overline{RESET}$	I	Master Reset
7,9,12,13,18,24,31-36,39,40,45, 49,55,59,60,67,70,73,79,82,84, 91,92,96,97,106,110,115,119,120	2,4,10,28,30,31, 32,33,43,52,53, 78,90,94		N/C	Reserved pins, leave unconnected, or connect to ground
42	-		GND	Reserved pin, connect to ground

4500-01.TBL

I - PIN INFORMATION (continued)

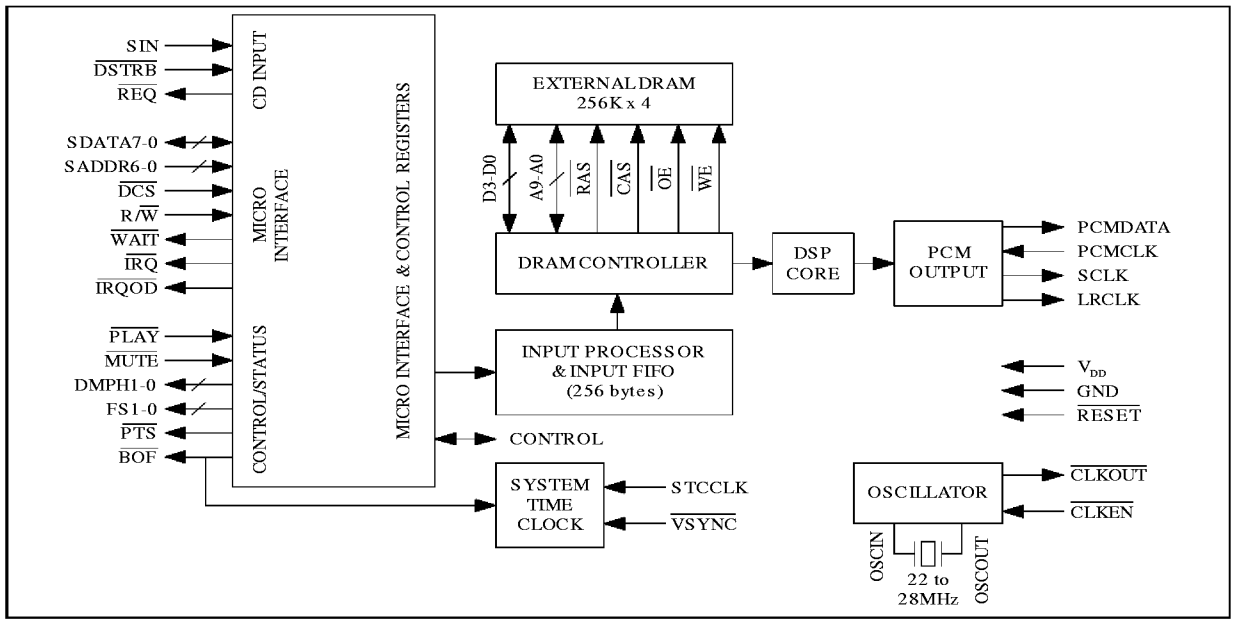
I.2 - Pin Description (continued)

STi4500	STi4510	Name	Type	Function
DRAM INTERFACE				
51,52,56,57	45,46,49,50	D3 - D0	I/O	Bidirectional data port
58,63-66,68, 69,71,72,74	51,56-64	A9 - A0	O	Address
50	44	$\overline{RAS}$	O	Row address strobe
48	42	$\overline{CAS}$	O	Column address strobe
44	39	$\overline{OE}$	O	Output enable
43	38	$\overline{WE}$	O	Write enable
SYSTEM TIME CLOCK CONTROL				
28	26	STCLK	I	System clock
41	36	$\overline{VSYNC}$	I	Video vertical synchronization signal
PCM OUTPUT INTERFACE				
20	19	PCMDATA	O	PCM serial data output
14	14	PCMCLK	I	PCM clock input
19	18	SCLK	O	PCM clock output
17	17	LRCLK	O	Left/right channel select output
MICROCONTROLLER INTERFACE				
77,78,80,81, 83,85-87	67-74	SDATA7 - SDATA0	I/O	Bidirectional data bus
114,112,111, 109-107,103	98,96,95, 93-91,87	SADDR6 - SADDR0	I	Address
94	80	$\overline{DCS}$	I	Chip select
95	81	R/$\overline{W}$	I	Read/write selection
100	84	$\overline{WAIT}$	O (3-state)	Data acknowledge
101	85	$\overline{IRQ}$	O	Interrupt request
102	86	$\overline{IRQOD}$	O (open-drain)	Interrupt request, open drain output
COMPRESSED DATA INPUT				
88	75	SIN	I	Serial compressed data input
93	79	$\overline{DSTRB}$	I	Compressed data input strobe
99	83	$\overline{REQ}$	O	Compressed data request
DECODING CONTROL AND STATUS				
118	1	$\overline{PLAY}$	I	Enable output of decoded audio
117	100	$\overline{MUTE}$	I	Forced muted audio output
26,25	24,23	DMPH1, DMPH0	O	De-emphasis mode of current frame
23,22	22,21	FS1,FS0	O	Sampling frequency of current frame
27	25	$\overline{BOF}$	O	Beginning of frame at PCM output
11	13	$\overline{PTS}$	O	Frame at PCM output has associated PTS

4500-02.TBL

II - BLOCK DIAGRAM

Figure 1



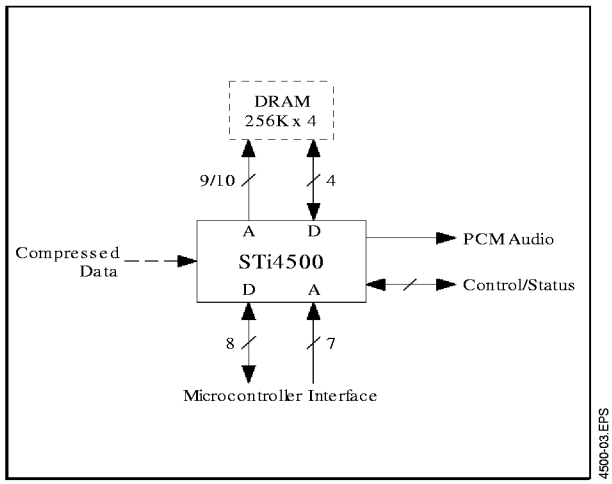
III - FUNCTIONAL DESCRIPTION

III.1 - STi4500/STi4510 Architecture

The STi4500/STi4510 has 5 principal blocks:
- host interface and control registers
- input processor
- DRAM controller
- DSP core
- PCM output

The interconnection of these blocks, and all external interfaces, are shown in Figure 1.

Figure 2



Host Interface and Control Register

The block implements the 8-bit interface to the host processor. All control registers are accessible through this block.

Input Processor

The block is responsible for the parsing of the bitstream at the packet level, implementation of the synchronizing algorithms, decoding of time stamps, and the tagging of the audio bitstream with the appropriate PTS before storage in the DRAM. There is an internal 256-byte FIFO buffer.

DRAM Controller

This block has the functions of testing for the presence of DRAM and generating of all necessary DRAM control signals.

DSP Core

This block performs bitstream decoding and synthesis subband filter execution, according to layers I and II of the MPEG algorithm.

PCM Output

This block organises the PCM audio output into the required serial format, and generates all of the D-A converter control signals. In addition, a system time clock counter is provided, which is not directly connected to any of the above blocks. This function is required when managing synchronization in an audio/video decoding system.

III - FUNCTIONAL DESCRIPTION (continued)

III.2 - Input Formats Accepted

The STi4500/4510 is able to accept the following 3 types of bitstream :
- MPEG audio elementary stream, as defined by ISO/IEC 11172-3, Layers I and II
- ISO/IEC 11172-1 packets with syntax as shown below

```
                                        no. of bits
packet()  {
        packet_start_code_prefix              24
        stream_id                              8
        packet_length                         16
        if(stream_id != private_stream_2) {
          while (nextbits() == '1111 1111')
            stuffing_byte                      8
          if (nextbits() == ' 01') {
              '01'                             2
              STD_buffer_scale                 1
              STD_buffer_size                 13
          }

          if (nextbits() == '0010') {
              '0010'                           4
            presentation_time_stamp[32..30]    3
            marker_bit                         1
            presentation_time_stamp[29..15]   15
            marker_bit                         1
            presentation_time_stamp[14..0]    15
            marker_bit                         1
          }

          else if (nextbits() == '0011') {
            '0011'                             4
            presentation_time_stamp[32..30]    3
            marker_bit                         1
            presentation_time_stamp[29..15]   15
            marker_bit                         1
            presentation_time_stamp[14..0]    15
            marker_bit                         1
            '0001'                             4
            decoding_time_stamp[32..30]        3
            marker_bit                         1
            decoding_time_stamp[29..15]       15
            marker_bit                         1
            decoding_time_stamp[14..0]        15
            marker_bit                         1
          }
          else
            '0000 1111'                        8
          }
          for (i=0; i  N; i++) {
            packet_data_byte                   8
}
}
```

The outlined parts indicate the information which is extracted by the STi4500/4510. The other items of packet body information are ignored.
- uncompressed PCM data (for bypass mode)

III - FUNCTIONAL DESCRIPTION (continued)

III.3 - System Time Clock

This function is included to assist the implementation of audio/video synchronization in decoding systems.

The system time clock (STC) counter is incremented by a '90 kHz' programmable sub-multiple of the input STCCLK, which could be, for example be fed from the same clock as PCMCLK. The value of STC can be latched by both BOF (internal signal indicating beginning of audio frame), and VSYNC (externally provided video picture synchronization signal), and read by the host controller.

III.4 - Documentation Conventions

In this data sheet, the following conventions are used when documenting the functions of signals :

I/O signals can either be **active high** or **active low**. The former have names without an overbar (i.e. SIGNAL) , the latter have an overbar (i.e. $\overline{\text{SIGNAL}}$). Where a signal has two different and mutually exclusive actions, a dual name is used (e.g. COME/GO).

Internal signals and variable names (e.g. bits in registers) are always documented as active high.

When the condition indicated by the name of the signal or variable is **true**, the signal or variable is said to be true, **asserted** or to have the value 1.

When the condition indicated by the name of the signal or variable is not true, the signal or variable is said to be **false**, **de-asserted** or to have the value 0.

When an active high signal is true or asserted, the logic voltage level is high.

When an active low signal is true or asserted, the logic voltage level is low.

When an internal signal or variable is **set**, it has the value 1. A bit is never "set to 0", but "reset to 0".

When an internal signal or variable is **reset**, it has the value 0.

Hexadecimal numbers are indicated by appending an "h", e.g. A70h.

III.5 - Summary Specification

Bitstreams accepted
ISO/IEC 11172-3 audio elementary stream
ISO/IEC 11172-1 packets
Audio PCM data (for decoder bypass)

Performance
ISO/IEC 11172-3 Layers I & II
All MPEG input bitrates supported with sampling rates of 32, 44.1 and 48kHz, free format at 32 & 48kHz sampling rates
Decodes in single channel, dual channel, stereo, or joint stereo modes

System Clock
24MHz nominal

Microcontroller Interface
8-bit interface with "wait" signal handshake. Interrupt request signal. Dedicated control inputs for "play" and "mute".

Compressed Data Input
Bit or byte-mode input
Burst rate up to 20 Mbit/s

External DRAM
External 1Mbit DRAM option for audio delay and error concealment by frame repeat
Standard interface for 256K X 4 or 1M X 4 DRAM

PCM Output
16 or 18-pit PCM output
I^2S and other popular formats supported

System Time Clock and Support for A/V Sync
Host-accessible counter included for handling of audio/video synchronization. Sampled on start of audio frame or video picture output.
PTS extraction from MPEG packet layer.

Error Concealment
Automatic error concealment on CRC or synchronization error detection

Package
120-pin PQFP or 100-pin PQFP

Power Consumption
425mW typical

IV - MICROCONTROLLER INTERFACE AND COMPRESSED DATA INPUT

IV.1 - Interface Signals

The combined microcontroller/compressed data interface consists of the following signals :

- SDATA7 - SDATA0 : I/O data port
- SADDR6-SADDR0 : I address
- R/$\overline{W}$: I read/write selection
- $\overline{DCS}$: I register read/write strobe
- $\overline{WAIT}$: O acknowledge
- SIN : I serial CD input
- $\overline{DSTRB}$: I CD write strobe
- $\overline{REQ}$: O CD data request
- $\overline{IRQ}$, $\overline{IRQOD}$: O Interrupt request

Input of compressed data in byte mode and read/write access to ST4500/4510 control registers share the same 8-bit data port, SDATA7-SDATA0. The signal $\overline{DCS}$ requests a register access cycle, while the signal $\overline{DSTRB}$ requests a compressed data write cycle. R/$\overline{W}$ selects the direction of transfer for a register access. Register addresses are selected by the 7 address bits SADDR6-SADDR0.

If compressed data is input in byte mode, the multiplexing of compressed data and control bytes on to SDATA7-SDATA0, as well as arbitration of compressed data and register read/write cycles, must be performed externally.

Compressed data can also be input in serial mode through the dedicated port SIN.

$\overline{WAIT}$ (a 3-state output) is the acknowledge for register access cycles triggered by $\overline{DCS}$. $\overline{REQ}$ indicates that the STi4500/4510 is available for the input of compressed data, and together with $\overline{DSTRB}$, makes a DMA handshake.

Interrupt requests are signalled by $\overline{IRQ}$. An alternative open-drain interrupt request, $\overline{IRQOD}$, is also provided.

IV.2 - Register Access

The address bits, SADDR6-SADDR0, select one of the 128 one-byte control register locations. The function of each register is detailed in section 8.0, "REGISTER DESCRIPTIONS". Some are read/write, some read-only, and some write-only. The signal R/$\overline{W}$ defines whether the register access is a read or a write (high for read, low for write).

A cycle is defined by the assertion of signal $\overline{DCS}$. In response to this the signal $\overline{WAIT}$ is always asserted. The address, read/write and data inputs must be set up before $\overline{DCS}$ line is activated.

If a read cycle is requested, the data lines SDATA7-SDATA0 will be driven by the STi4500/4510. For a write cycle the STi4500/4510 will latch the data placed on the data lines on the rising edge of $\overline{DCS}$.

When WAIT is de-asserted, indicating the completion of the read or write operation, $\overline{DCS}$ can return to its high state and the cycle ends. The timing of register read/write cycles is given in Figure 16 and Figure 16 of section 9.3.3, "Microcontroller Interface Timing" . The minimum time between two successive read or write cycles is 100 ns. The signal $\overline{WAIT}$ is in its high state when a read/write cycle is not in progress (i.e. while $\overline{DCS}$ is high).

During a register read/write cycle (i.e. while $\overline{DCS}$ is low), the compressed data input strobe $\overline{DSTRB}$ must be high if :

1. The STi4500/4510 is configured for byte-mode compressed data input (i.e register SIN_EN = 0),
2. The STi4500/4510 is configured for serial compressed data input (i.e. register SIN_EN = 1), and register DATAIN is being accessed.

The relative timing constraints of these two signals are given in Figure 18 of section XI.3.3, "Microcontroller Interface Timing" .

IV - MICROCONTROLLER INTERFACE AND COMPRESSED DATA INPUT (continued)

IV.3 - Interrupts

The conditions that can cause an interrupt are listed in the table below :

No	Condition Signalled
14	First bit of new frame at PCM output
13	Input FIFO full
12	Input FIFO level = FIFO_THRES
11	External DRAM full
10	De-emphasis changed
9	Sampling frequency changed
8	PCM output buffer underflow
7	Ancillary data register full
6	not used
5	CRC error detected
4	Blocks in DRAM ≥ BALF_LIM
3	Blocks in DRAM ≤ BALE_LIM
2	Valid PTS registered
1	Valid header registered
0	Change in synchronization status

An interrupt is enabled by setting the corresponding bit in the interrupt mask register, INTR_EN. An interrupt is signalled externally by a 100 ns pulse appearing on IRQ. At the same time one of the bits of the interrupt register, INTR, becomes set. The interrupt source may then be identified by reading INTR.

The most significant byte (bits 8-14), and bits 3-5 of the least significant byte of INTR can be independently cleared by reading. Bits 0-2 and 7 are cleared by a different method, as explained in the description of the INTR register in section X, "REGISTER DESCRIPTIONS" . If the condition giving rise to the interrupt remains, a new interrupt will be generated.

The INTR and INTR_EN registers are cleared on reset (assertion of RESET pin or writing to the RESET register), or restart (writing to the RESTART register).

IV.4 - Compressed Data Input

The following 3 types of bitstream may be input :

1. MPEG audio elementary stream, as defined by ISO/IEC 11172-3, Layers I and II.
2. ISO/IEC 11172-1 packets.
3. uncompressed PCM data.

The input mode is determined by the programming of register STR_SEL (see section X, "REGISTER DESCRIPTIONS").

There are three possible ways of inputting compressed data, shown in the table below :

	Serial Input (SIN_EN = 1)	Parallel Input (SIN_EN = 0)
Strobed by $\overline{\text{DSTRB}}$	DMA mode	DMA mode
Strobed by $\overline{\text{DCS}}$		Write to DATAIN

The compressed bit stream can be input in parallel or serial mode depending on the value of SIN_EN register.

If serial mode is selected, data is placed on pin SIN, and strobed in on the rising edge of signal $\overline{\text{DSTRB}}$. If the signal $\overline{\text{REQ}}$ is asserted (low), then another data bit can be input. $\overline{\text{REQ}}$ goes high when the input buffer is full. Two further bits can safely be entered after this. Serial input timing is given in Figure 20 of section XI.3.4, "Compressed Data Input" .

If parallel mode is selected, data can be input using $\overline{\text{DSTRB}}$ as described above, or by writing to the DATAIN register using $\overline{\text{DCS}}$. If the signal $\overline{\text{REQ}}$ is asserted (low), then another data byte can be input. $\overline{\text{REQ}}$ goes high when the input buffer is full. ONE further byte can safely be entered after this. Parallel input timing is given in Figure 20 of section XI.3.4, "Compressed Data Input" and Figure 16 of section XI.3.3, "Microcontroller Interface Timing" .

The signal $\overline{\text{REQ}}$ is high for the duration of the reset and restart processes (see section VIII.2, "Initialization of the Decoder" and section VIII.3, "Play and Mute").

The relative timing constraints between $\overline{\text{DCS}}$ and $\overline{\text{DSTRB}}$ specified in section IV.2, "Register Access", must be respected.

Data may be input in bursts at rates of up to 20 Mbit/s in serial mode, or 2.5 Mbyte/s in parallel mode.

IV.5 - Input Buffer Level Control

The input buffering is shown in Figure 2. Input data is entered into a 256-byte FIFO store before interpretation by the parser. If external DRAM is installed, and low latency mode (LATENCY = 0) or bypass mode (STR_SEL = 11_2) are not enabled, audio frames are stored in an additional 128 Kbyte buffer before being sent to the decoder. The format of data storage in the DRAM buffer is given in section VI.3, "Frame Data Storage Structure and Delay".

5 interrupts are available for the monitoring of buffer levels, two relating to the input FIFO, and three relating to the DRAM buffer.

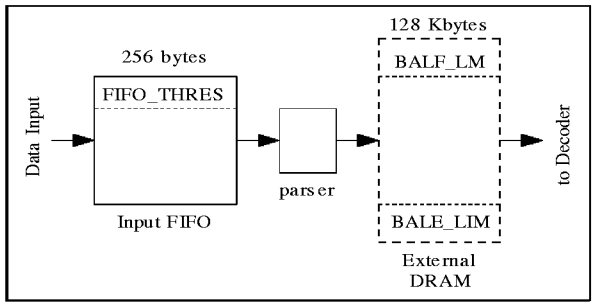
IV - MICROCONTROLLER INTERFACE AND COMPRESSED DATA INPUT (continued)

Interrupt 13 indicates that the input FIFO is full, while interrupt 12 indicates that the input FIFO level is equal to the value loaded into register FIFO_THRES. Interrupt 12 is generated whenever the level crosses the threshold. It is recommended to use $\overline{REQ}$ to control input data flow whenever possible.

The level of data in the DRAM buffer can be read from register BUFF_LEVEL. Two thresholds can be set: an upper level in BALF_LIM, and a lower one in BALE_LIM. When the level is greater than BALF_LIM, interrupt 4 is generated, when it is lower than BALE_LIM, interrupt 3 is generated. When the DRAM buffer is full, interrupt 11 is generated.

All buffers are flushed after a reset or restart.

Figure 3 : Input Buffer Organization



IV.6 - Latency

Before being able to output samples, the STi4500/4510 must first be synchronized to the bitstream. After this the decoder requires a certain amount of data, equal to roughly 1/12 of a frame, before the output samples can be computed. The time required to compute these samples is about 2ms.

The total delay is equal to the sum of the synchronization time, the time required to input the data, and the decoding time. The synchronization time is time required to skip zero, one, two or three frames (see section VIII.5, "Bitstream Synchronization"). This depends on the Layer and sampling frequency, and has a maximum value of 3 x 36 = 108ms (frame Duration for Layer II at 32kHz). Similarly, the longest data input time is 36/12 = 3ms. Once the STi4500/4510 is synchronized, the longest latency in low latency mode is 3 + 2 = 5ms.

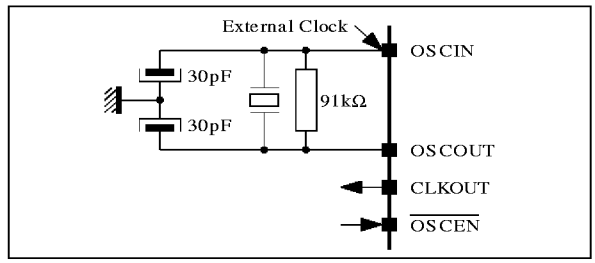
V - CLOCKS

V.1 - Primary Clock

The STi4500/4510 primary clock, which has a nominal value of 24MHz, can either be independently generated or derived from another system clock. It can either be input directly on Pin OSCIN, or generated from a crystal using the circuit shown in Figure 4.

The crystal should be a fundamental-mode, parallel-resonant, 15pF device. The values of the capacitors shown should be in the range of 10 to 30pF.

Figure 4 : Primary Clock Circuit



V.2 - PCM Clock

The input PCMCLK is used to generate the PCM output bit clock. Programming of the internal clock divider is described in section VII.2, "PCM Clock Generation" .

V.3 - System Time Clock

The input STCLK is used to generated the system time clock, which is used to increment the system time clock counter. Programming of the internal clock divider is described in section IX, "SYSTEM TIME COUNTER" .

VI - EXTERNAL DRAM

VI.1 - General

The utilisation of an external 1 Mbit DRAM provides the following capabilities :

- At least one second of audio may be buffered for the purposes of audio/video synchronization
- Error concealment by frame repeat
- Skip and repeat of audio frames
- Synchronization look-ahead

The STi4500/4510 is designed to interface with a (120ns maximum) 256K x 4 DRAM. It is also designed to support a 1M x 4 DRAM in the event that the 1M x 4 DRAM becomes less expensive than the 256K x 4. When a 1M x 4 DRAM is used, only 256K x 4 of the1M x 4 is utilised.

VI - EXTERNAL DRAM (continued)

VI.2 - Interface

The memory interface contains the following signals :

- D3 - D0 bidirectional data port
- A9 - A0 address
- RAS row address strobe
- CAS column address strobe
- OE output enable
- WE write enable

Memory timing diagrams are shown in section XI.3.2, "DRAM Interface" .

The STi4500/4510 provides a 655µs power-on pause followed by 16 initialization cycles.

At power-up, the bit DRAM_EXT is set automatically to indicate whether an external DRAM is connected.

VI.3 - Frame Data Storage Structure and Delay

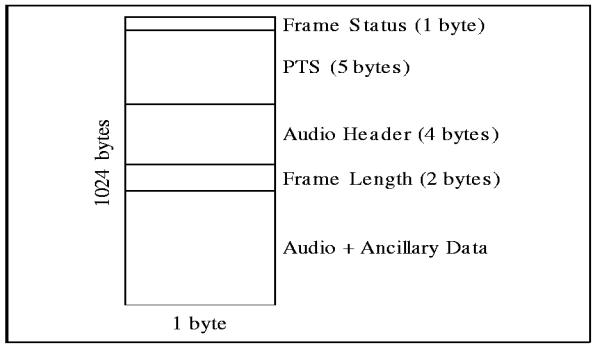
Frame data is stored in the external DRAM in units of blocks, each containing 1024 bytes. The maximum number of blocks which can be stored in the 1 Mbit memory is 128.

A Layer I audio frame is always stored in one block. A Layer II audio frame is always stored in two blocks.

The organisation of data within a block is shown in Figure 5.

The first byte is a status word indicating whether or not the frame is valid. After this, a second byte indicates whether the following PTS code is valid. The PTS value is stored in 5 bytes. After the PTS, the 4-byte audio frame header is stored. Following the header is the frame length (2 bytes). Finally the compressed audio data, plus any ancillary data, is stored.

Figure 5 : DRAM Block Format



The amount of audio delay possible in 128 blocks depends on the layer and sampling rate.

For layer I : delay = (384 X 128) / sampling rate
For Layer II : delay = (1152 X 64) / sampling rate

The table below gives the values possible.

	Sampling Frequency		
	32kHz	44.1kHz	48kHz
Layer I	1.536 s	1.115 s	1.024 s
Layer II	2.304 s	1.672 s	1.536 s

VII - PCM OUTPUT

VII.1 - Interface and Output Formats

The decoded audio data is output in serial PCM format. The interface consists of the following signals :

- PCMDATA PCM serial data output
- SCLK PCM clock output
- LRCLK Left/right channel select output
- PCMCLK PCM clock input

Output precision is selectable to be either 16 bits/word or 18 bits/word by setting the output precision select, PCM_18, register.

In 16-bit mode, data may be output either with the most significant bit first or least significant bit first as selected by the contents of the output order select, PCM_ORD, register.

When 18-bit data is selected, 32 bits are output for each channel. The data in front register, PCM_DIF, is used to position the 18 data bits either at the beginning or at the end of each 32-bit frame. The PCM_FORMAT register is used to select standard or I^2S-compatible format when 18-bit precision is selected.

Figure 6 shows the five different output formats which are possible. PCM_ORD only has significance in 16-bit mode. PCM_DIF only has significance in 18-bit mode. PCM_FORMAT only has significance in 18-bit mode and when PCM_DIF = 1. The last option shown in Figure 6 is compatible with the I^2S format.

The polarity of the PCM serial output clock, SCLK, and the left/right channel selection, LRCLK, are selected by bits INV_SCLK and INV_LRCLK, respectively.

Figure 7 shows the two polarities of SCLK. Normally, the DAC will sample LRCLK and PCMDATA on the rising edge of SCLK in the first case, and on the falling edge of SCLK in the second. The first option (INV_SCLK = 0) is the one normally used in I^2S systems.

Figure 8 shows how the polarity of LRCLK is selected. The second option (INV_LRCLK = 1) is compatible with the I^2S format.

PCM interface timing is given in Figure 20 of section XI.3.4, "Compressed Data Input" .

VII - PCM OUTPUT (continued)

Figure 6 : PCM Output Formats

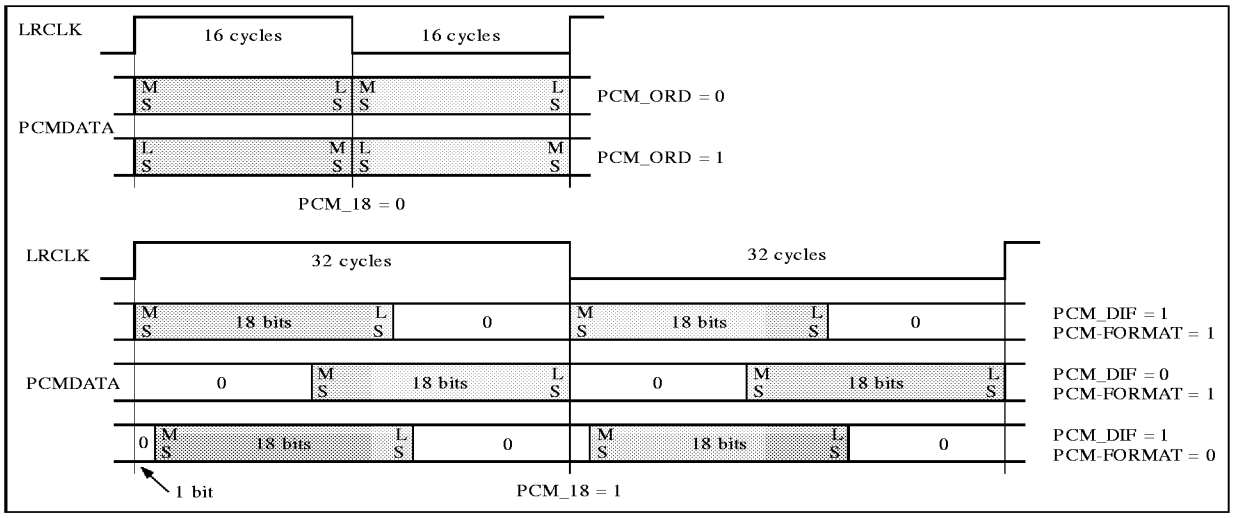


Figure 7 : SCLK Polarity

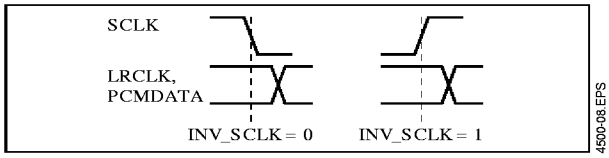
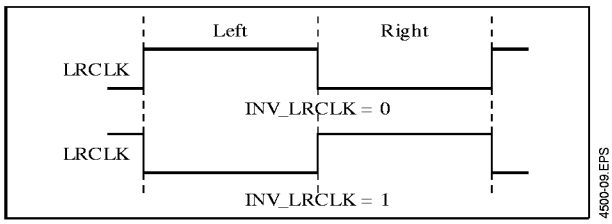


Figure 8 : LRCLK Polarity



VII.2 - PCM Clock Generation

The PCM serial clock SCLK is derived from the clock input PCMCLK. The frequency of PCMCLK may be equal to the PCM output bit rate, or it may be an integer multiple of this, allowing the use of oversampling D-A converters. In many applications PCMCLK is externally synchronized to the compressed audio bit stream.

SCLK is derived from PCMCLK by dividing it by the contents of the divider register, PCM_DIV.This number, in the range 0 to 63, defines the ratio of the frequency of the PCM bit clock, SCLK, to that of PCMCLK, according to the relationship :

$$f_{SCLK} = \frac{f_{PCMCLK}}{2 \cdot (PCM\_DIV + 1)}$$

For example, PCM_DIV is loaded with 0, the frequency of SCLK is one half of the frequency of PCMCLK, while if PCM_DIV is loaded with 63, the frequency of SCLK is one 128th of the frequency of PCMCLK. The value of PCM_DIV = 16 is reserved. If this number is loaded, the divider is bypassed and the frequency of SCLK is equal to the frequency of PCMCLK. PCM_DIV must be set up before the output of SCLK starts. This can be done by first disabling PCM outputs by de-asserting the MUTE and PLAY commands, and then writing to the PCM_DIV register. Once the register is set up, the MUTE and/or PLAY commands can be asserted. PCM_DIV cannot be changed "on the fly".

The frequency of LRCLK is given by :

$$f_{LRCLK} = \frac{f_{SCLK}}{32} \text{ ; for 16-bit PCM output}$$

$$f_{LRCLK} = \frac{f_{SCLK}}{64} \text{ ; for 18-bit PCM output}$$

VII.3 - Interrupts Associated with PCM Output

There are two interrupts associated with the PCM output, interrupt 8, "PCM Buffer Underflow", and interrupt 14, "Output of New Frame".

An interrupt 8 is generated (if not masked) when a new output sample is required and the PCM buffer is empty. The PCM buffer, which contains up to 64 samples (i.e. 64 word-pairs in stereo), receives the decoded outputs from the DSP core. If the buffer is empty the output sample will have the value zero. Decoding will not stop. If the PCM buffer becomes full, decoding will stop, but PCM output will not be affected.

An interrupt 14 is generated (if not masked) whenever the first bit of a frame appears at the PCM output.

VIII - DECODER CONTROL

VIII.1 - Control and Status Pins

MUTE forces the output of muted PCM data. PCM muting will be in effect if either this line or the MUTE register is set. Muting does not affect the audio decoding process.

PLAY enables the output of decoded audio data. Output of decoded audio data is enabled only if both this line is asserted and the PLAY register is set. It does not affect the output of muted audio.

PTS becomes active when the first data word associated with a frame that contained a PTS (presentation time stamp) is at the PCM output stage. PTS is active for a duration of 1ms. The PTS associated with the current frame may be read from PTS[32:0]. This register is updated only if its associated interrupt request is enabled.

The falling edge of BOF signals the beginning of a new audio frame. The first sample of the new frame is on the PCM output at the falling edge of this signal. This signal is active for a duration of 180ns.

FS1, FS0 signal the sampling frequency code extracted from the frame header. This data is also available in the PCM_FS register. The FS1 and FS0 pins will reflect the current sampling frequency when the first data point is at the PCM output stage. If enabled, an interrupt 9 is generated at this time if the sampling frequency value has changed.

DMPH1, DMPH0 signal the audio de-emphasis code extracted from the frame header. The same information is also available in the DMPH register. If enabled, an interrupt 10 is generated on a change in the DMPH value. The interrupt occurs and the DMPH1 and DMPH0 pins change state when the corresponding frame is at the PCM output stage.

The action of RESET is described in the following section.

VIII.2 - Initialization of the Decoder

There are two methods of initiating a reset of the STi4500/4510 :

1. Writing 0 or 1 (after which it is automatically restored to the 0 state) to the register RESET.
2. Asserting the RESET pin for a duration of at least 200ns.

Either of these actions will reset the INTR and INTR_EN registers. In addition, asserting the RESET Pin will reset the registers INV_SCLK, MUTE, PLAY, STC_INC and STC_CTL. All other registers must be set up by the microcontroller before decoding is started.

A reset, initiated either by RESET Pin or by register write initiates the following actions :

- The RESET register is set (if not set already).
- The REQ Pin goes high.
- The INTR, INTR_EN and BUFF_LEV registers are reset.
- The registers INV_SCLK, STC_INC, STC_DIV and STC_CTL are cleared (only if reset was activated by RESET Pin).
- The STi4500/4510 checks for the presence of external DRAM and fixes state of bit DRAM_EXT accordingly.
- The DRAM goes through its power-up refresh cycling (only if reset was activated by RESET Pin).
- All data buffers are cleared. This takes multiple clock cycles.
- The MUTE and PLAY registers are reset (only if reset was activated by RESET Pin). This inhibits the output clocks, LRCLK and SCLK, and places PCMDATA in their inactive state.
- All other control registers remain at their pre-existing state
- The STi4500/4510 terminates the reset cycle. The RESET register is cleared, and the REQ Pin goes low. The PCM output clocks and data remain inactive.

Register accesses by the host interface are not disabled during the reset process. However, while the REQ Pin is asserted audio data cannot be input.

The IRQ and IRQOD outputs are low while the RESET Pin is asserted.

Changing of layer or sampling frequency requires a prior reset of the decoder.

VIII.3 - Play and Mute

Once initialized and configured, decoding and output of PCM data is controlled by the commands PLAY and MUTE.

The command PLAY is asserted when both the PLAY register is set and the PLAY Pin is asserted.

The command MUTE is asserted if either the MUTE register or the MUTE Pin is asserted.

The actions of the PLAY and MUTE commands are specified in the Table 1.

VIII - DECODER CONTROL (continued)

Table 1 : Mute and Play Functions

Mute	Play	Function
de-asserted	de-asserted	No output or decoding. SCLOCK, LRCLK, PCMDATA all move into their inactive state. LRCLK completes its current cycle and stops, SCLK completes its last cycle in the second LRCLK frame and stops. Decoding stops when all internal buffers become full.
de-asserted	asserted	Normal decoding and PCM output. When PLAY is re-asserted, PCMDATA resumes where it left off without data loss.
asserted	de-asserted	PCM clocks only, no decoding. PCMDATA becomes low after the output of the last complete sample. LRCLK and SCLK are not stopped. Decoding stops when all internal buffers become full. When PLAY is re-asserted, PCMDATA resumes where it left off without data loss.
asserted	asserted	Decoding and muted output (soft mute). PCMDATA gradually decays to zero. Decoding continues normally. Data consumed as if output were playing.

VIII.4 - Restart

The restart procedure is invoked when it is required to flush all buffers and restart decoding immediately.

Restart is initiated by writing 0 or 1 (after which it is automatically restored to the 0 state) to the RESTART register. A restart initiates the following actions :

- The $\overline{\text{REQ}}$ Pin goes high
- The INTR and INT_EN registers are cleared.
- The BUFF_LEV register is cleared.
- All data buffers are cleared.
- The MUTE, PLAY and all others registers (except those mentioned above) remain in their existing state.
- Registers access is not disabled. However, while the $\overline{\text{REQ}}$ Pin is high audio data cannot be input.
- The STi4500/4510 terminates the restart cycle. The RESTART register is cleared, and the $\overline{\text{REQ}}$ Pin goes low

The DRAM does not go through the power-up refresh cycle during the restart sequence.

VIII.5 - Bitstream Synchronization

The compressed input bit stream must be synchronized before the decompression step may begin. This is done by looking for synchronization words inserted into the data stream at encoding. Synchronization must be done both at the audio frame and at the system packet layer if present.

At the packet level, the audio decoder will look for a valid start code, doing a bit by bit search. Once an audio packet is found, it extracts the presentation time stamp (PTS), if present, and starts the audio synchronization described below.

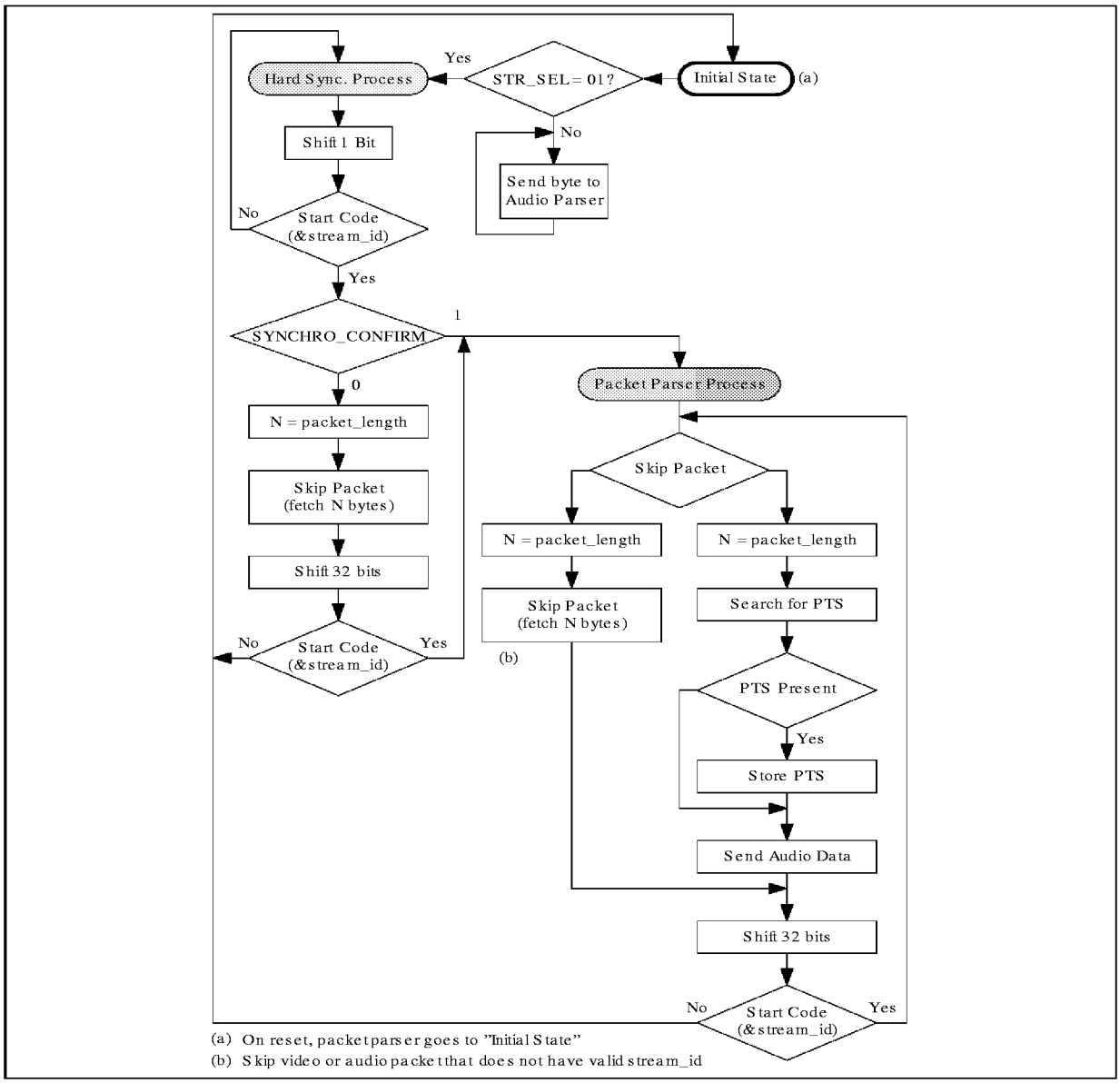
At the audio frame level, there is a non-unique sync word at the beginning of the header. The STi4500/4510 attempts to find this sync word by doing a bit by bit search. When found the action taken depends on the contents of the SYNC_LOCK and LATENCY registers.

VIII - DECODER CONTROL (continued)

VIII.5.1 - Packet Level Synchronization

The complete algorithm is given in Figure 9.

Figure 9 : Packet Synchronization Algorithm



To help the synchronization algorithm ignore an emulated packet synchronization word, an extension of the packet start code to be matched is possible. Depending to the content of registers PACKET_SYNC, AUDIO_ID and AUDIO_ID_EN, synchronization can be made on the 24-bit *packet_start_code_prefix* or can be extended to the *stream_id* field.

VIII - DECODER CONTROL (continued)

Synchronization mode depends on the type of packets received by the STi4500/4510. The decoder can receive either :

1. Multiplexed audio/video bitstream (PACKET_SYNC = 0).
   In this case the STi4500/4510 can receive both video and audio streams multiplexed together. Packet synchronization is possible only on the 24-bit start code. All packets are used by the synchronization algorithm but all non-audio packets and, if AUDIO_ID_EN is set, all audio packets which have a *stream_id* which does not match the AUDIO_ID register value, are not decoded.
2. Multiplexed audio bitstream (PACKET_SYNC = 1).
   In this case, the STi4500/4510 expects to receive only multiplexed audio streams. Synchronization is performed on 27 bits (24 bits *packet_start_code_prefix* + 3 first bits of *stream_id*). All packets are used by the synchronization algorithm but if AUDIO_ID_EN is set, all audio packets that have a *stream_id* which does not match the AUDIO_ID register value are not decoded.
3. Single audio bitstream (PACKET_SYNC = 2, AUDIO_ID_EN=1).
   Synchronization is performed on 32 bits. All packets are used by the synchronization algorithm, and all audio packets that have a *stream_id* which matches the AUDIO_ID register value are decoded.

The SYNCHRO_CONFIRM register is also taken into account in the global synchronization algorithm. If SYNCHRO_CONFIRM = 1, after the first packet synchronization word is found the STi4500/4510 is considered to be synchronized. If SYNCHRO_CONFIRM = 0, after the first packet synchronization word is found, the STi4500/4510 must read the packet length and confirm synchronization by finding the next synchronization word in the correct position.

VIII.5.2 - Audio Frame Synchronization

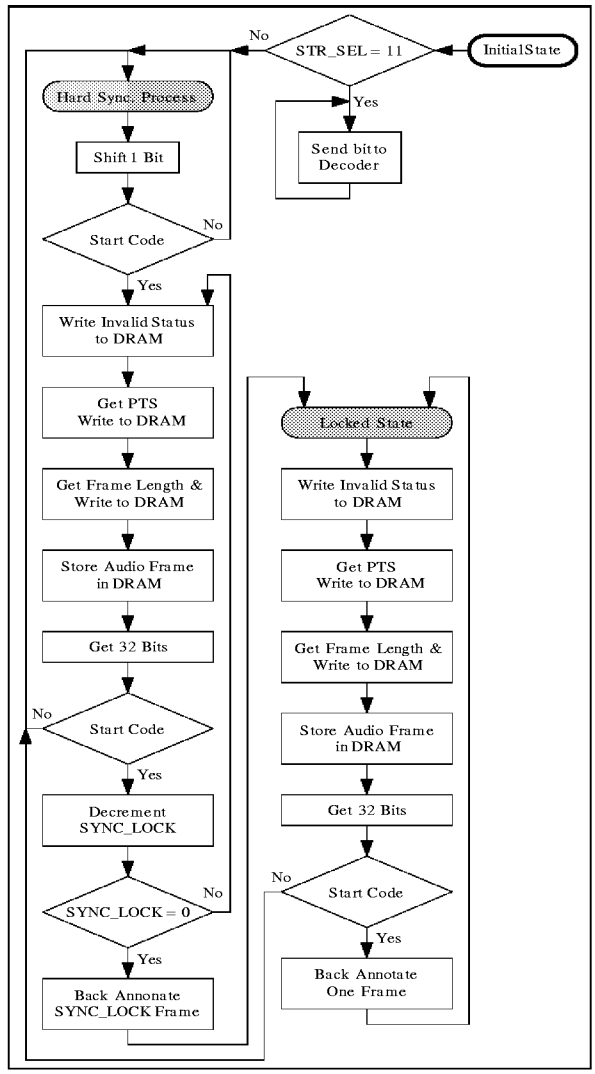
The synchronization algorithm is given in Figure 10.

Because the audio *syncword* can be emulated in the bitstream, it is useful to extend this audio start code to avoid the detection of a false sync word. Each time the STi4500/4510 detects a false sync word during the synchronization process, the delay to reach the locked state increases.

The SYNC_REG register is used for this purpose. When no field of the SYNC_REG register is enabled, the STi4500/4510 saves the layer and sampling frequency information after synchronization has been achieved. This aids the task of resynchronization, should synchronization be lost owing to an error in the audio data or the system layer. This internal register is disabled on RESET or RESTART and will not be reinitialized until the audio parser is synchronized.

The SYNC_LOCK register specifies how many valid synchronization words after the initial one have to be found before entering the locked state. The highest value of SYNC_LOCK (i.e. 3) is assumed when the SYNC_REG register has its default value. The definition of a valid synchronization word depends on the LATENCY register value.

Figure 10 : Audio Frame Synchronization Algorithm



VIII - DECODER CONTROL (continued)

In high latency mode (LATENCY = 1) a valid synchronization word is a sequence of bits that matches the expected word. In addition, the calculated length of the audio frame must be equal to the distance to the start of the next sequence of bits matching the synchronization word. In low latency mode (LATENCY = 0), a valid synchronization word is a sequence of bits matching the expected word. High latency mode is not allowed if no DRAM is present.
In free-format mode one additional register (FREE_FORM) can be used. The FREE_FORM register is a way of specifying the length of an audio frame in free-format mode. This register is 16 bits long and contains the length of the frame in bits.
The method of storing frames in the DRAM is given in section VI.3, "Frame Data Storage Structure and Delay".
By default a frame is always written always "bad" status. The back annotation process writes a "good" status word. A frame with a "bad" status word is decoded using the concealment method specified by the value of SYNC_ECM register.
The algorithm without DRAM is similar except that back annotation is not possible. In this case frames are lost before the locked state is achieved.

VIII.6 - Error Recovery and Concealment

The STi4500/4510 is able to recover from certain detectable errors. For this purpose it has a number of user-selectable error concealment modes.
Detectable errors may be caused by a bad audio frame CRC or by loss of synchronization. Concealment is similar, but may be selected independently by setting the CRC_ECM and SYNC_ECM registers.

The register CRC_ECM defines the action which will be taken upon detection of a CRC error in an input frame :

00 : Disable CRC detection and error concealment
01 : Mute on detection of CRC error
10 : Repeat last valid frame. Repeat once if Layer II, three times if layer I, mute thereafter. Only possible when external DRAM used.
11 : Skip invalid frame

The register SYNC_ECM defines the action which will be taken upon detection of a synchronization error :

00 : Ignore error
01 : Mute on detection of synchronization error
10 : Repeat last valid frame. Repeat once if Layer II, three times if layer I, mute thereafter. Only possible when external DRAM used.
11 : Skip invalid frame

VIII.7 - Ancillary Data Extraction

The ancillary data which may be held at the end of audio frames can be extracted and read from the ANC register. This register constitutes a 32-bit FIFO. The first bit of ancillary data received is stored in bit ANC[0].

The extraction of ancillary data in ANC is started by enabling interrupt 7. An interrupt 7 is generated when either :

1. 32 bits of ancillary data have been received from the bitstream and written into ANC, i.e. when it is full, or
2. the end of a frame is reached.

Register ANC_AV holds the number of bits available in the ancillary data buffer, ANC[31:0]. When ANC[31:24] is read, interrupt 7 is cleared, ANC_AV is cleared and the ancillary data buffer is reinitialized. Decoding stops if the STi4500/4510 tries to write data into ANC when it is full. The normal response would be to read ANC_AV and then ANC. However, if interrupt 7 is disabled (by resetting bit INTR_EN[7]), decoding will continue and the registers ANC and ANC_AV will retain their contents until ANC[31:24] is read. If ANC is not read at the end of the frame, and it is not full, ancillary data bits in the next frame will be appended.

VIII.8 - Bypass Mode

The STi4500/4510 has an audio bypass capability that allows 16-bit PCM data to be loaded directly and passed through to the PCMDATA output.
To set up audio bypass operation the STR_SEL register must be set to the bypass mode (STR_SEL = 3) and then a reset or restart sequence must be executed. While the $\overline{REQ}$ output is low, PCM data can be loaded into the device directly. The data is loaded in exactly the same way as compressed data, using one of the three loading mechanisms available. The data can be input at up to the maximum burst rate of 20 Mbit/s. Data must be input in the sequence: 2 bytes left, 2 bytes right, 2 bytes left, and so on. In each byte-pair, the most significant byte must be loaded first. The external DRAM is not used in bypass mode (the LATENCY register must be reset during bypass). All 16-bit PCM output modes can be used in bypass mode. The volume control is operational in bypass mode. The PCM underflow interrupt (interrupt 8) can be used to detect when all bypass data has been output. To switch back to compressed data input, the STR_SEL register and the LATENCY register must be changed back to select the normal input configuration (STR_SEL = 0 or 1, LATENCY = 0 or 1) and then a reset or restart sequence must be executed.

IX - SYSTEM TIME COUNTER

A System Time Counter (STC) has been added to the STi4500/4510 in order to improve integration in a system which includes a video decoder.
The STC structure is shown in Figure 11. The system time counter itself is constituted by the accumulator and the adder from which its input is taken.
The accumulator clock is derived from an external clock provided by the system (STCCLK), divided by a value programmed into register STC_DIV. After a reset initiated by assertion of the RESET pin, STC_DIV has the value 0 and STCCLK is not divided. STC_INC is also reset after assertion of RESET. Connecting PCMCLK to STCCLK allows the STC to be locked to the audio clock.
The accumulator increment is programmable ; it is defined by the contents of register STC_INC. This gives the possibility to use a fractional division of the input clock at the expense of a loss in STC resolution. This is particularly useful when the PCMCLK is used because typical PCMCLK frequencies are not integer multiples of 90kHz.
The STC accumulator will be augmented by STC_INC every STC_DIV cycles of STCCLK. If the input clock in M/N times the frequency of the desired STC frequency (usually 90khz), then M is stored in STC_DIV and N stored in STC_INC.
The table opposite gives the values of STC_DIV and STC_INC for typical values of PCMCLK frequencies.
The lowest STC resolution is that in the first line of the table. The time between STC updates is 45/90000 = 0.5ms.
The register STC_AUD will latch the STC value at the start of every audio frame (BOF), and the register STC_VID will latch the STC when the display of very picture display starts (signalled by $\overline{\text{VSYNC}}$, available through a pin).
The register STC_CTL is used to transfer data to and from the STC register. Writing to this register with the appropriate bits set will trigger the action. This register is also used to define the polarity of $\overline{\text{VSYNC}}$. Writing to the register with the appropriate bit set will trigger the defined action. The different functions of the STC_CTL register are given in the Table 3.

Table 2

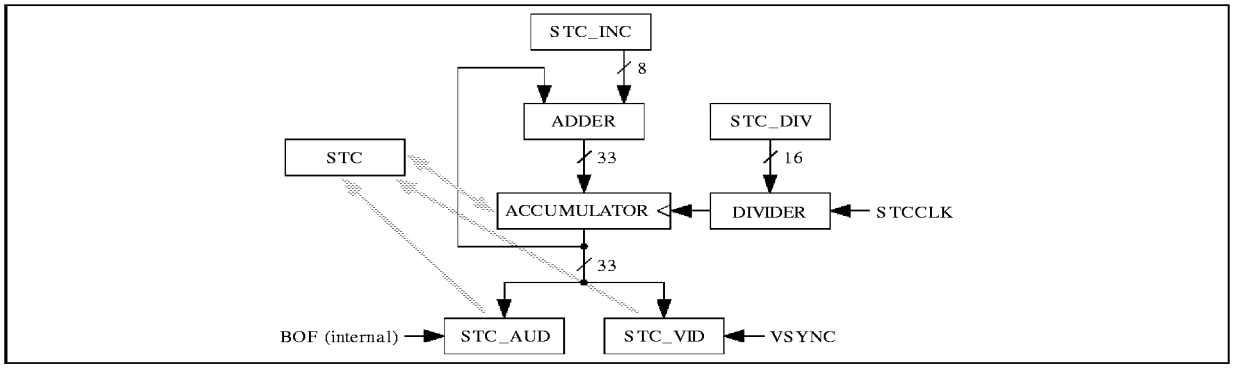
Sampling Frequency	PCMCLK Frequency	STC_DIV	STC_INC
32kHz	8192kHz	4096	45
32kHz	12288kHz	2048	15
44.1kHz	11289.6kHz	3136	25
44.1kHz	16934.4kHz	4704	25
48kHz	12288kHz	2048	15
48kHz	18432kHz	1024	5

Table 3

Bit	Function
7	Must be low
6	STV_VID latched on rising edge of $\overline{\text{VSYNC}}$
5	STV_VID latched on falling edge of $\overline{\text{VSYNC}}$
4	Transfer STC_AUD to STC register
3	Transfer STC_VID to STC register
2	Transfer STC accumulator to STC register
1	Transfer STC to accumulator (Mode 1)
0	Transfer STC to accumulator (Mode 0)

Bits 5 and 6 must not be set together.
The STC register is a 33-bit value and it is spanned by five 8-bit registers. The "Mode 0" mapping is direct but the "Mode 1" mapping is particular, in which the data are mapped exactly as are the SCR, PTS and DTS values in the bitstream. This mapping avoids bit manipulation when transferring values from the bitstream to the register. The two mappings are defined in the STC register description in section X, "REGISTER DESCRIPTIONS".
Mode 0 mapping is applied for read access (STC_CTL bit 2) and Mode 0 write access (STC_CTL bit 0).
Mode 1 is applied write access (STC_CTL bit 1).

Figure 11 : System Time Counter



X - REGISTER DESCRIPTIONS

Registers are listed in alphabetical order. All addresses are in hexadecimal.
All unspecified addresses of the register map are reserved, and must not be written to. Unspecified bits of user-accessible registers have no function.

ANC - Ancillary Data Buffer

	7	0
09	ANC[31:24]	
08	ANC[23:16]	
07	ANC[15:8]	
06	ANC[7:0]	

Address : 09-06
Type : R
Reset State : undefined

Description
The 4 8-bit ancillary data registers constitute a 32-bit FIFO which holds the ancillary data extracted from audio frames. The first bit of ancillary data received is stored in bit ANC[0].
The extraction of ancillary data in ANC is started by enabling interrupt 7. An interrupt 7 is generated when 32 bits have been written into ANC, i.e. when it is full.
When ANC[31:24] is read, ANC_AV is cleared and the ancillary data buffer is reinitialized.

ANC_AV - Ancillary Data Available

5	0
ANC_AV[5:0]	

Address : 6C
Type : R
Reset State : 0

Description
This register holds the number of bits available in the ancillary data buffer, ANC[31:0].
It is cleared by reading ANC[31:24].

ATTEN_L - Left Channel Attenuation

5	0
ATTEN_L[5:0]	

Address : 1E
Type : R/W
Reset State : undefined

Description
This register defines the left channel attenuation in steps of 2dB. The minimum attenuation is 0dB, the maximum is 2 X 63 = 126dB.

ATTEN_R - Right Channel Attenuation

5	0
ATTEN_R[5:0]	

Address : 20
Type : R/W
Reset State : undefined

Description
This register defines the right channel attenuation in steps of 2dB. The minimum attenuation is 0dB, the maximum is 2 X 63 = 126B.

AUD_ID - Audio Stream ID

4	0
AUD_ID[4:0]	

Address : 22
Type : R/W
Reset State : undefined

Description
This value stored in this register is only taken into account if AUD_ID_EN is set.
This register specifies the number (between 0 and 31) of the audio stream which is to be decoded. The stream number is defined in the field *stream_id* of the packet header. All other packets will be discarded.
If AUD_ID_EN is reset, then all audio packets are decoded.

AUD_ID_EN - Audio Stream ID Enable

bit 0
AUD_ID_EN

Address : 24
Type : R/W
Reset State : undefined

Description
If this bit is reset, then the contents of AUD_ID are ignored.
If it is set, then the register AUD_ID is taken into account.
0 : Ignore AUD_ID
1 : Use AUD_ID

X - REGISTER DESCRIPTIONS (continued)

BALE_LIM - Buffer Almost Empty Limit

6	0
BALE_LIM[6:0]	

Address : 69
Type : R/W
Reset State : undefined

Description

This register defines the level of data, in units of blocks, in the external DRAM at or below which an interrupt 3 can be generated.
A block can contain up to 8K bits of data. The external DRAM can contain up to 128 blocks. For Layer I frames, one block is used to store one frame of compressed data. For Layer II frames, two blocks are used to store one frame of compressed data.

BALF_LIM - Buffer Almost Full Limit

6	0
BALF_LIM[6:0]	

Address : 6B
Type : R/W
Reset State : undefined

Description

This register defines the level of data, in units of blocks, in the external DRAM at or above which an interrupt 4 can be generated.
A block can contain up to 8K bits of data. The external DRAM can contain up to 128 blocks. For Layer I frames, one block is used to store one frame of compressed data. For Layer II frames, two blocks are used to store one frame of compressed data.

BUFF_LEV - DRAM Buffer Level

	6	0
13	7	BUFF_LEV[14:8]
12		BUFF_LEV[7:0]

Address : 13-12
Type : R
Reset State : 0. Also cleared on restart.

Description

This register indicates the data level in the external DRAM buffer. BUFF_LEV[14:8] gives the number of complete blocks. BUFF_LEV[7:0] gives the remainder, in units of 4 bytes (32 bits). When the DRAM is full, the value of BUFF_LEV[14:8] is 124, and the value of BUFF_LEV[7:0] is 0.
A block can contain up to 8K bits of data. The external DRAM can contain up to 128 blocks. For Layer I frames, one block is used to store one frame of compressed data. For Layer II frames, two blocks are used to store one frame of compressed data.

CRC_ECM - CRC Error Concealment Mode

1	0
CRC_ECM - CRC[1:0]	

Address : 2A
Type : R/W
Reset State : undefined

Description

This register defines the action which will be taken upon detection of a CRC error in an input frame.

00 : Disable CRC detection and error concealment
01 : Mute on detection of CRC error
10 : Repeat last valid frame. Repeat once if Layer II, three times if layer I, mute thereafter. Only possible when external DRAM used.
11 : Skip invalid frame

DATAIN - Compressed Data Input

7	0
DATAIN[7:0]	

Address : 18
Type : R/W
Reset State : undefined

Description

This register is provided to allow the transfer of compressed data across the microcontroller interface. When this mode of data entry is used, the signal DSTRB must be inactive.

X - REGISTER DESCRIPTIONS (continued)

DMPH - De-Emphasis Mode

1		0
	DMPH[1:0]	

Address : 46
Type : R
Reset State : undefined

Description

This register is set with the value of the emphasis field of the frame currently being decoded.

00 : None
01 : 50/15µs
10 : Reserved value
11 : ITU-T J.17

DRAM_EXT - External Memory Status

bit 0
DRAM_EXT

Address : 3E
Type : R
Reset State : see below

Description

The value of this bit is determined automatically on power-up.

0 : No external DRAM present. Only the internal 256-byte input FIFO buffer is used.
1 : External DRAM present. Both this memory and the input FIFO are used.

FIFO_THRES - Input FIFO Threshold

7		0
	FIFO_THRES[7:0]	

Address : 52
Type : R/W
Reset State : undefined

Description

This value loaded into this register defines the input FIFO level at which an interrupt 12 can be generated. The level is defined as a byte address, in the range 0 to 255.

An interrupt can be generated each time the FIFO level is equal to FIFO_THRES, regardless of whether it was approached from above or below.
When external DRAM is installed, interrupt 12 should be masked, since interrupts 3 and 4 would normally be used for buffer level indication.

FREE_FORM - Free-Format Frame Length

	7	0
15	FREE_FORM[15:8]	
14	FREE_FORM[7:0]	

Address : 15-14
Type : R/W
Reset State : undefined

Description

When free-format decoding is used (*bitrate_index* = 0), the frame length, if known, can be loaded into this register, in units of bits. (In free-format, the frame length cannot be determined from bitstream parameters).
The length loaded into FREE_FORM is used in the internal synchronization algorithm.
If the frame length is not known, FREE_FORM must be loaded with zero.

HEADER - Frame Header

	7	0
61	HEADER[31:24]	
60	HEADER[23:16]	
5F	HEADER[15:8]	
5E	HEADER[7:0]	

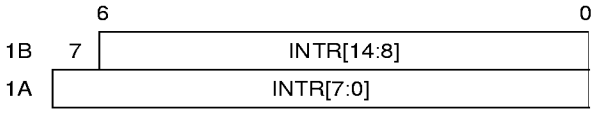
Address : 61-5E
Type : R
Reset State : undefined

Description

This 32-bit register contains the header of the frame currently being decoded.
This register is updated after interrupt 1 is enabled. An interrupt 1 is generated when a valid header has been received.
The contents are retained until HEADER[31:24] is read.

X - REGISTER DESCRIPTIONS (continued)

INTR - Interrupt Request Register



Address : 1B-1A
Type : R
Reset State : 0. Also cleared on restart.

Description

An interrupt is signalled by a 100ns pulse on $\overline{IRQ}$ whenever one of the bits of INTR becomes set.

This can only occur if the corresponding bit is set in the INTR_EN register.

The INTR register is cleared on reset (assertion of $\overline{RESET}$ Pin or setting of RESET register), or restart (setting the RESTART register).

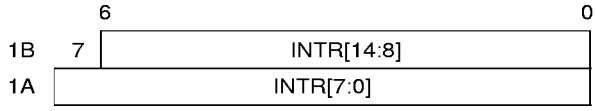
Also the most significant byte, and bits 3-5 of the least significant byte of INTR can be independently cleared by reading.

Bits 0-2 and 7 are cleared by a different method, as indicated in the notes below the following table.

No	Condition Signalled
14	First bit of new frame at PCM output
13	Input FIFO full
12	Input FIFO level = FIFO_THRES
11	External DRAM full
10	De-emphasis changed
9	Sampling frequency changed
8	PCM output buffer underflow
7	Ancillary data register full (see Note 1)
6	not used
5	CRC error detected
4	Blocks in DRAM BALF_LIM
3	Blocks in DRAM BALE_LIM
2	Valid PTS registered (see Note 2)
1	Valid header registered (see Note 3)
0	Change in synchronization status (see Note 4)

Notes : 1. ANC[31:24] must be read in order to clear bit INTR[7] and to reinitialize the ancillary data buffer.
2. PTS[32] must be read in order to clear bit INTR[2] and to reinitialize the PTS register.
3. HEADER[31:24] must be read in order to clear bit INTR[1] and to reinitialize the HEADER register.
4. SYNC_ST must be read in order to clear bit INTR[0] and to reinitialize the SYNC_ST register.

INTR_EN - Interrupt Mask Register



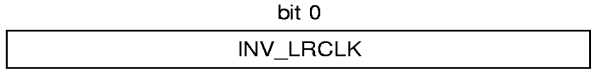
Address : 1D-1C
Type : R/W
Reset State : 0. Also cleared on restart.

Description

A one in any bit position of this register will enable the corresponding bit of the INTR register.
In addition, setting certain bits of this register have additional actions, as specified below :

- Setting INTR_EN[7] enables the reading of ancillary data into ANC
- Setting INTR_EN[2] enables the updating of the PTS register.
- Setting INTR_EN[1] enables the updating of the HEADER register.
- Setting INTR_EN[0] enables the updating of the SYNC_ST register.

INV_LRCLK - LRCLK Polarity

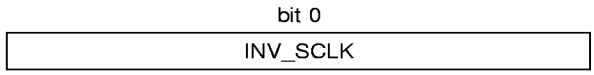


Address : 11
Type : R/W
Reset State : 0 after assertion of $\overline{RESET}$ Pin only

Description

This bit is used to define the polarity of the output signal LRCLK.
0 : Left channel when LRCLK = 1
1 : Left channel when LRCLK = 0

INV_SCLK - SCLK Polarity



Address : 53
Type : R/W
Reset State : 0 after assertion of $\overline{RESET}$ Pin only

Description

This bit defines the polarity of the PCM bit clock output SCLK.
0 : The LRCLK and PCMDATA outputs change on the falling edge of SCLK. The external DAC will sample LRCLK and PCMDATA on the rising edge of SCLK.
1 : The LRCLK and PCMDATA outputs change on the rising edge of SCLK. The external DAC will sample LRCLK and PCMDATA on the falling edge of SCLK (Figure 7).

X - REGISTER DESCRIPTIONS (continued)

LATENCY - Latency Selection

bit 0

LATENCY

Address : 3C
Type : R/W
Reset State : undefined

Description

This bit is used to select the latency mode of the decoder.

0 : Low latency mode. The decoding latency is less than 5 ms (see section IV.6, "Latency"). In this mode the STi4500/4510 is forced to work without external DRAM, even if installed. This mode must be selected if audio bypass is required (STR_SEL = 3).

1 : High latency mode. The latency is greater than one frame period. This mode must not be selected unless external DRAM is installed. In high latency mode synchronization detection is more robust, and loss of synchronization can be checked for before the decoding of each frame.

MUTE - Mute

bit 0

MUTE

Address : 30
Type : R/W
Reset State : 0 after assertion of $\overline{\text{RESET}}$ Pin only

Description

The output of this register is ORed with the $\overline{\text{MUTE}}$ Pin to form the mute command. The action of the mute command is explained in section VIII.3, "Play and Mute" .

PACKET_SYNC - Packet Sync Mode

1 0

PACKET_SYNC[1:0]

Address : 23
Type : R/W
Reset State : undefined

Description

This register defines the packet synchronization mode.

00 : Synchronize only on 24-bit *packet_start_code_prefix* (Multiplexed audio/video bitstream).

01 : Synchronize both on 24-bit *packet_start_code_prefix* and first 3 bits of *stream_id*. (Multiplexed audio bitstream).

10 : Synchronize both on 24-bit *packet_start_code_prefix* and all 8 bits of *stream_id*. (Audio bitstream with unique id).

PCM_18 - PCM Output Precision

bit 0

PCM_18

Address : 16
Type : R/W
Reset State : undefined

Description

This bit defines the PCM output precision.

0 : 16-bit PCM data output
1 : 18-bit PCM data output

PCM_DIF - PCM Output Justification

bit 0

PCM_DIF

Address : 6F
Type : R/W
Reset State : undefined

Description

This bit selects whether the PCM output data is right or left justified with respect to the 32-clock frame when in 18-bit mode (i.e. when PCM_18 = 1). This bit is has no significance when in 16-bit mode (i.e. when PCM_18 = 0).

0 : 18-bit PCM data is right justified (i.e. occupies the last 18 cycles of each 32-cycle frame)

1 : 18-bit PCM data is left justified (i.e. occupies the first 18 cycles of each 32-cycle frame when PCM_FORMAT = 1, or the next 18 when PCM_FORMAT = 0).

X - REGISTER DESCRIPTIONS (continued)

PCM_DIV - PCM Clock Divider

5							0
PCM_DIV[5:0]							

Address : 6E
Type : R/W
Reset State : undefined

Description

The number loaded into this register, in the range 0 to 63, defines the ratio of the frequency of the PCM bit clock, SCLK, to that of PCMCLK, according to the relationship :

$$f_{SCLK} = \frac{f_{PCMCLK}}{2 \cdot (PCM\_DIV + 1)}$$

For example, PCM_DIV is loaded with 0, the frequency of SCLK is one half of the frequency of PCMCLK, while if PCM_DIV is loaded with 63, the frequency of SCLK is one 128th of the frequency of PCMCLK.
The value of PCM_DIV = 16 is reserved. If this number is loaded, the divider is bypassed and the frequency of SCLK is equal to the frequency of PCMCLK.
PCM_DIV must be set up before the output of SCLK starts. This can be done by first disabling PCM outputs by de-asserting the MUTE and PLAY commands, and then writing to the PCM_DIV register. Once the register is set up, the MUTE and/or PLAY commands can be asserted. PCM_DIV cannot be changed "on the fly".

PCM_FORMAT - PCM Output Format

bit 0
PCM_FORMAT

Address : 19
Type : R/W
Reset State : undefined

Description

This bit is used to select the I^2S-compatible PCM output format when in 18-bit left-justified mode (i.e. when PCM_18 = 1 and PCM_DIF = 1). In this mode the most- significant bit of the PCM data is output one cycle later than the change of LRCLK. PCM_FORMAT has no significance when PCM_18 =0.

0 : I^2S-compatible PCM output
1 : Standard format (most-significant bit of data coincident with LRCLK)

PCM_FS - Sampling Frequency

1							0
PCM_FS[1:0]							

Address : 44
Type : R
Reset State : undefined

Description

This register is loaded with the sampling frequency code extracted from the bitstream. This is equal to the frequency of the output LRCLK.

00 : 44.1kHz
01 : 48kHz
10 : 32kHz
11 : reserved

PCM_ORD - PCM Output Bit Order

bit 0
PCM_ORD

Address : 38
Type : R/W
Reset State : undefined

Description

This bit determines the order of PCM data output when in 16-bit mode (i.e. when PCM_18 = 0). It has no significance when PCM_18 = 1, when data is always output most-significant bit first.

0 : Most-significant bit output first
1 : Least-significant bit output first

PLAY - Play

bit 0
PLAY

Address : 2E
Type : R/W
Reset State : 0 after assertion of $\overline{\text{RESET}}$ Pin only

Description

The output of this register is ANDed with the $\overline{\text{PLAY}}$ Pin to form the play command. The action of the mute command is explained in section VIII.3, "Play and Mute" .

X - REGISTER DESCRIPTIONS (continued)

PTS - Presentation Time Stamp

	7	0
66		32
65	PTS[31:24]	
64	PTS[23:16]	
63	PTS[15:8]	
62	PTS[7:0]	

Address : 66-62
Type : R
Reset State : undefined

Description

This 33-bit register contains the PTS associated with the frame currently being decoded.

This register is updated after interrupt 2 is enabled. An interrupt 2 is generated when a valid PTS has been received.

The contents are retained until PTS[32] is read.

REPEAT - Repeat Next Frame

bit 0

REPEAT

Address : 34
Type : R/W
Reset State : 0 (command)

Description

When this bit is set, the next audio frame is repeated, and then the REPEAT bit is automatically reset.

This command is only valid when external DRAM is installed.

RESET - Software Reset

bit 0

RESET

Address : 40
Type : R/W
Reset State : 0 (command)

Description

Writing a 0 or 1 to this bit has an equivalent function to asserting the hardware reset pin, RESET, except that the following registers are not cleared :
- INV_SCLK
- MUTE
- PLAY
- STC_INC
- STC_DIV
- STC_CTL

This bit is reset automatically after being set. STi4500/4510 reset actions are described in section VIII.2, "Initialization of the Decoder" .

RESTART - Restart

bit 0

RESTART

Address : 42
Type : R/W
Reset State : 0 (command)

Description

When this bit is set, all data buffers are flushed, and then the RESTART bit is automatically reset. In addition the INTR and INTR_EN registers are cleared.

SIN_EN - Enable Serial Input

bit 0

SIN_EN

Address : 70
Type : R/W
Reset State : undefined

Description

This bit determines whether compressed data input is serial (input through SIN pin), or parallel (input through SDATA[7:0] pins).

0 : Parallel data input
1 : Serial data input

SKIP - Skip Next Frame

bit 0

SKIP

Address : 32
Type : R/W
Reset State : 0 (command)

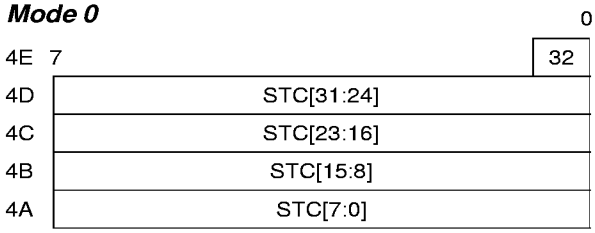
Description

When this bit is set, the next audio frame is skipped, and then the SKIP bit is automatically reset.

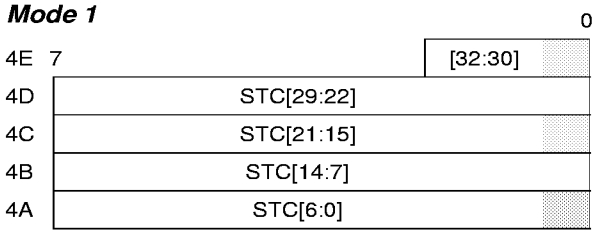
X - REGISTER DESCRIPTIONS (continued)

STC - System Time Clock Access Register

Mode 0



Mode 1



Address : 4E-4A
Type : R/W
Reset State : undefined

Description

This register is used for read and write access to the STC accumulator, and for read access to the STC_AUD and STC_VID registers. Data transfers are controlled by the STC_CTL register.
Two formats for data transfer into the STC accumulator are defined. These are shown as "Mode 0" and "Mode 1" above. Mode 1 is provided in order to give compatibility with the format of the SCR, PTS and DTS fields in the MPEG bitstream, between which are inserted marker bits.

STC_CTL - STC Control

Address : 21
Type : R/W
Reset State : 0 after assertion of $\overline{\text{RESET}}$ Pin only

Description

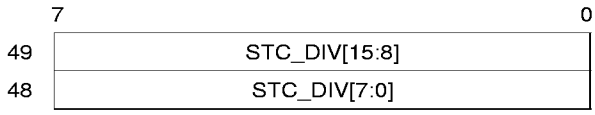
This register is used to define the polarity of $\overline{\text{VSYNC}}$, and to control the transfer of data to and from the STC register.

Writing to the register with the appropriate bit set will trigger the defined action.

Bit	Function
7	Must be low
6	STV_VID latched on rising edge of $\overline{\text{VSYNC}}$
5	STV_VID latched on falling edge of $\overline{\text{VSYNC}}$
4	Transfer STC_AUD to STC register
3	Transfer STC_VID to STC register
2	Transfer STC accumulator to STC register
1	Transfer STC to accumulator (Mode 1)
0	Transfer STC to accumulator (Mode 0)

Bits 5 and 6 must not be set together.

STC_DIV - STC Divisor

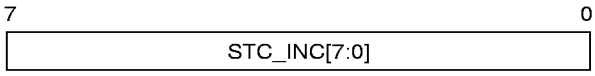


Address : 49-48
Type : R/W
Reset State : 1 after assertion of $\overline{\text{RESET}}$ Pin only

Description

This register defines the number by which the input clock STCCLK is divided before being used to clock the STC accumulator.
This value, together with that loaded into STC_INC, define the internal STC rate.

STC_INC - STC Accumulator Increment



Address : 10
Type : R/W
Reset State : 0 after assertion of $\overline{\text{RESET}}$ Pin only

Description

This register defines the amount by which the STC accumulator is incremented on every cycle of the divided STCCLK.
This value, together with that loaded into STC_DIV, define the internal STC rate.

X - REGISTER DESCRIPTIONS (continued)

STR_SEL - Input Stream Selection

1		0
STR_SEL[1:0]		

Address : 36
Type : R/W
Reset State : undefined

Description

This register defines the type of input bitstream expected by the STi4500/4510.

00 : MPEG audio elementary stream
01 : MPEG packet stream
10 : reserved
11 : PCM data (select bypass mode)

SYNC_CONF - Sync Confirmation Mode

bit 0
SYNC_CONF

Address : 25
Type : R/W
Reset State : undefined

Description

This bit selects one of two options in the packet synchronization algorithm.

0 : After the first valid packet start code and stream id are found, the packet length is used to locate the next start code and stream id before synchronization is confirmed and audio decoding starts.
1 : Synchronization is confirmed when the first valid packet start code and stream id are found.

SYNC_ECM - Sync Error Concealment Mode

1		0
SYNC_ECM[1:0]		

Address : 2C
Type : R/W
Reset State : undefined

Description

This register defines the action which will be taken upon detection of a synchronization error.

00 : Ignore error
01 : Mute on detection of synchronization error
10 : Repeat last valid frame. Repeat once if Layer II, three times if layer I, mute thereafter. Only possible when external DRAM used.
11 : Skip invalid frame

SYNC_LOCK - Sync Words Until Lock

1		0
SYNC_LOCK[1:0]		

Address : 28
Type : R/W
Reset State : undefined

Description

This register defines how many valid synchronization words after the initial one must be found before locking audio frame synchronization.
When SYNC_REG is set to its default value, the STi4500/4510 assumes that SYNC_LOCK is set to the value 3.
Synchronization error concealment is still enabled when SYNC_LOCK has the value zero.

X - REGISTER DESCRIPTIONS (continued)

STC_REG - Sync Word Extension

7							0
STC_REG[7:0]							

Address : 27
Type : R/W
Reset State : undefined

Description

This register defines an extension to the frame synchronization word which can be used to increase the reliability of synchronization when the layer number, bit rate or sampling frequency are known. The three fields are defined in the following tables.
Programming of this register is mandatory.

Layer Field

Bits 7,6	
11	Layer I
10	Layer II
00	This field not used

Bit Rate Field

Bits 5-2	Layer I	Layer II
0000	free format	free format
0001	32 kbits	32 kbits
0010	64 kbits	48 kbit/s
0011	96 kbit/s	56 kbit/s
0100	128 kbit/s	64 kbit/s
0101	160 kbit/s	80 kbit/s
0110	192 kbit/s	96 kbit/s
0111	224 kbit/s	112 kbit/s
1000	256 kbit/s	128 kbit/s
1001	288 kbit/s	160 kbit/s
1010	320 kbit/s	192 kbit/s
1011	352 kbit/s	224 kbit/s
1100	384 kbit/s	256 kbit/s
1101	416 kbit/s	320 kbit/s
1110	448 kbit/s	384 kbit/s
1111	This field not used	This field not used

Sampling Frequency Field

Bits 1,0	
00	44.1kHz
01	48kHz
10	32Hz
11	This field not used

Examples

1. Layer II, 48kHz sampling frequency, variable bit rate : STC_REG = 10111101_2
2. Parameters unknown : STC_REG = 00111111_2

SYNC_ST - Synchronization Status

1		0
SYNC_ST[1:0]		

Address : 26
Type : R
Reset State : undefined

Description

This register is loaded with the synchronization status on every synchronization cycle. This status values are:
00 : Unlocked
01 : Attempting to recover lost synchronization
11 : Locked

If the status changes an interrupt 0 is generated. The status must then be read and the interrupt cleared by reading SYNC_ST.

VERSION - Version Register

7							0
VERSION[7:0]							

Address : 6D
Type : R

Description

This register holds the chip version number, "x.y", where x is represented by bits 6-4, and y by bits 3-0. Bit 7 is always 1.

The version numbers which currently exist are:
1.0 : VERSION = 1001000_2
1.1 : VERSION = 10010001_2
2.0 : VERSION = 10100000_2
2.1 : VERSION = 10100001_2

XI - ELECTRICAL SPECIFICATION

XI.1 - Absolute Maximum Ratings

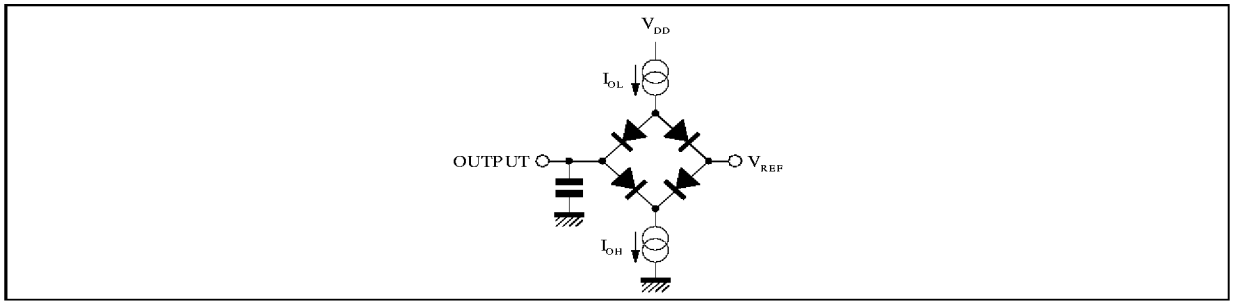
Symbol	Parameter	Value	Unit
V_{DD}	Power Supply	6	V
V_I, V_O	Voltages on Input and Output Pins	-1, V_{DD} + 0.5	V
T_{stg}	Storage Temperature	-65, +150	°C
T_{oper}	Ambient Operating Temperature	0, +70	°C

XI.2 - DC Electrical Characteristics (V_{DD} = 5V ± 5%, T_{amb} = 0 to 70°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage		4.75		5.25	V
I_{DD}	Average Power Supply Current	C_{LOAD} = 50pF on all outputs $f_{primary}$ = 24MHz, all inputs at V_{DD} or 0V $f_{primary}$ = 0Hz		120 ?		mA mA
V_{IL}	Input Logic Low Voltage				2.4	V
V_{IH}	Input Logic High Voltage		2.75			V
	Input Leakage Current Inputs I/Os	V_{DD} = 5.25V, 0 ≤ V_{IN} ≤ V_{DD}	 -5 -1		 +5 +1	 µA µA
V_{OL}	Output Logic Low Voltage	V_{DD} = 4.75, I_{LOAD} = 500µA			0.28	V
V_{OH}	Output Logic High Voltage	V_{DD} = 4.75, I_{LOAD} = -500µA	4.5			V
C_{IN}	Input Capacitance	V_{offset} = 2.5V, f = 1MHz			10	pF

XI.3 - AC Electrical Characteristics (V_{DD} = 5V ± 5%, T_{amb} = 0 to 70°C)

Figure 11 : Test Load Circuit



Test Loads

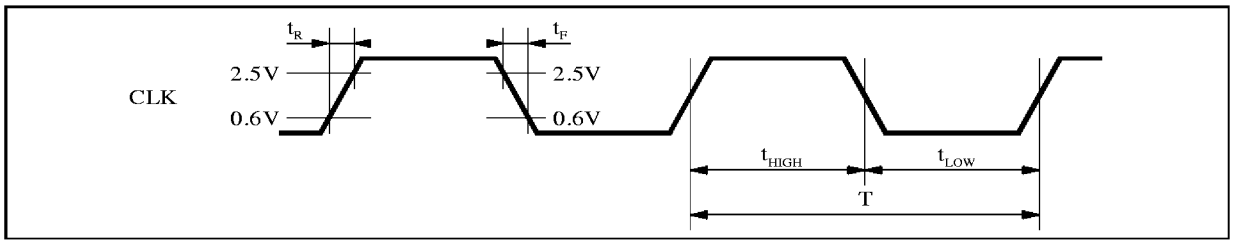
Output	I_{OL}	I_{OH}	C_L	V_{REF}
All Ouputs except I_{RQOD}	5mA	5mA	30pF	1.5V
I_{RQOD}	5mA	5mA	30pF	3.5V

XI - ELECTRICAL SPECIFICATION (continued)

XI.3.1 - Primary Clock

(Timings other than rise and fall times are specified with respect to a threshold of 1.5V)

Figure 12 : Primary Clock



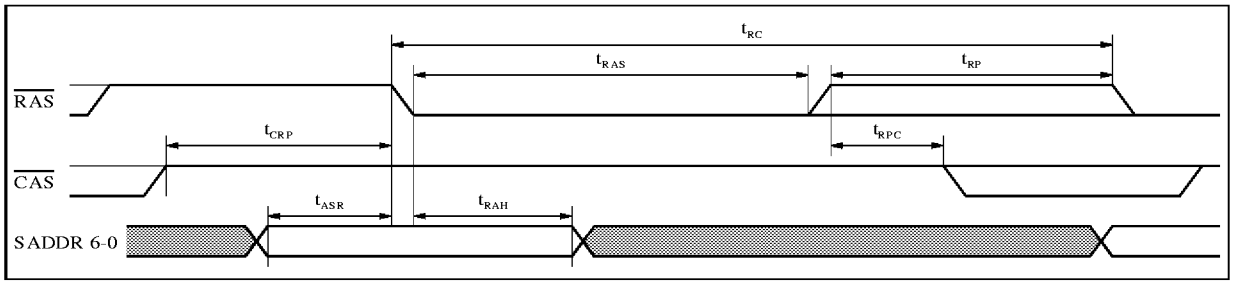
Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Primary Clock Period (see Note 1)	35.75		45.5	ns
t_{HIGH}	Clock High Time	10			ns
t_{LOW}	Clock Low Time	10			ns
t_R	Clock Rise Time	5			ns
t_F	Clock Fall Time	5			ns

Note 1 : This corresponds to a maximum primary clock frequency of 28MHz.

XI.3.2 - DRAM Interface

(All timing measurements are made with respect to thresholds of 0.8V and 2.4V)

Figure 13 : RAS only Refresh Cycle



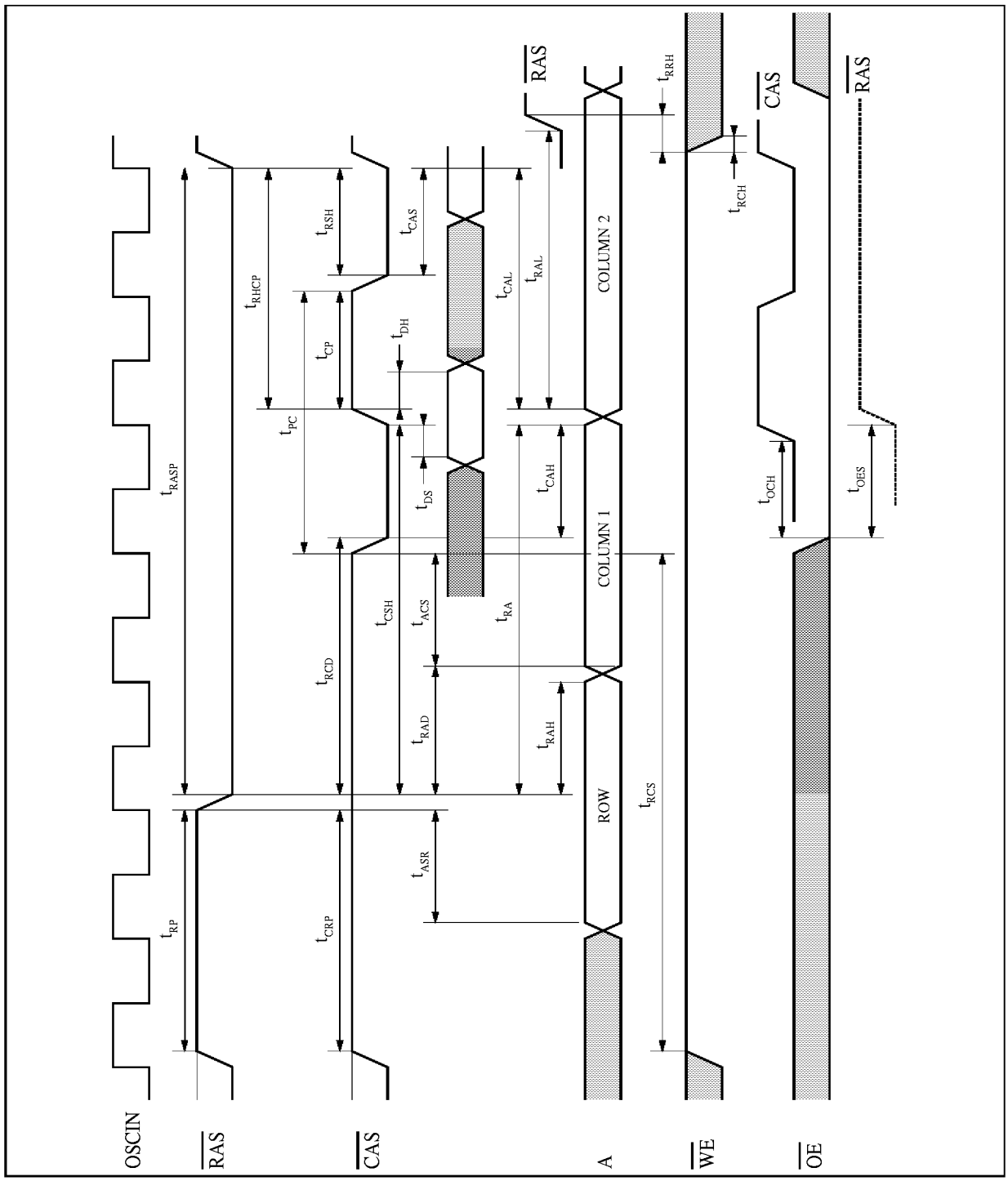
RAS only Refresh Cycle

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RC}	Cycle Time	5.25 T			ns
t_{RP}	$\overline{RAS}$ Precharge Time	2.5 T			ns
t_{RAS}	$\overline{RAS}$ Pulse Width	2.75 T			ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0.5 T			ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0.5 T			ns
t_{ASR}	Row Adress Set-up Time	20			ns
t_{RAH}	Row Adress Hold Time	70			ns

Note : T : primary clock period .

XI - ELECTRICAL SPECIFICATION (continued)

Figure 14 : Page Mode Read Cycle



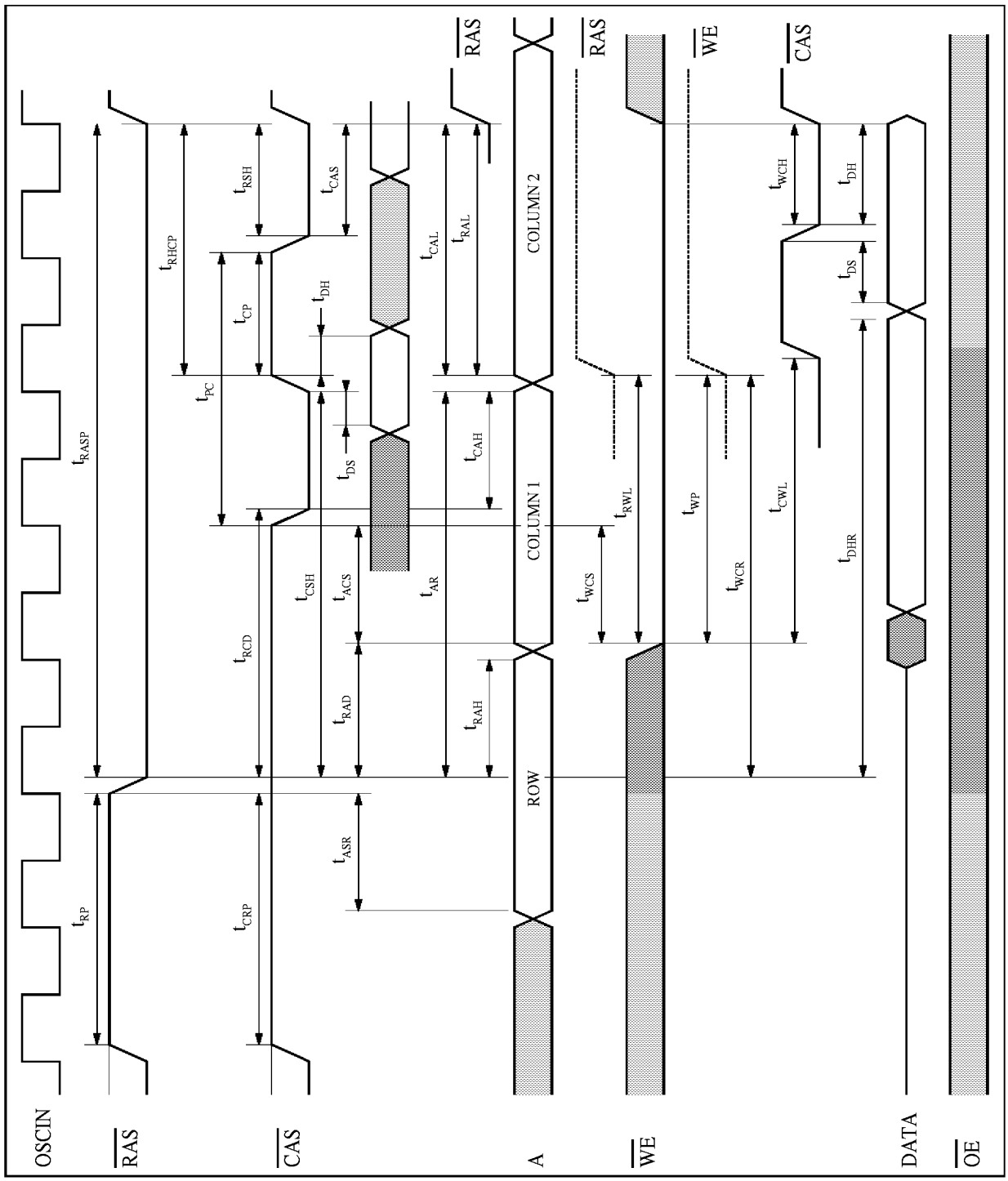
XI - ELECTRICAL SPECIFICATION (continued)

Page Mode Read Cycle

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RC}	Read cycle time	7 T			ns
t_{RP}	$\overline{RAS}$ precharge time	2.5 T			ns
t_{RASP}	$\overline{RAS}$ pulse width	4.5 T			ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	2.5 T			ns
t_{RCD}	$\overline{RAS}$ low to $\overline{CAS}$ low delay time	1.75 T			ns
t_{PC}	Fast page mode read cycle time	1.75 T			ns
t_{CP}	$\overline{CAS}$ precharge time	0.75 T			ns
t_{RHCP}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	1.5 T			ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$	0.75 T			ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$	2.75 T			ns
t_{CAS}	$\overline{CAS}$ pulse width	0.75 T			ns
t_{ASR}	Row address set-up time to $\overline{RAS}$	0.5 T			ns
t_{RAH}	Row address hold time after $\overline{RAS}$	0.6 T			ns
t_{ASC}	Column address set-up time to $\overline{CAS}$	0.5 T			ns
t_{RAD}	Column address delay time from $\overline{RAS}$	1.25 T			ns
t_{CAH}	Column address hold time from $\overline{CAS}$	0.75 T			ns
t_{AR}	Column address hold time from $\overline{RAS}$	2.5 T			ns
t_{CAL}	Column address to $\overline{CAS}$ lead time	1.75 T			ns
t_{RAL}	Column address to $\overline{RAS}$ lead time	1.75 T			ns
t_{DS}	Data in set-up time to $\overline{CAS}$ rising edge	0.5 T			ns
t_{DH}	Data in hold time from $\overline{CAS}$ rising edge	0.75 T			ns
t_{RCS}	Read command to $\overline{CAS}$ set-up time	0.5 T			ns
t_{RCH}	Read command from $\overline{CAS}$ hold time	0.5 T			ns
t_{RRH}	Read command from $\overline{RAS}$ hold time	0.5 T			ns
t_{OCH}	$\overline{CAS}$ from $\overline{OE}$ hold time	1 T			ns
t_{OES}	$\overline{RAS}$ from $\overline{OE}$ hold time	2 T			ns

XI - ELECTRICAL SPECIFICATION (continued)

Figure 15 : Page Mode Early Write Cycle



XI - ELECTRICAL SPECIFICATION (continued)

Page Mode Early Write Cycle

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RP}	$\overline{RAS}$ precharge time	2.5 T			ns
t_{RASP}	$\overline{RAS}$ pulse width	4.5 T			ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	2.5 T			ns
t_{RCD}	$\overline{RAS}$ low to $\overline{CAS}$ low delay time	1.75 T			ns
t_{PC}	Fast page mode read cycle time	1.75 T			ns
t_{CP}	$\overline{CAS}$ precharge time	0.75 T			ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$	0.75 T			ns
t_{CSH}	$\overline{CAS}$ hold time after RAS	2.75 T			ns
t_{CAS}	$\overline{CAS}$ pulse width	0.75 T			ns
t_{ASR}	Row address set-up time to $\overline{RAS}$	0.5 T			ns
t_{RAH}	Row address hold time after $\overline{RAS}$	0.6 T			ns
t_{ASC}	Column address set-up time to $\overline{CAS}$	0.5 T			ns
t_{RAD}	Column address delay time from $\overline{RAS}$	1.25 T			ns
t_{CAH}	Column address hold time from $\overline{CAS}$	0.75 T			ns
t_{AR}	Column address hold time from $\overline{RAS}$	2.5 T			ns
t_{CAL}	Column address to $\overline{CAS}$ lead time	1.75 T			ns
t_{RAL}	Column address to $\overline{RAS}$ lead time	1.75 T			ns
t_{WCS}	Write command set-up time to $\overline{CAS}$	0.5 T			ns
t_{RWL}	Write command to $\overline{RAS}$ lead time	1 T			ns
t_{CWL}	Write command to $\overline{CAS}$ lead time	1 T			ns
t_{WCR}	Write command hold time after $\overline{RAS}$	3.25 T			ns
t_{WCH}	Write command hold time after $\overline{CAS}$	0.75 T			ns
t_{WP}	Write command pulse width	2 T			ns
t_{DS}	Data in set-up time to $\overline{CAS}$ rising edge	0.5 T			ns
t_{DH}	Data in hold time from $\overline{CAS}$ rising edge	0.75 T			ns
t_{DHR}	Data hold time after $\overline{RAS}$	2.5 T			ns

XI - ELECTRICAL SPECIFICATION (continued)

XI.3.3 - Microcontroller Interface Timing

(All timing measurements are made with respect to a threshold of 1.5V)

Figure 16 : Read Cycle Timing

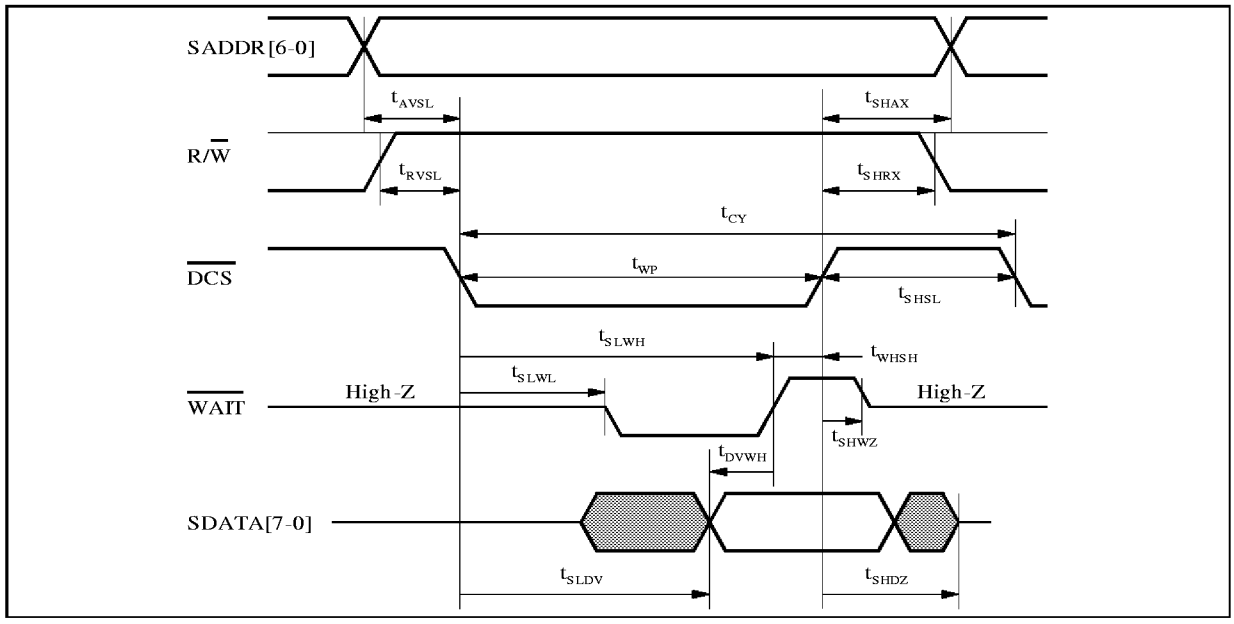
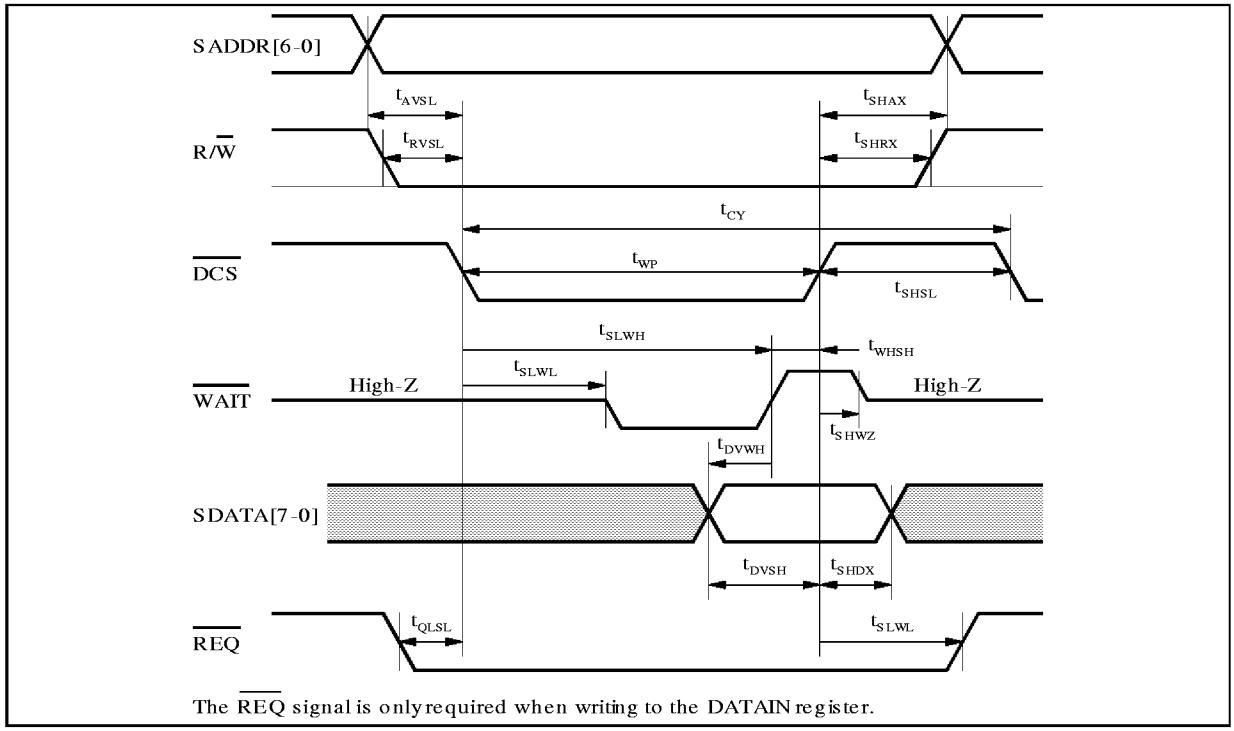


Figure 17 : Write Cycle Timing



XI - ELECTRICAL SPECIFICATION (continued)

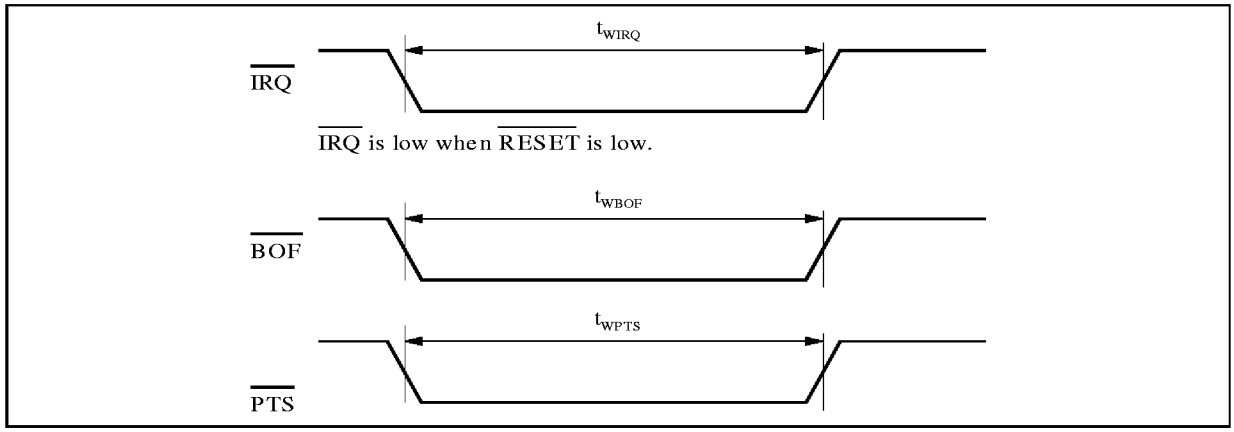
Register Read and Write Cycles

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{AVSL}	Address to $\overline{DCS}$ low set-up time	10			ns
t_{RVSL}	R/W to $\overline{DCS}$ low set-up time	10			ns
t_{SHAX}	Address from $\overline{DCS}$ high hold time	10			ns
t_{SHRX}	R/W from $\overline{DCS}$ high hold time	10			ns
t_{WP}	$\overline{DCS}$ pulse width	25			ns
t_{SHSL}	$\overline{DCS}$ high to low again	25			ns
t_{CY}	Read or write cycle time	100			ns
t_{SLWL}	$\overline{DCS}$ low to WAIT low			10	ns
t_{WHSH}	WAIT high to $\overline{DCS}$ high set-up time	10			ns
t_{SLWH}	$\overline{DCS}$ low to WAIT high (see Note 1)	15			ns
t_{SHWZ}	$\overline{DCS}$ high to WAIT disabled			30	ns
t_{DVWH}	Data valid before WAIT high	15			ns
t_{SHDZ}	$\overline{DCS}$ high to data off (hi-Z)			20	ns
t_{SLDV}	$\overline{DCS}$ low to data valid (see Note 1)			35	ns
t_{DVSH}	Data valid to $\overline{DCS}$ high set-up time	20			ns
t_{SHDX}	Data from $\overline{DCS}$ high hold time	20			ns
t_{QLSL}	$\overline{REQ}$ low to $\overline{DCS}$ low set-up time	25			ns
t_{SHQH}	$\overline{DCS}$ high to $\overline{REQ}$ high (see Note 2)	25			ns

Notes : 1. WAIT will remain low if PCM output is stopped and the buffers are full.
2. One more byte can be strobed in after REQ going high signals that the input buffer is full.

Interrupt Request

Figure 18 : Interrupt Request



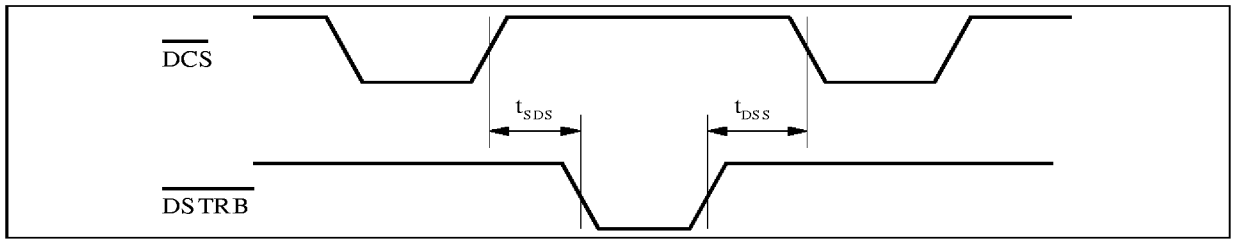
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WIRQ}	$\overline{IRQ}$ pulse width (see Note 1)	3.5 T			ns
t_{WBOF}	$\overline{BOF}$ pulse width	3.5 T			ns
t_{WPTS}	$\overline{PTS}$ pulse width	23.5 T			ns

Note 1 : IRQ pulse is generated when a bit becomes set in register INTR.

XI - ELECTRICAL SPECIFICATION (continued)

Relative Timing of DCS and DSTRB *(Note 1)*

Figure 19 : DCS, DSTRB Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SDS}	$\overline{DCS}$ high before $\overline{DSTRB}$ low	1 T			ns
t_{DSS}	$\overline{DSTRB}$ high before $\overline{DCS}$ low	1 T			ns

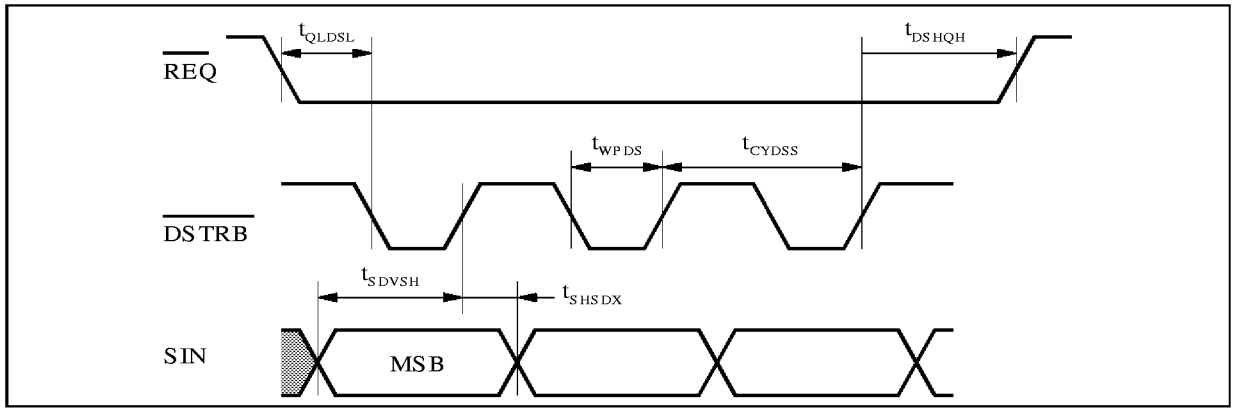
Note 1 : This constraint does not apply when compressed data in input serially (SIN_EN = 1) and no writes are made to DATAIN.

XI.3.4 - Compressed Data Input

(All timing measurements are made with respect to a threshold of 1.5V)

Bit-Serial Compressed Data Input *(Note 1)*

Figure 20 : Serial Port CD Input



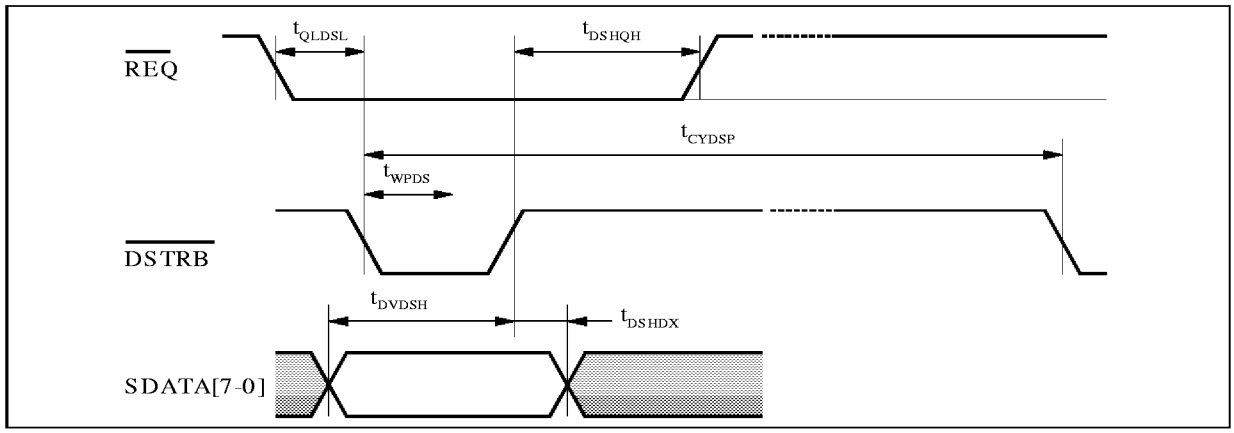
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{QLDSL}	$\overline{REQ}$ low to $\overline{DSTRB}$ low set-up time	25			ns
t_{DSHQH}	$\overline{DSTRB}$ high to $\overline{REQ}$ high (see Note 2)	20			ns
t_{WPDS}	$\overline{DSTRB}$ low time	20			ns
t_{CYDSS}	$\overline{DSTRB}$ cycle time (see Note 3)	50			ns
t_{SDVSH}	SIN set up time to $\overline{DSTRB}$ rising edge	20			ns
t_{SHSDX}	SIN hold time from $\overline{DSTRB}$ rising edge	20			ns

Notes : 1. Register bit SIN_EN must be set.
2. Two more bits can be strobed in after REQ going high signals that the input buffer is full.
3. This corresponds to a maximum input rate of 20 Mbit/s.

XI - ELECTRICAL SPECIFICATION (continued)

Byte-Parallel Compressed Data Input *(Note 1)*

Figure 21 : Byte-Parallel CD Input



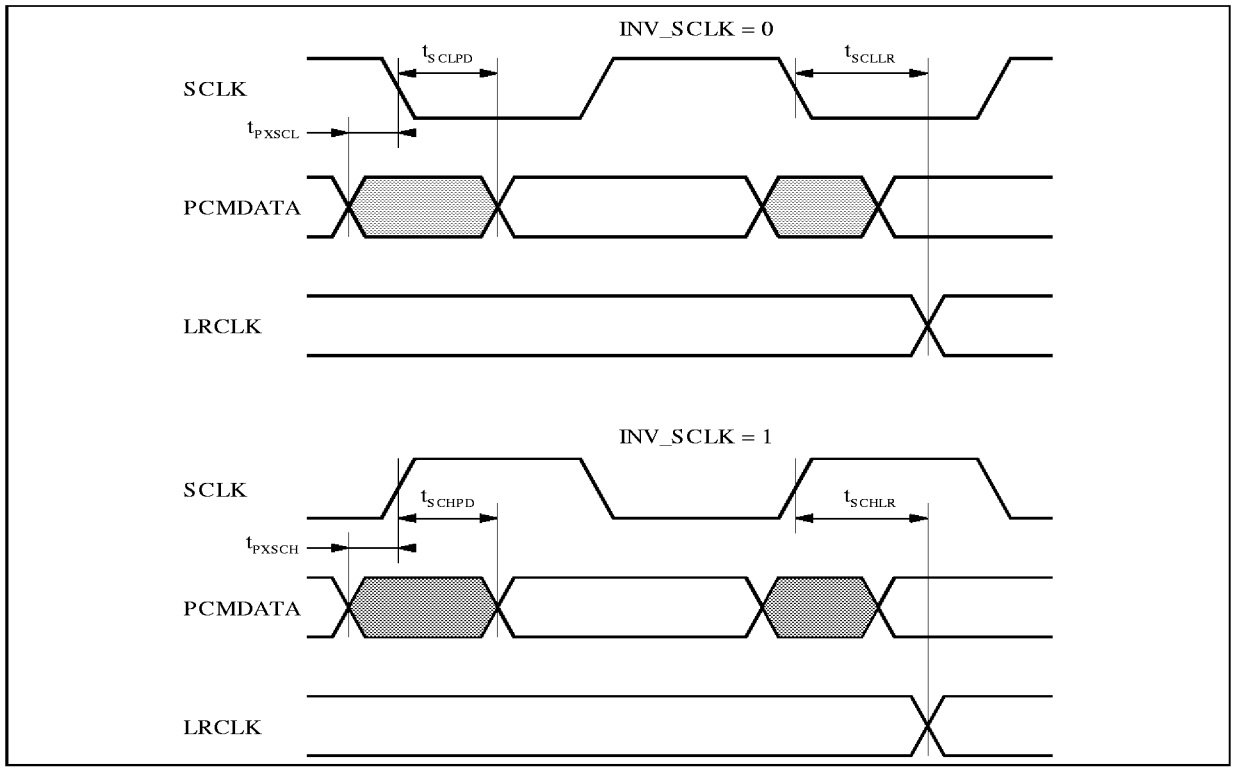
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{QLDSL}	$\overline{REQ}$ low to $\overline{DSTRB}$ low set-up time	25			ns
t_{DSHQH}	$\overline{DSTRB}$ high to $\overline{REQ}$ high (see Note 2)	20			ns
t_{WPDS}	$\overline{DSTRB}$ low time	20			ns
t_{CYDSP}	$\overline{DSTRB}$ cycle time (see Note 3)	400			ns
t_{DVDSH}	SDATA set up time to $\overline{DSTRB}$ rising edge	20			ns
t_{DSHDX}	SDATA hold time from $\overline{DSTRB}$ rising edge	20			ns

Notes : 1. Register bit SIN_EN must be set.
2. One more byte can be strobed in after REQ going high signals that the input buffer is full.
3. This corresponds to a maximum input rate of 2.5 Mbyte/s.

XI - ELECTRICAL SPECIFICATION (continued)

XI.3.5 - PCM Data Output (All timing measurements are made with respect to a threshold of 1.5V)

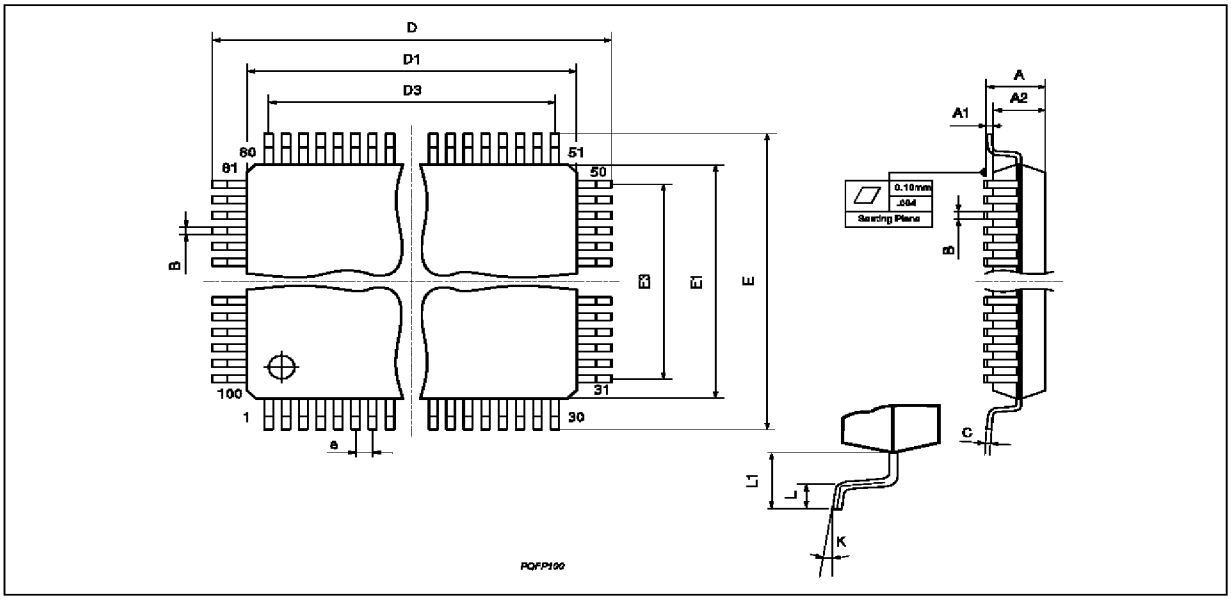
Figure 22 : PCM Data Output Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SCLPD}	SC low to PCMDATA valid			10	ns
t_{SCLLR}	SC low to LRCLK			25	ns
t_{SCHPD}	SC high to PCMDATA valid			10	ns
t_{PXSCL}	PCMDATA invalid to SC low			10	ns
t_{PXSCH}	PCMDATA invalid to SC high			10	ns
t_{SCHLR}	SC high to LRCLK			25	ns

PACKAGE MECHANICAL DATA

100 PINS - PLASTIC QUAD FLAT PACK (PQFP)



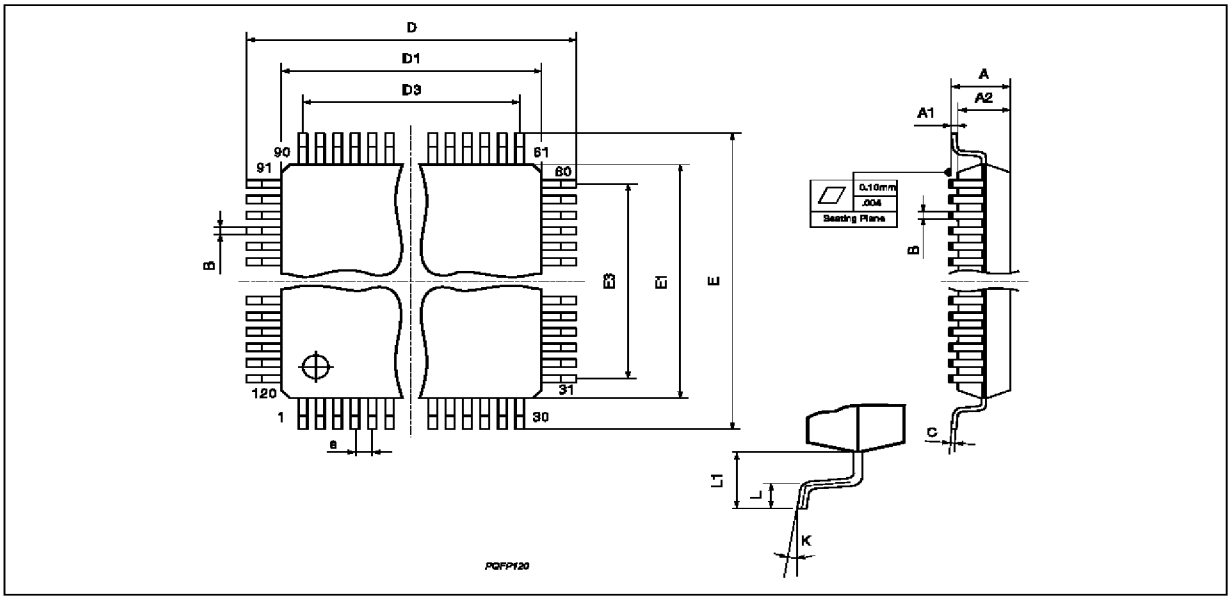
PMPQF100.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.22		0.38	0.0087		0.015
C	0.13		0.23	0.005		0.009
D	22.95	23.20	23.45	0.903	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
D3		18.85			0.742	
e		0.65			0.026	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.35			0.486	
L	0.65	0.80	0.95	0.026	0.0315	0.0374
L1		1.60			0.063	
K	0^o (Min.), 7^o (Max.)					

PQFP100.TBL

PACKAGE MECHANICAL DATA

120 PINS - PLASTIC QUAD FLAT PACK (PQFP)



PMPQF120.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			4.07			0.160
A1	0.25			0.010		
A2	3.17	3.42	3.67	0.125	0.135	0.145
B	0.30		0.45	0.012		0.018
C	0.13		0.23	0.005		0.009
D	30.95	31.20	31.45	1.218	1.228	1.238
D1	27.90	28.00	28.10	1.098	1.102	1.106
D3		23.20			0.913	
e		0.80			0.031	
E	30.95	31.20	31.45	1.218	1.228	1.238
E1	27.90	28.00	28.10	1.098	1.102	1.106
E3		23.20			0.913	
L	0.65	0.80	0.95	0.026	0.0315	0.0374
L1		1.60			0.063	
K	0^o (Min.), 7^o (Max.)					

PQFP120.TBL