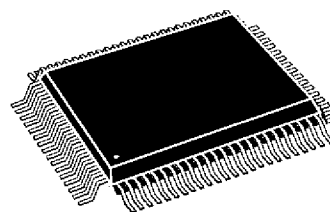


6 CHANNEL DOLBY AC-3 MPEG1/2 AUDIO DECODER

ADVANCE DATA

- Single Chip Dolby* Class A AC-3 Decoder
- Decodes 5.1 Dolby AC-3 Digital Surround
- Output to 6 Channels. Downmix Modes: 1, 2, 3 or 4 Channels
- Karaoke Aware Mode for DVD
- MPEG2 Audio Decoder: Layers I and II, Data Rates up to 448 Kbit/s
- PCM: transparent, downsampling 96 to 48KHz
- Accepts MPEG-2 PES Stream Format for: MPEG-2, MPEG-1, Dolby AC-3 and Linear PCM
- Bitstream Input Interface: Serial or Parallel
- IEC-958 Output Interface
- Pro Logic Decoder
- Down Mix for Dolby Pro Logic Compatible Outputs
- PLL for Internal 44.1 and 48KHz PCM Clock Generation
- On Chip Pink Noise Generator
- PTS Handling Control On Chip
- No External DRAM
- I C or Parallel Control Bus
- 27MHz Master Clock
- 80 Pin PQFP Package
- 3.3V Power Supply, I/Os 5V Compatible, 0.5µm CMOS Technology



PQFP80
(Plastic Package)

ORDER CODE: STi4600ACV

APPLICATIONS

- DVD Consumer Players
- Multimedia PC
- Set Top Box
- HDTV
- High End Audio Equipment

* "Dolby", AC-3" and "Pro Logic" are trademarks of Dolby Laboratories

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1 INTRODUCTION

1.1 DESCRIPTION

The STi4600 is a fully integrated Class A Dolby AC-3 decoder capable of decoding both 5.1 and 2 Channels compatible with the DVD standard. The device also decodes both MPEG1 and MPEG2 layers I and II Audio.

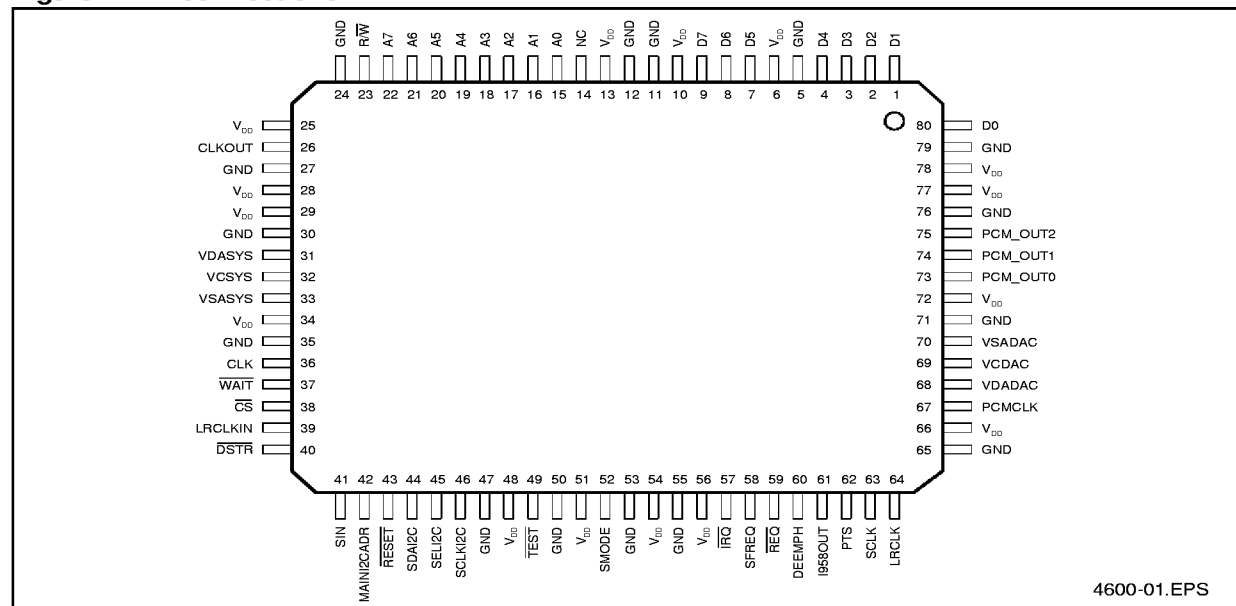
The device accepts a MPEG-2 PES stream, input data can be entered either by a serial or parallel interface. The control interface can be either I C or a parallel 8-bit interface. No external DRAM is necessary for a total of 35ms surround delays.

1.2 PIN OUT DESCRIPTION

Pin Number	Name	Type	Function
CONTROL INTERFACES			
57	IRQ	O	Interrupt Signal (level)
45	SELIC2C	I	Select the Control Interface
(parallel or serial_ I C			
I C Control Interface			
44	SDAI2C	I/O	I C Serial Data
46	SCLKI2C	I	I C Clock
42	MAINI2CADDR	I	Determine the slave address
Parallel Control Interface			
80 - 1 - 2 - 3	D0 - D1 - D2 - D3	I/O	Host Data
4 - 7 - 8 - 9	D4 - D5 - D6 - D7		
15 - 16 - 17 - 18	A0 - A1 - A2 - A3	I	Host Address
19 - 20 - 21 - 22	A4 - A5 - A6 - A7		
38	CS	I	Chip Select
23	R/W	I	Read/ Write Selection
37	WAIT	O	Data Acknowledge
DATA INPUT INTERFACES			
Serial Data Interface			
40	DSTR	I	Clock Input Data
41	SIN	I	Serial Input Data
39	LRCLKIN	I	Word Clock for the Input
59	REQ	O	Handshake for the Data Transfer
DATA OUTPUT INTERFACES			
67	PCMCLK	I/O	Clock Input or PLL Output
DAC Interface			
63	SCLK	O	Bit Clock for the DAC
64	LRCLK	O	Word Clock for the DAC
73	PCM_OUT0	O	Data for the first DAC (Left/Right)
74	PCM_OUT1	O	Data for the second DAC (Centre/Sub)
75	PCM_OUT2	O	Data for the third DAC (L _S /R _{S1})
IEC958 Interface (S/PDIF)			
61	I958OUT	O	S/PDIF Signal

INTRODUCTION (Cont'd)**PIN OUT DESCRIPTION (continued)**

Pin Number	Name	Type	Function
STATUS INFORMATION			
PCM Related Information			
58	SFREQ	O	sf= 48KHz when 0/ sf= 44. 1 when 1
60	DEEMPH	O	Deemphasis
Audio Video Synchronization			
62	PTS	O	To signal a PTS
Other Signals			
36	CLK	I	Master Clock Input Signal (27MHz)
43	RESET	I	Reset Signal Input
49	TEST	I	Test: Connect to VDD
52	SMODE	I	Test: Connect to GND
PLL INTERFACES			
26	CLKOUT	O	
68	VDADAC	VDD	Analog DAC PLL Supply Voltage
69	VCDAC		DAC PLL Filter
70	VSADAC	GND	Analog DAC PLL Ground
31	VDASYS	VDD	Analog System Supply
32	VCSYS		Filter System
33	VSASYS	GND	Analog System Ground
5 - 11 - 12 - 24 - 27 - 30 - 35 - 47	GND	GND	Ground
50 - 53 - 55 - 65 - 71 - 76 - 79			
6 - 10 - 13 - 25 - 28 - 29 - 34 - 48	VDD	VDD	Power Supply
51 - 54 - 56 - 66 - 72 - 77 - 78			
14	NC	NC	Reserved Pin, tie to ground

Figure 1. Pin connections

2 GENERAL DESCRIPTION

The device has 3 operating modes:

- AC-3 bitstream decoding 1 to 6 channel PCM outputs,
- MPEG1 Layers I and II decoding to 2 PCM channel outputs or MPEG2 layers I and II multichannel decoding,
- PCM modes for CD backwards compatibility, SD PCM data processing,

A Pro Logic decoder for 4 channel surround PCM output is available in each of the above three operating modes; it can be used for surround encoded digital bitstreams and in PCM mode.

Additional Features

- Controllable delays for centre and surround in programmable steps (e.g. for 48KHz, 0.3ms steps).
- Five choices for low frequency redirection output configurations.
- A pink noise generator for optimal surround sound set up.
- A Digital IEC-958 output interface to be used for PCM or encoded bitstream data.
- Selectable serial or parallel data control inputs.
- Processing of many packetised or non-packetised input formats.
- The device has a sample rate converter on chip which enables 96KHz to 48kHz downsampling.

Control Interface

The device has 2 control interfaces:

- I C interface operating at 400kHz,
- 8-bit interface with "Wait" signal handshake and interrupt request signal.

Data Input Interface

There are three possible ways of inputting compressed data, shown in the Table below.

	Serial Input	Parallel Input
Strobed by DSTR	DMA Mode	DMA Mode
Strobed by CS		write to DATAIN

The compressed bitstream can be input in parallel or serial mode depending upon the value of the relevant register.

If serial mode is selected, data is placed on Pin SIN, and strobed in on the rising edge of signal DSTR. If the signal REQ is asserted, then 16 more data bits can be input. REQ is deasserted when the input buffer is full. REQ polarity is programmable.

If Parallel mode is selected, data can be input using DSTR as described above, or by writing to the DATAIN register using CS. If the signal REQ is asserted, then two more bytes can be input.

Output Interface

The STi4600 has 2 output interfaces:

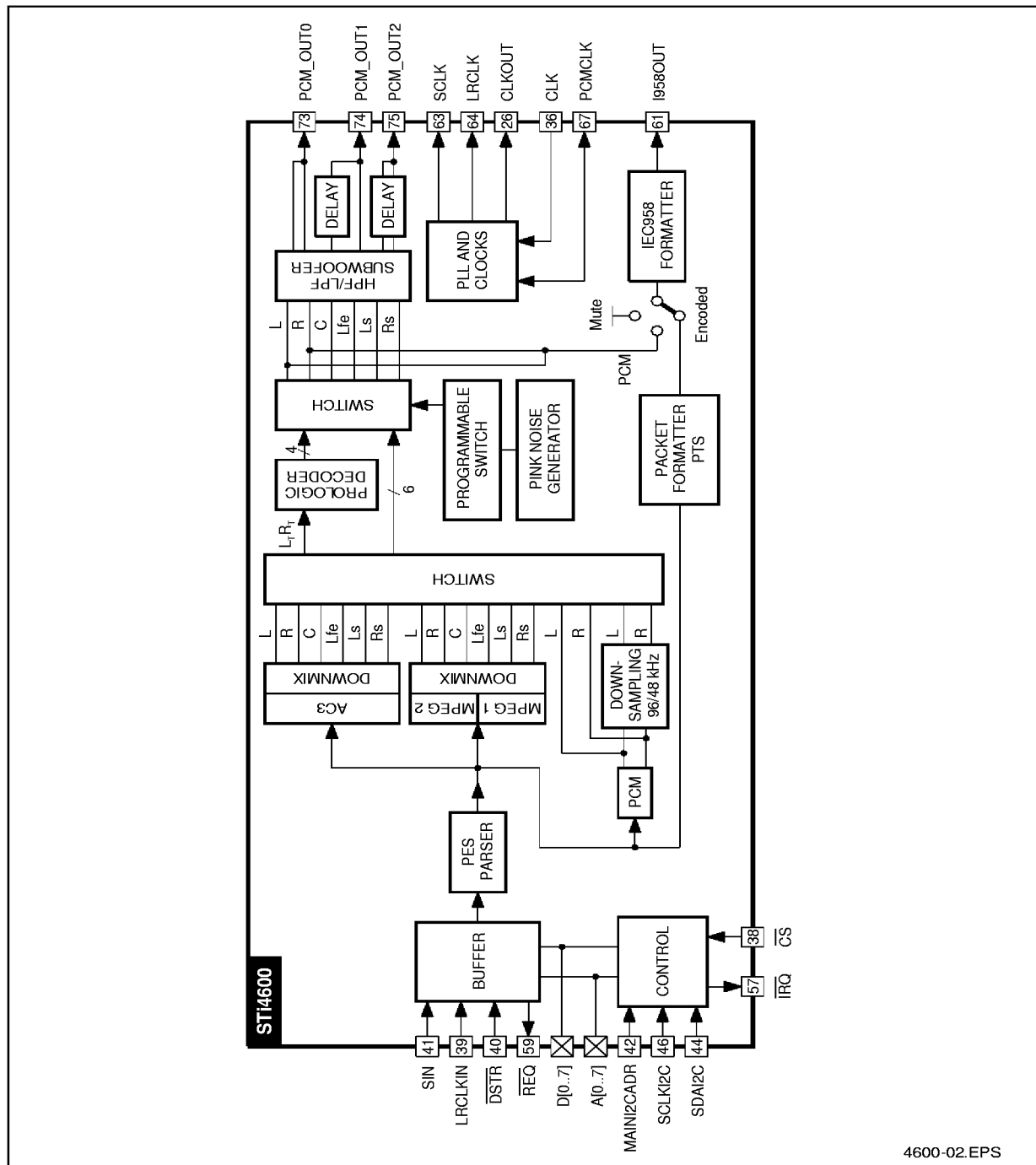
- Digital IEC958 Fully IEC958 formatted, single ended CMOS/TTL output for:
Encoded bitstreams according to Dolby proposal for AC-3 and MPEG Audio with time stamps,
linear PCM output (left and right channels, 16, 18, 20 & 24 bits), Zero output (Mute mode)
- PCM Audio output

Format of Input Data

- Packetized Input Data
 - MPEG1 system streams carrying MPEG1 Audio
 - MPEG2 PES streams for DVD
 - MPEG2 PES streams
- Non-Packetized Input Data
 - AC-3 elementary streams
 - MPEG1 and MPEG2 Audio elementary streams (with or without extensions)
 - Stereo PCM data from an ADC

GENERAL DESCRIPTION(Cont'd)

Figure 2. Audio Decoder Top Level Functional Diagram



3 INTERNAL CIRCUIT DESCRIPTION

3.1 ARCHITECTURE

The STi4600 is based on a programmable core optimized for audio decoding algorithms. Dedicated hardware has been added to perform specific operations such as bitstream depacking or IEC data formatting.

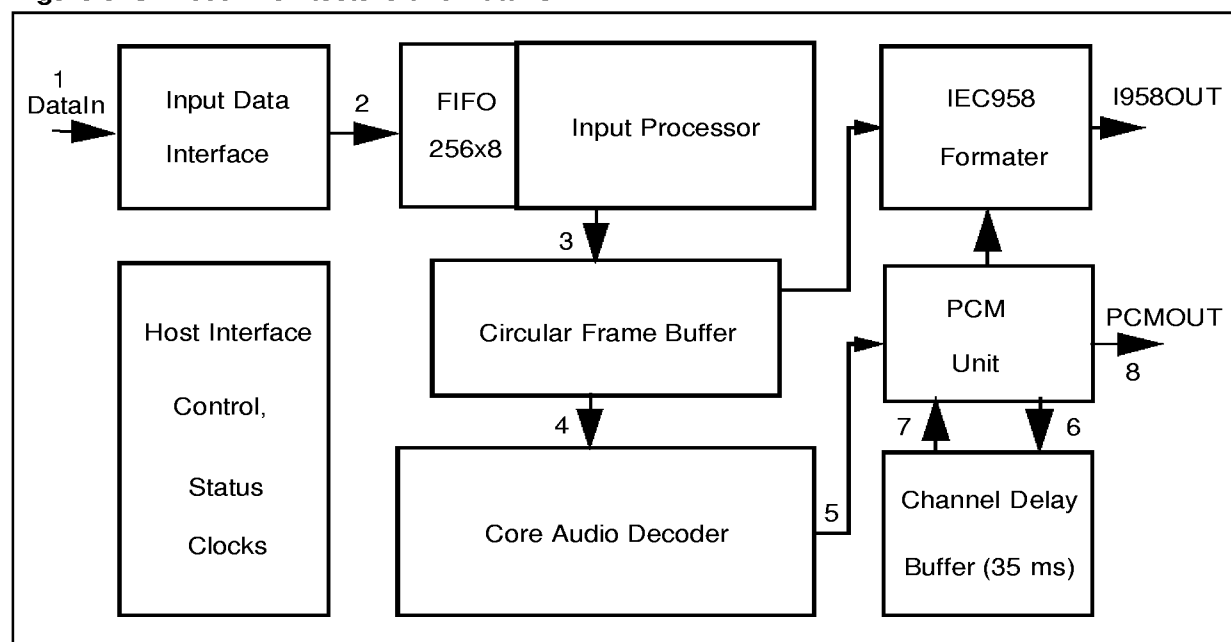
The arrows in Figure 3 indicate the data flow within the chip. The compressed bitstream is input via the input interface. Data is transferred on a byte basis to the FIFO. This FIFO allows burst input data up to 33Mbit/s. The input processor depacks the bitstream (Packet level). The compressed audio frames with their associated information (PTS) are stored into the circular frame buffer before the audio core decoder extracts and decodes them.

The samples are the output of the core audio decoder.

The PCM unit converts the samples to the PCM format. The PCM unit controls the channel delay buffer in order to delay each channel independently.

The IEC unit transmits non compressed data or compressed data. In the compressed mode the data is extracted from the circular buffer and formatted according to the IEC1937 standard. In non compressed modes the left and right PCM channels are output by the IEC unit.

Figure 3. STi4600 Architecture and Dataflow



INTERNAL CIRCUIT DESCRIPTION(Cont'd)**3.2 PLL SETUP**

There are two embedded PLLs in the STi4600: the system PLL and the PCM PLL. Both are used to generate clocks from the 27 MHz clock input.

3.2.1 System PLL

The system PLL is used to create the system clock from the 27 MHz input clock. This PLL is software programmable. A register is used to set the frequency between 1.5 MHz up to 33 MHz in steps of 1.5 MHz. After hard reset the system clock is running at 33 MHz. An RC must be connected to the filter pin VCSYS, recommended values are 1.5 Kohms / 1nf.

3.2.2 DAC PLL

This PLL is used to generate the clock for the digital to analog converter. The use of this PLL is optional. After Hard reset this PLL is disabled and the pin PCMCLK is an input of the device.

To activate this PLL an internal register must be set. In this case the pin PCMCLK becomes an output. The output clock frequency can be 384x44.1KHz or 384x48 KHz, the choice is done via a host register. An RC must be connected to the filter pin VCDAC, recommended values are 10 Kohms / 2.2nf.

INTERNAL CIRCUIT DESCRIPTION(Cont'd)

3.3 DECODING PROCESS

The decoding process in the STi4600 is done in several stages :

- Parsing
- Main decoding
- Post decoding
- Bass redirection

Each of the stages can be activated or bypassed according to the configuration registers.

Parsing:

The bitstream parsing is in charge of discarding all the non audio information in order to transmit to the next stage only the audio elementary stream (AC3, MPEG1/2, LPCM, PCM). The parsing stage checks also the syntax of the bitstream. Two kinds of checks are done : checksum calculation and detection of expected synchronization word. The checksum is done for AC3 frame and MPEG-2 extension part. When an error occurs the bitstream is discarded, and the parser tries to recover synchronization. This leads to skip the erroneous frame at the output stage.

Main decoding:

The input of this stage is an elementary stream, the outputs are decoded samples. The number of output channels is defined by the downmix register (1 up to 6). The decoding formats currently supported are AC3 , MPEG1 , MPEGII, LPCM.

Post decoding:

The post decoding includes specific PCM processing : DC filter , deemphasis filter, Downsampling filter and also a Pro Logic decoder.

Bass redirection:

This stage redirects the low frequency signals to the subwoofer and controls the volume of each channel. The low frequencies are extracted from the other channels (L,R,C,Ls,Rs,LFE).

3.3.1 Decoding States

There are three different decoder states: **Idle**, **Init** and **decode** (see Figure 4). Commands to change the decoding states are described in Section 5.4.7 (eg. RUN, MUTE, PLAY).

Idle mode

In this mode the decoder is waiting for the RUN command. This mode should be used to initialise the configuration registers of the device. The DAC connected to the device can be initialized during this mode (set mute to 1).

Play	Mute	Clock state	PCM Output
X	0	Not running	0
X	1	Running	0

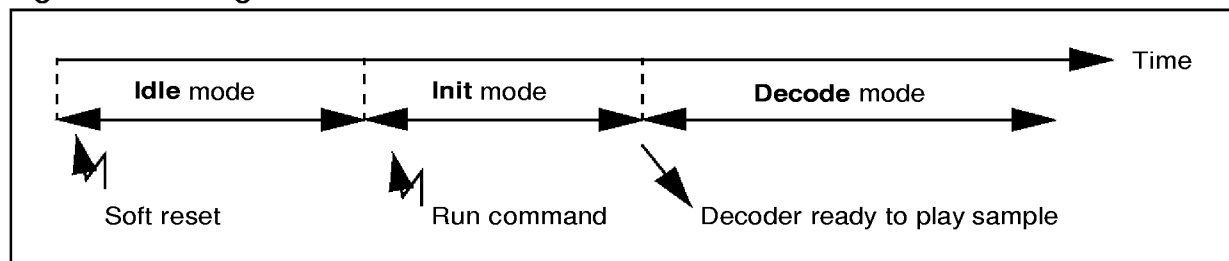
Init mode

“Play” and “Mute” changes are ignored in this mode. The internal state of play and mute will be updated only when the decoder changes from the state “init” to “decode”. The “init” phase ends when the first decoded samples are at the output stage of the device.

Decode mode

Play	Mute	Clock state	Pcm Output	Decoding
0	0	Not running	0	No
0	1	Running	0	No
1	0	Running	Decoded samples	Yes
1	1	Running	0	Yes

Figure 4. Decoding States



INTERNAL CIRCUIT DESCRIPTION(Cont'd)

3.4 INTERFACE DESCRIPTION

3.4.1 Data Serial interface

When serial mode is selected the STi4600 uses a four signal data interface (see Figures 12 and 13) that provides an input data line **SIN**, an input CLK **DSTR**, a word clock input **LRCLKIN** and a handshake output signal **REQ**. The register **CAN_SETUP** is used to configure this serial interface, see Register Manual.

3.4.1.1 Modes without LRCLKIN

In this mode the signal LRCLKIN is not used by the STi4600. The input data **SIN** is sampled on the rising edge of **DSTR**. When the STi4600 input buffer is full the **REQ** signal is asserted.

The polarity of **REQ** signal is programmable. The data must be sent most significant bits first.

When the decoder cannot accept further data the **REQ** is deasserted, the **DSTR** clock must be stopped as soon as possible to avoid data loss. After the **REQ** is deasserted, the decoder is still able to accept data for a limited number of clock cycles. The maximum number of data that can be transmitted with respect to the change of **REQ** is given by the following formula:

$N_{bits} = 23 - 6 * FDSTRB/33MHz$, Maximum value is 23 bits, Minimum value is 17 bits.

Where:

FDSTR: **DSTR** clock frequency, (max is 33 MHz)

The polarity of **REQ** signal is programmable. In the above example it is active low. The **REQ** is deasserted (went high on figure) asynchronously from **DSTR**. See Figure 13 for timing details.

3.4.1.2 LRCLKIN modes

These modes are used mainly for non compressed data (But they can be used also for compressed data). The LRCLKIN signal is used to make the distinction between the left and right channel. In these modes any edge of the LRCLKIN signal indicates a word boundary. The data transfer between the input interface and the FIFO is done on a byte basis. After the edge (rising or falling) of the LRCLKIN, a new byte is transferred to the first stage of the STi4600 every 8 **DSTR** clock cycles. If the number of time slots is not a multiple of 8, the remaining data is lost. The polarity of LRCLKIN and **DSTR** are programmable. The LRCLKIN can be delayed by one time slot, in order to support PCM delayed mode.

The register **CAN_SETUP** is a 4 bit register. Each bit has specific meaning, see Table 1 and Register Manual.

Table 1. CAN_SETUP Mapping

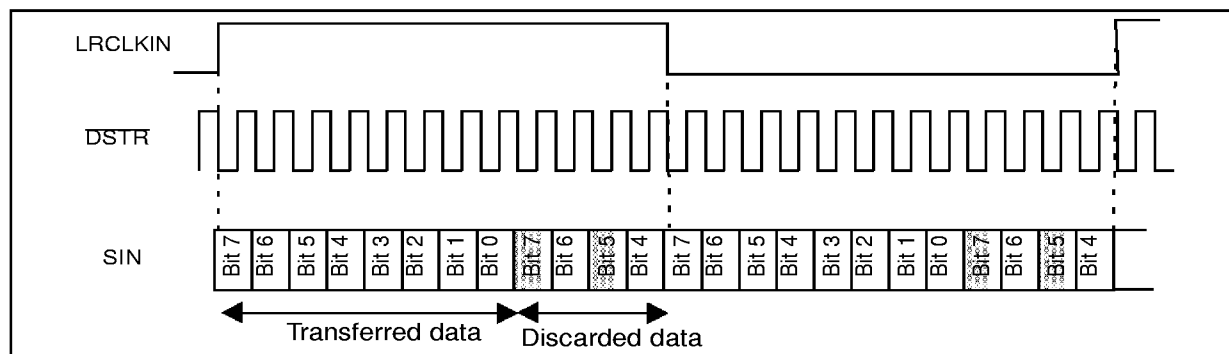
	When Set	When Clear	Name
bit[0]	The input data is one slot delayed with respect to LRCLKIN	The input data is not delayed	DelayMode 1
bit[1]	First channel when LRCLKIN is set	First channel when LRCLKIN is clear	RightFirstChannel 2
bit[2]	Data are sampled on falling strobe	Data are sampled on rising strobe	FallingStrobe 4
bit[3]	Only the first 16 data bits are extracted	All the bytes are extracted	AllSlot 8

INTERNAL CIRCUIT DESCRIPTION(Cont'd)

Example 1:

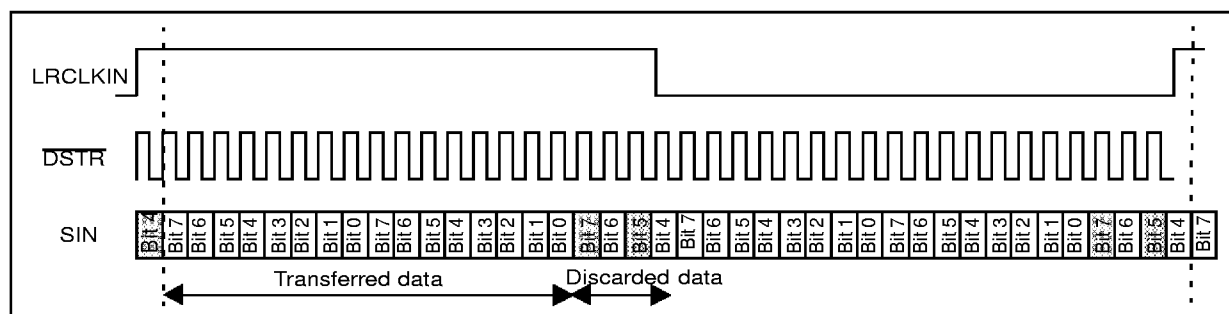
Only the first byte is transferred to the STi4600 because the number of time slots is 12 (8+4). SIN and LRCLKIN are sampled on the falling edge of

DSTR. In this case $SIN_SETUP=3$ and $CAN_SETUP=LeftFirstChannel + FallingStrobe + AllSlot = 2 + 4 + 8 = 14$.

**Example 2:**

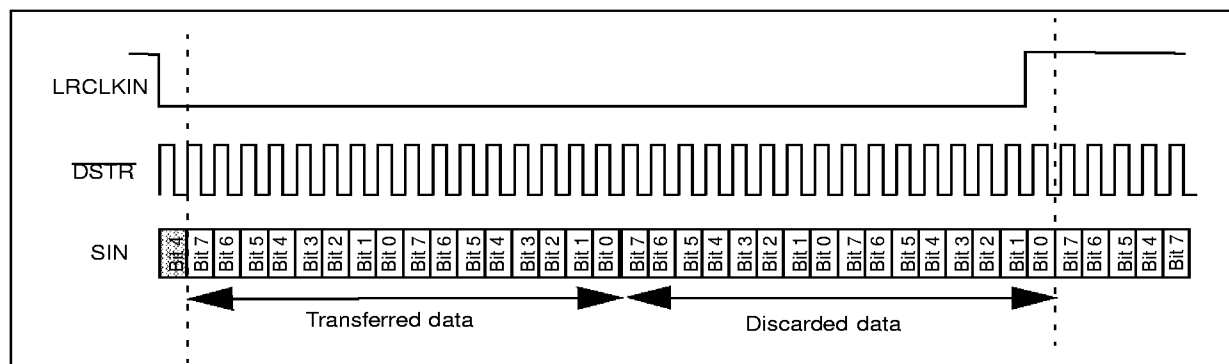
Only the first 2 bytes are transferred to the STi4600 because the number of slots is 20(16+4). SIN and LRCLKIN are sampled on the falling edge of

DSTR. The data is in delayed mode. The register configuration is $SIN_SETUP=3$ and $CAN_SETUP=DelayMode+ RightFirstChannel + FallingStrobe + AllSlot = 1 + 2 + 4 + 8 = 15$.

**Example 3:**

This mode is a specific mode where only the first 16 data bits are transferred. The remaining bits are

discarded. The register configuration is $SIN_SETUP=3$ and $CAN_SETUP=DelayMode+ FallingStrobe = 1+4=5$.



INTERNAL CIRCUIT DESCRIPTION(Cont'd)

3.4.2 Data Parallel interface

In this mode the data must be presented on the 8 bit parallel host data bus. On the rising clock of **DSTR** the data byte is sampled by the STi4600. The signal **REQ** is used to signal when the input FIFO is full. When **REQ** is deasserted the transfer must be stopped to avoid to data loss.

The host data bus is shared between the Parallel Control interface and the Data Parallel interface. To avoid conflict the **DSTR** signal and the **CS** signal must respect certain timing constraints. The timing diagram for the data parallel interface is given in Figure 14.

The IC can also be controlled by a host using an I C interface or a general purpose host interface. These interfaces provide the same functions and are described in the following sections.

3.4.3 Parallel control interface

The address bus A[7:0] is used to select one of the 128 register locations. (A[7] is not used in the current implementation of the devices, it can be stuck to GND). Some registers are Read/Write, and some write only. The signal $\overline{RW}$ defines whether the register access is a read or a write (high for read, low for write).

A cycle is defined by the assertion of signal **CS**. In response to this signal the signal **WAIT** is always asserted. The address, read/write must be setup before the **CS** line is activated. If a read cycle is requested the data lines D[7:0] will be driven by the IC. For a write cycle the STi4600 will latch the data placed on the data lines on the rising edge **CS**. The timing diagrams for the parallel control interface are given in Figures 15 and 16.

3.4.4 I C control interface

3.4.4.1 Introduction :

The I C unit works at up to 400 KHz in slave mode with 7 bit addressing. The pin MAINI2CADDR selects the device address. When MAINI2CADDR is high the address is 0x5C, when low the device address is equal to the value on the Data bus.

The I C-BUS standard does not specify sub-addressing. There are thus potentially multiple ways to implement it. Any implementation that respects the standard is of course legal but a particular implementation is used by many companies. The following paragraphs describe this implementation.

3.4.4.2 Protocol Description :

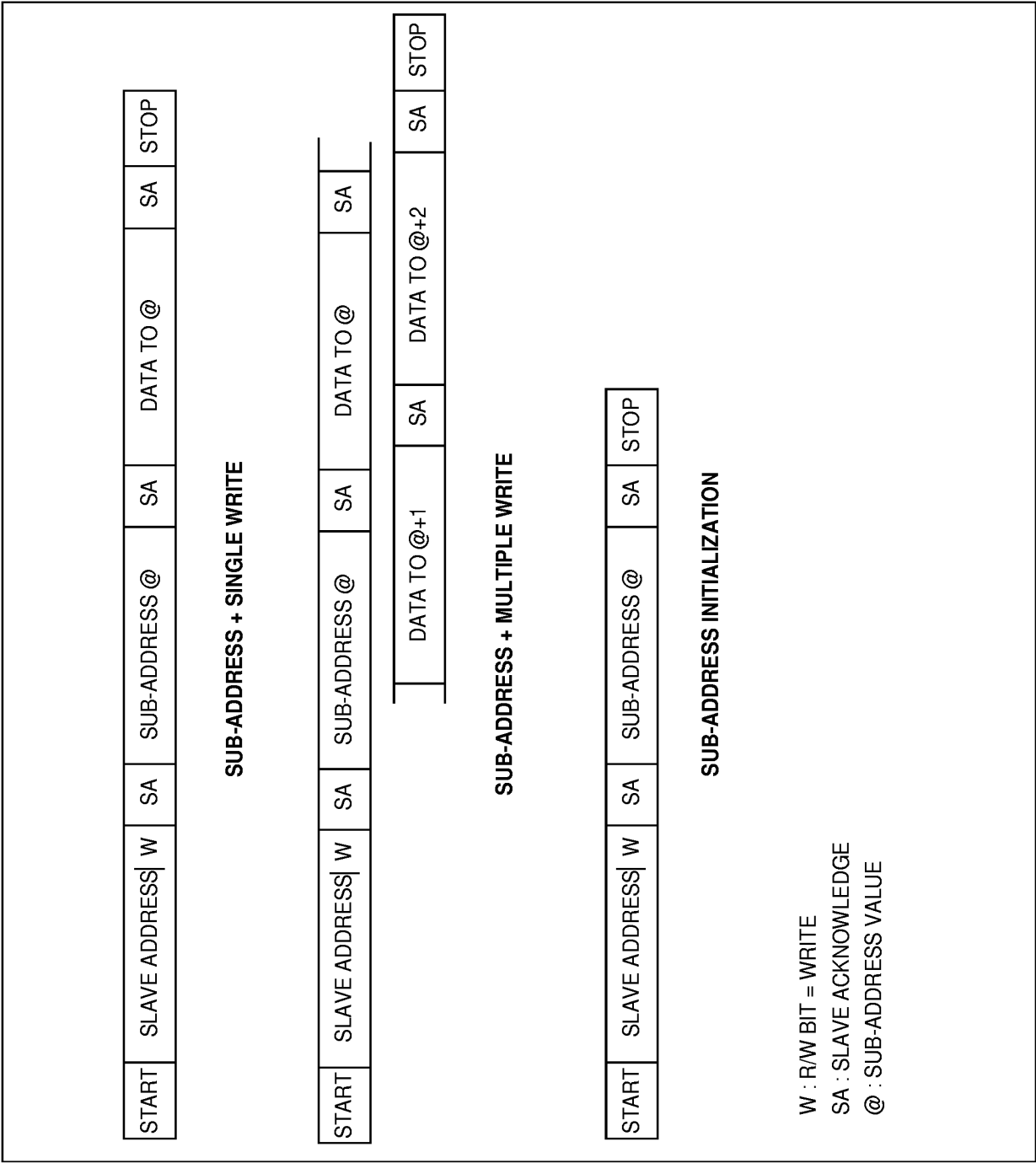
For write accesses *only*, the *first data* which follows the slave address is *always* the sub-address. This is *the one and only way* to declare the sub-address. It should be noticed that the sub-address is implemented as a standard data on the I C-BUS protocol point of view. It is a sub-address because the slave knows that it must load its address pointer with the first data sent by the master.

Included : I C-BUS message format examples :

- sub-address initialization
- sub-address + single write
- sub-address + multiple write
- single read (from the current address)
- multiple read (starts from the current address)
- sub-address + single read (combined message)
- sub-address + multiple read (combined message)

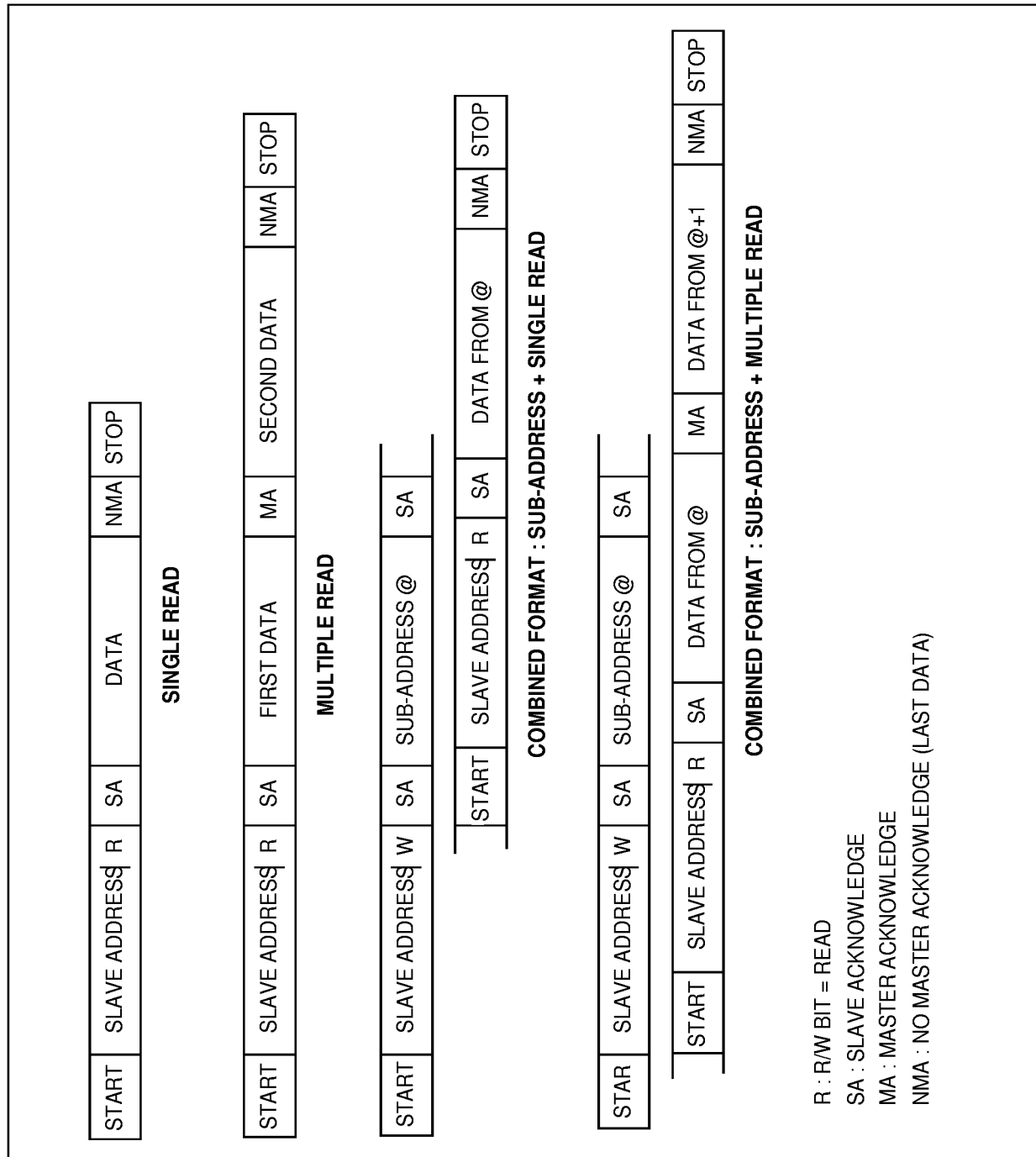
INTERNAL CIRCUIT DESCRIPTION(Cont'd)

Figure 5. I C Message Formats



INTERNAL CIRCUIT DESCRIPTION(Cont'd)

Figure 6. I C Message Formats (Cont'd)



INTERNAL CIRCUIT DESCRIPTION(Cont'd)**3.4.5 PCM OUTPUT****3.4.5.1 Interface and Output Formats**

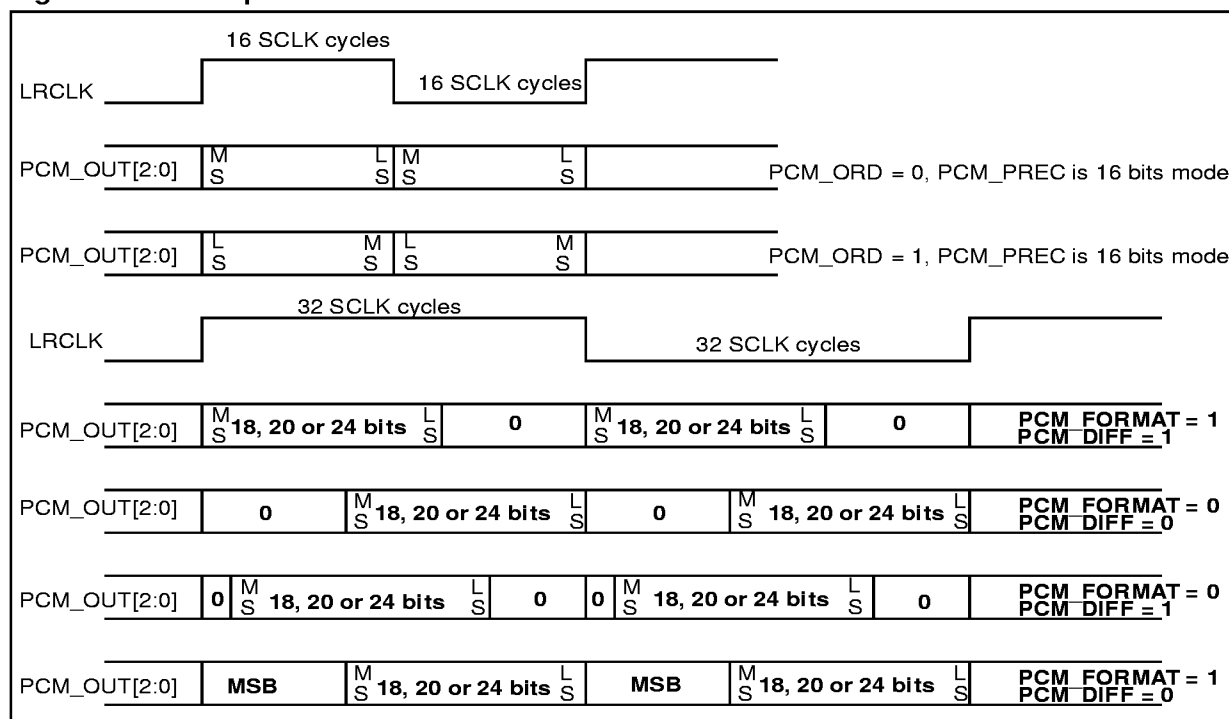
The decoded audio data are output in serial PCM format. The interface consists of the following signals :

PCM_OUT0,	
PCM_OUT1,	PCM serial data outputs
PCM_OUT2 :	
SCLK	PCM clock output
LRCLK	Left/Right channel select output
PCMCLK	PCM clock input

Output precision is selectable from 16 bits/word to 24 bits/word by setting the output precision select,

PCMCONF (16, 18, 20 and 24 bits mode), register; see Section 5.4.3. In 16 bits mode, data may be output either with the most significant bit first or least significant bit first selected by the contents of the output order select, PCMCONF.ORD. When PCMCONF.PREC > 16 bits, 32 bits are output for each channel. The data in front register, PCMCONF.DIF, is used to position the 18, 20 or 24 bits either at the beginning or at the end of each 32-bit frame. PCMCONF.FOR is used to select standard or I2S-compatible format when PCM.CONF.PREC > 16 bits is configured.

Figure 7 and Table 2 show the different output formats which are possible.

Figure 7. PCM Output Formats

INTERNAL CIRCUIT DESCRIPTION(Cont'd)

Table 2. Data Alignments vs. PCM_PREC, PCM_ORD, format and dif

PCM_prec	PCM_ord	format	dif	data in sample memory data[23:0]	data sent on the PCM serial output (left bit first)
0 : 16-bit mode	1	Na	Na	{d23-d8}{8*0}	{d8-d23} : 16 bits
0 : 16-bit mode	0	Na	Na	{d23-d8}{8*0}	{d23-d8} : 16 bits
1 : 18-bit mode	Na	0	0	{d23-d6}{6*0}	{13*0}{0}{d23-d6} : 32 bits
1 : 18-bit mode	Na	0	1	{d23-d6}{6*0}	{0}{d23-d6}{13*0} : 32 bits
1 : 18-bit mode	Na	1	0	{d23-d6}{6*0}	{14*d23}{d23-d6} : 32 bits
1 : 18bit mode	Na	1	1	{d23-d6}{6*0}	{d23-d6}{14*0} : 32 bits
2 : 20-bit mode	Na	0	0	{d23-d4}{4*0}	{11*0}{0}{d23-d4} : 32 bits
2 : 20-bit mode	Na	0	1	{d23-d4}{4*0}	{0}{d23-d4}{11*0} : 32 bits
2 : 20-bit mode	Na	1	0	{d23-d4}{4*0}	{12*d23}{d23-d4} : 32 bits
2 : 20-bit mode	Na	1	1	{d23-d4}{4*0}	{d23-d4}{12*0} : 32 bits
3 : 24-bit mode	Na	0	0	{d23-d0}	{6*0}{0}{d23-d0} : 32 bits
3 : 24-bit mode	Na	0	1	{d23-d0}	{0}{d23-d0}{7*0} : 32 bits
3 : 24-bit mode	Na	1	0	{d23-d0}	{8*d23}{d23-d0} : 32 bits
3 : 24-bit mode	Na	1	1	{d23-d0}	{d23-d0}{8*0} : 32 bits

Notations :

{5*0} means {00000} and {4*d12} represents the following binary word {d12,d12,d12,d12}

PCM_DIF = 1, PCM_FORMAT = 0 is compatible with I2S format.

The polarity of the PCM serial output clock, SCLK and LRCLK are selected by the INV_SCLK and INV_LRCLK registers, respectively.

Figure 8 shows the two polarities of SCLK. Normally, the DAC will sample LRCLK and the PCM-DATA on the rising edge of SCLK in the first case, and on the falling edge of SCLK in the second. The first option (INV_SCLK=0) is the one normally used in I2S systems.

Figure 9 shows how the polarity of LRCLK is selected. The second option (INV_LRCLK=1) is compatible with the I2S format. See Section 4.4.5 for data output timing.

Figure 8. SCLK polarity

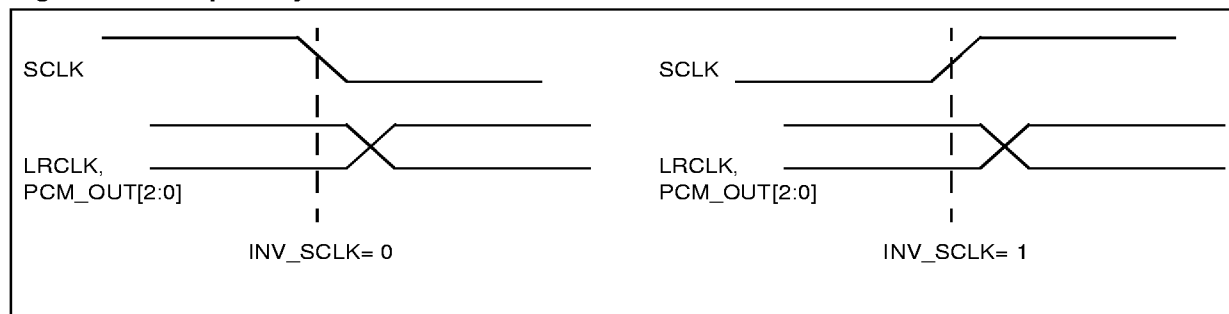
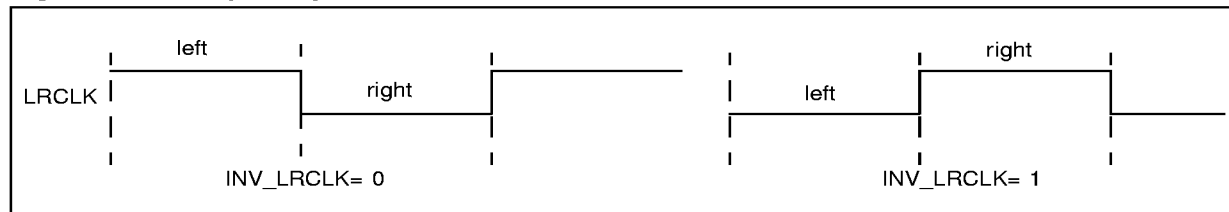


Figure 9. LRCLK polarity



INTERNAL CIRCUIT DESCRIPTION(Cont'd)**3.4.5.2 PCM Clock Generation**

The PCM serial clock SCLK is derived from the clock input PCMCLK. The frequency of PCMCLK may be equal to the PCM output bit rate, or it may be an integer multiple of this, allowing the use of oversampling D-A converters.

SCLK is derived from PCMCLK by dividing it by the contents of the divider register, PCM_DIV. This number defines the ratio of the frequency of the PCM bit clock, SCLK, to that of PCMCLK, according to the relationship:

$$F_{sclk} = F_{PCMCLK} / (2 \times (PCM_DIV + 1))$$

The value of PCM_DIV=0 is reserved. If this number is loaded, the divider is bypassed and the frequency of SCLK is equal to the frequency of PCMCLK.

The PCM_DIV register must be set up before the output of SCLK starts. This can be done by first disabling PCM outputs, by de-asserting the MUTE and PLAY commands and then writing into the PCM_DIV register. Once the register is setup, the MUTE and/or PLAY commands can be asserted. PCM_DIV can not be changed "on the fly".

The frequency of LRCLK is given by:

$$F_{lrclk} = F_{sclk} / 32 ; \text{ for 16 bit PCM output}$$

$$F_{lrclk} = F_{sclk} / 64 ; \text{ for 18, 20 or 24 bits PCM output.}$$

3.4.6 IEC output interface

The IEC output pad is a TTL output pad with slew rate control. The output DC capability is 4 mA. The voltage drop is 3V. This output must be connected to a TTL driver before the transformer.

4 ELECTRICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to

those conditions specified in section 4.2 DC ELECTRICAL CHARACTERISTICS.

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply	-0.5, 6	V
V_I, V_O	Voltages on Input and Output Pins	- 0.5, 5.25	V
T_{STG}	Storage Temperature	-65, +150	°C
T_{OPER}	Ambient Operating Temperature	0, +70	°C

4.2 DC ELECTRICAL CHARACTERISTICS

Operating conditions: $V_{DD} = 3.3V \pm 0.3V$, $T_{amb} = 0$ to 70°C unless otherwise specified

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
I_{DD}	Average Power Supply Current	$C_{LOAD} = 50\text{pF}$ on all outputs $f_{primary} = 27\text{MHz}$, all inputs at V_{DD} or $0V$		220	250	mA
V_{IL}	Input Logic Low Voltage	Except CLK	-0.3		+0.8	V
V_{IL}	Input Logic Low Voltage	CLK			+0.6	V
V_{IH}	Input Logic High Voltage	Except CLK	2.0		5.25	V
V_{IH}	Input Logic High Voltage	CLK	2.5		5.25	V
	Input Leakage Current Inputs I/Os	$V_{DD} = 3.6V$, $0 \leq V_{IN} \leq V_{DD}$	-10 -10		-10 -10	μA μA
V_{OL}	Output Logic Low Voltage	$I_{LOAD} = 0.2$ to 5mA depending on the pin			0.4	V
V_{OH}	Output Logic High Voltage	$I_{LOAD} = 0.2$ to 5mA depending on the pin	2.4			V
C_{IN}	Input Capacitance	Bidirectional Pads, Input Pads			10	pF

4.3 AC ELECTRICAL CHARACTERISTICS

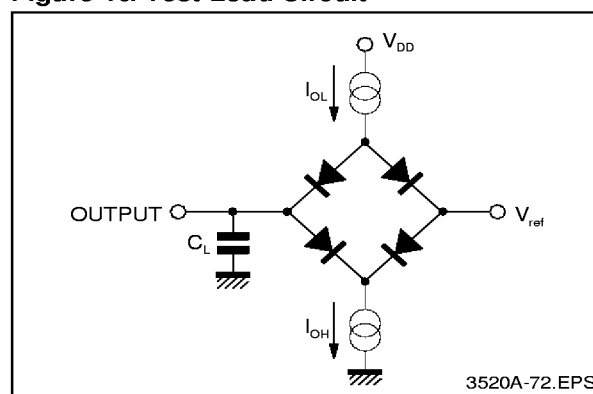
Test conditions: $V_{DD} = 3.3V \pm 0.3V$, $T_{amb} = 0$ to 70°C unless otherwise specified

Test Loads

Output	I_{OL}	I_{OH}	C_L	V_{REF}
D7-D0, REQ, WAIT	500 μA	500 μA	50pF	1.5V
IRQ	5mA	0	50pF	3.6V
A7-A0	200 μA	200 μA	50pF	1.5V
Other Outputs	200 μA	200 μA	50pF	1.5V

Notes: All values need to be characterised, values given are for guidance only.

Figure 10. Test Load Circuit



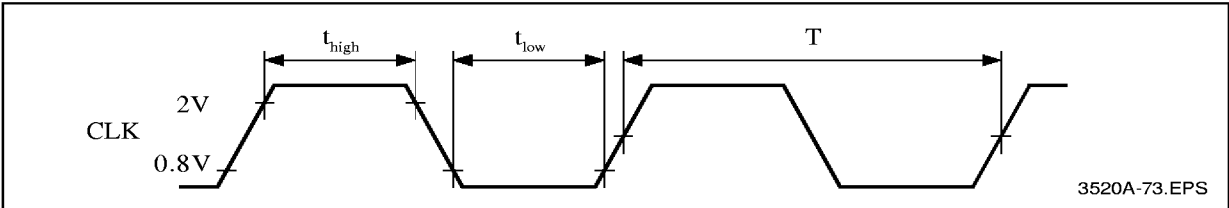
ELECTRICAL SPECIFICATIONS(Cont'd)

4.4 TIMING DIAGRAMS

Timings other than rise and fall times are specified with respect to a threshold of 1.5V.

4.4.1 Clock

Figure 11. Clock Signals

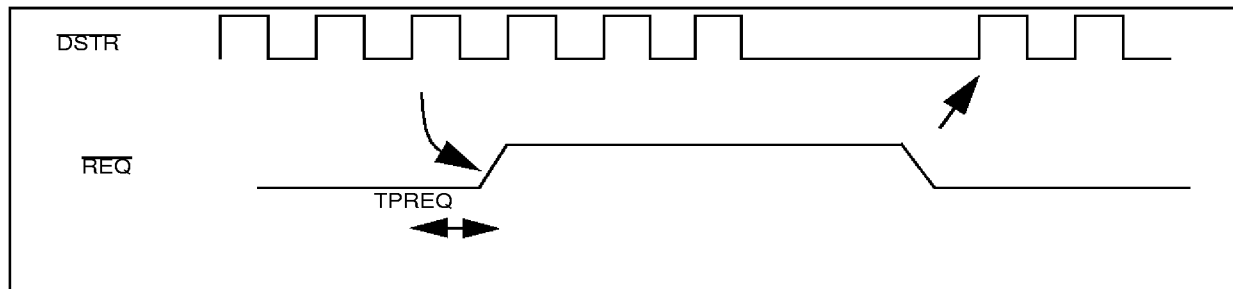
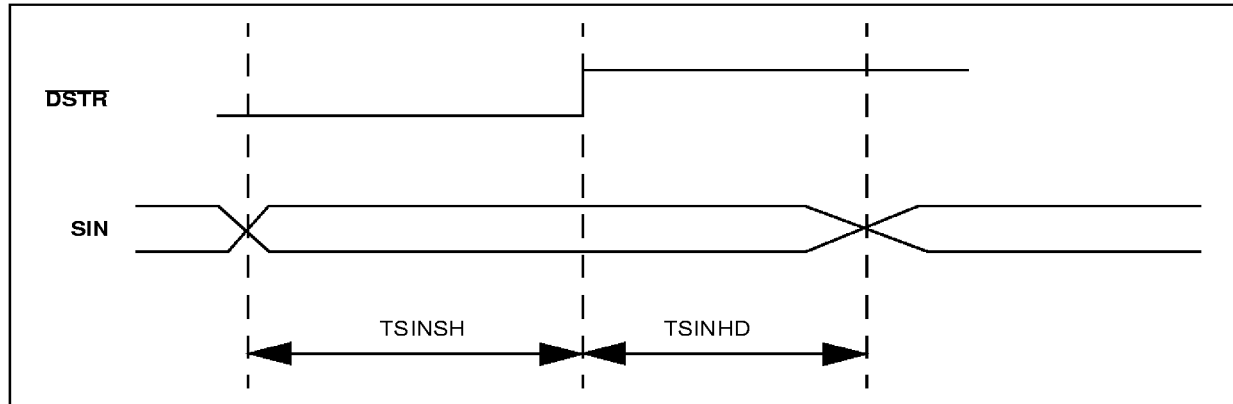


Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
T	Primary Clock Period (see note 1)	37ns			ns
T _{HIGH}	Clock High Time	10			ns
T _{LOW}	Clock Low Time	10			ns

Note 1: This corresponds to a maximum primary clock frequency of 27MHz.

ELECTRICAL SPECIFICATIONS(Cont'd)**4.4.2 Data Serial interface**

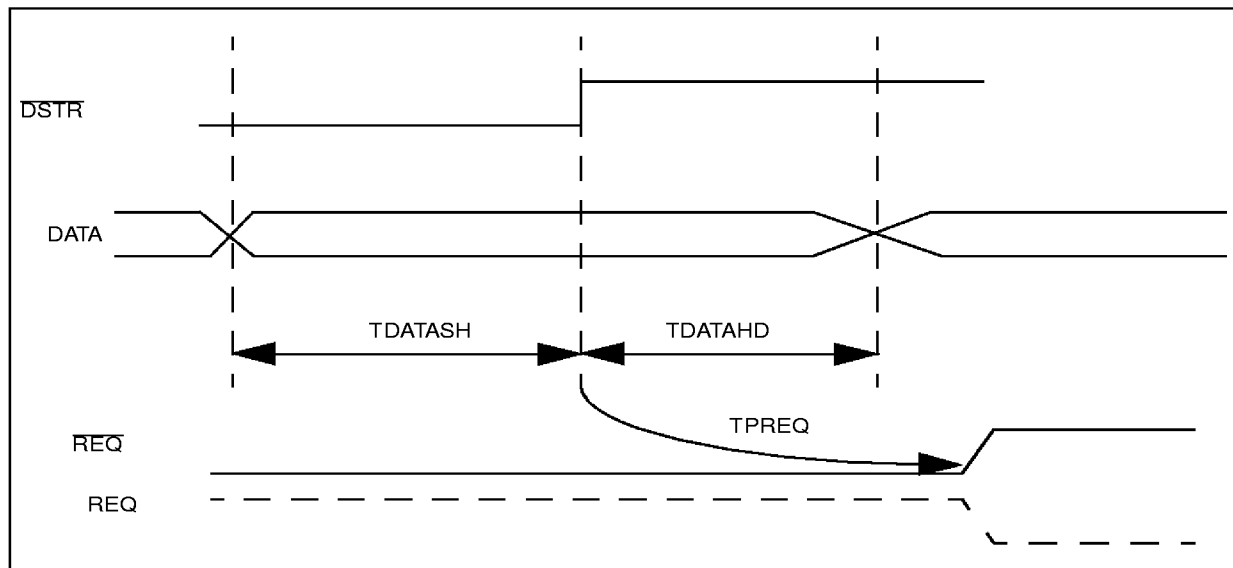
Register configuration: "SIN_SETUP"=1 and "CAN_SETUP"=Don't care



Symbol	Parameter	Min	Max	Unit
FDSTRBSerial	DSTR Max frequency in serial mode		33	Mhz
TDSTRBLOW	DSTR low pulse	5		ns
TDSTRBHIGH	DSTR high pulse	5		ns
TSINSH	SIN set-up time to DSTR rising edge	5		ns
TSINHD	SIN hold time from DSTR rising edge	5		ns
TPREQ	Propagation time from DSTR rising to REQ high	120	200	ns

ELECTRICAL SPECIFICATIONS (Cont'd)

4.4.3 Data Parallel interface



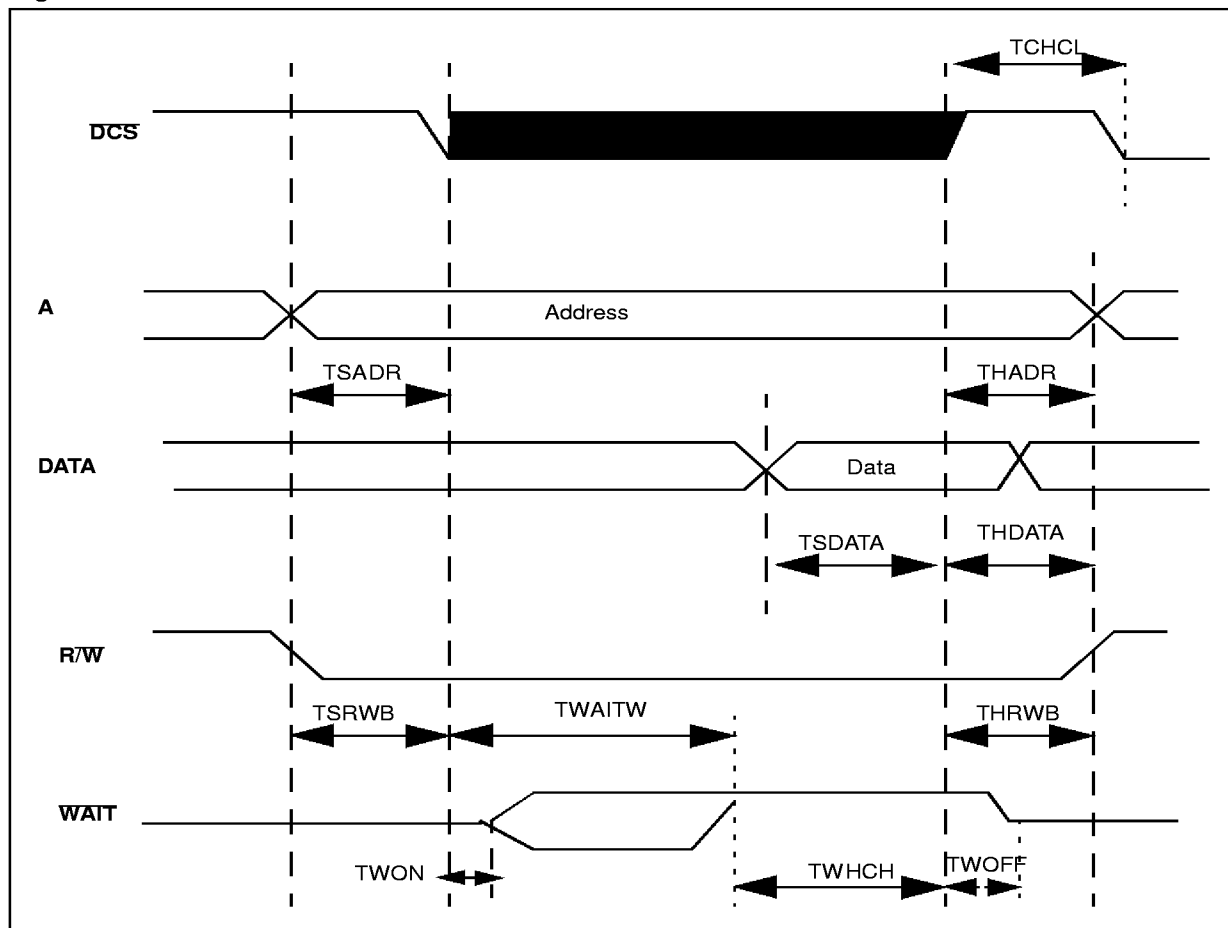
Note: Register configuration is "SIN_SETUP"=0 and "CAN_SETUP"=don't care.

Symbol	Parameter	Min	Max	Unit
FDSTRBPARA	DSTR Max frequency in parallel mode		4	Mhz
TDSTRBLOW	DSTR low pulse	5		ns
TDSTRBHIGH	DSTR high pulse	5		ns
T _{DATA SH}	DATA set-up time to DSTR rising edge	5		ns
T _{DATA HD}	DATA hold time from DSTR rising edge	5		ns
T _{PREQ}	Propagation time from DSTR rising to REQ deasserted	120	200	ns

ELECTRICAL SPECIFICATIONS(Cont'd)

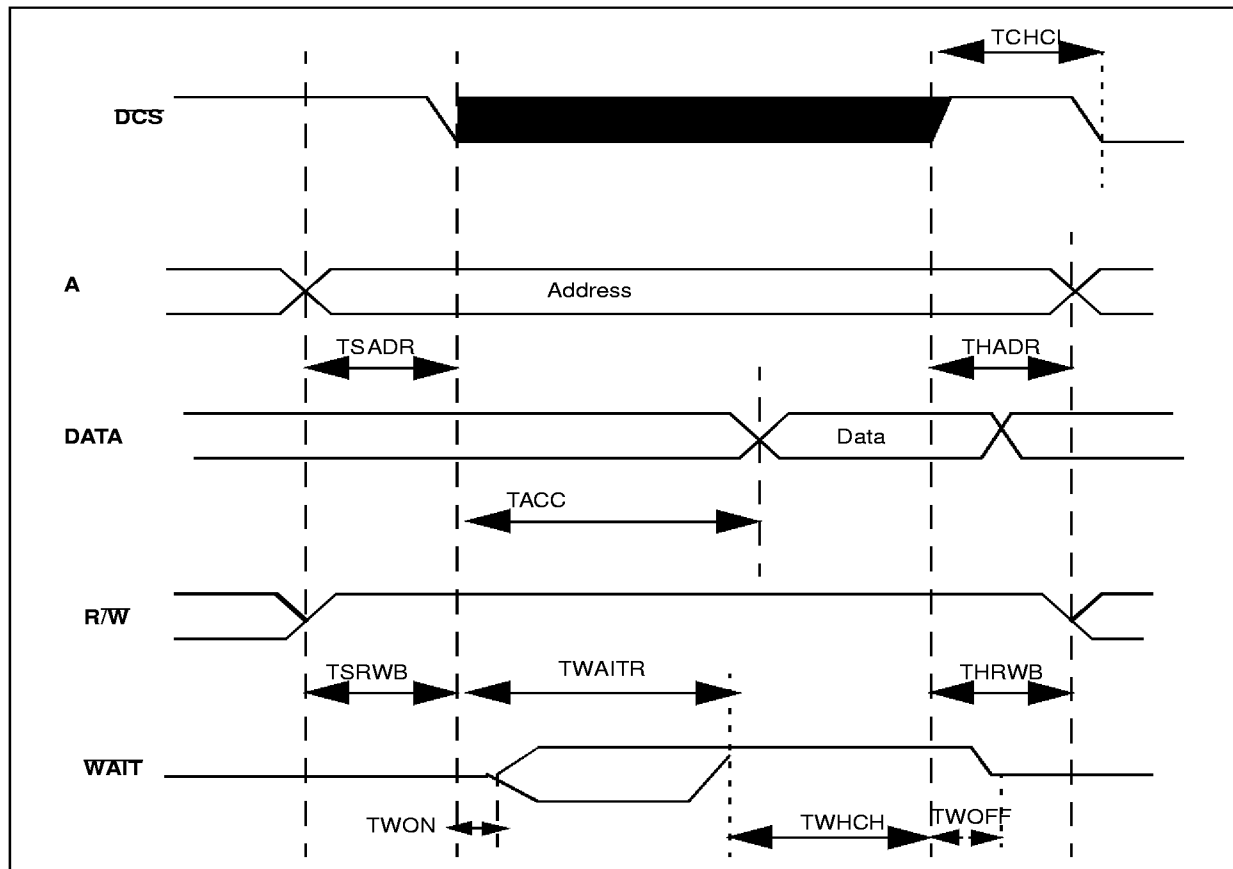
4.4.4 Parallel Control Interface

Figure 12. Write Access



ELECTRICAL SPECIFICATIONS(Cont'd)

Figure 13. Read Access



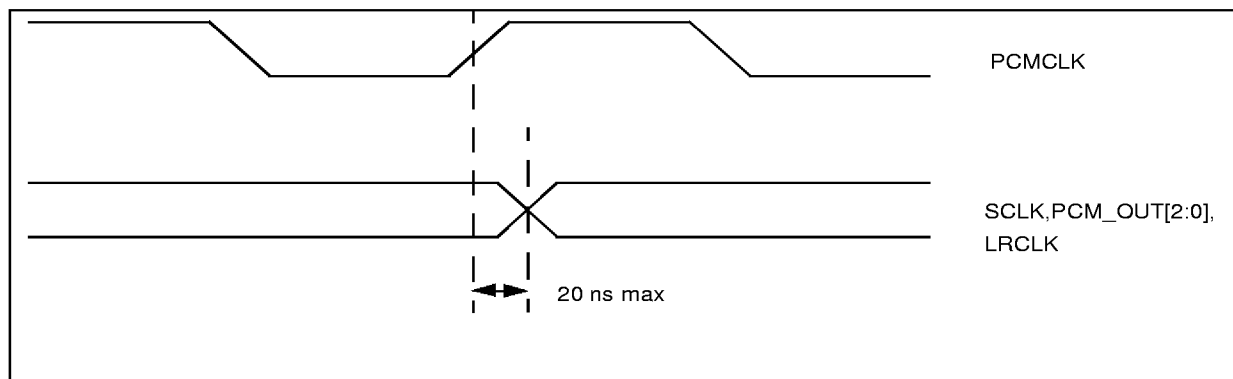
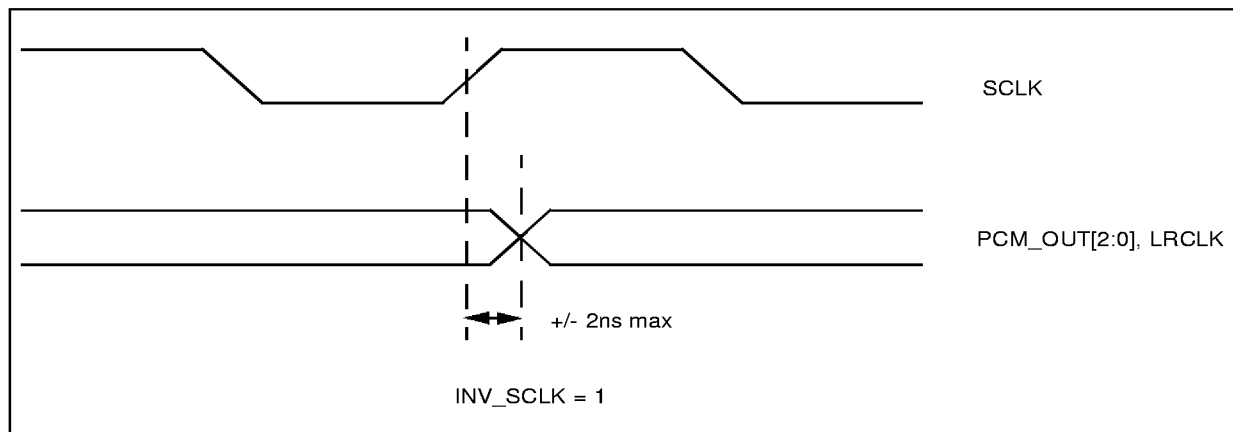
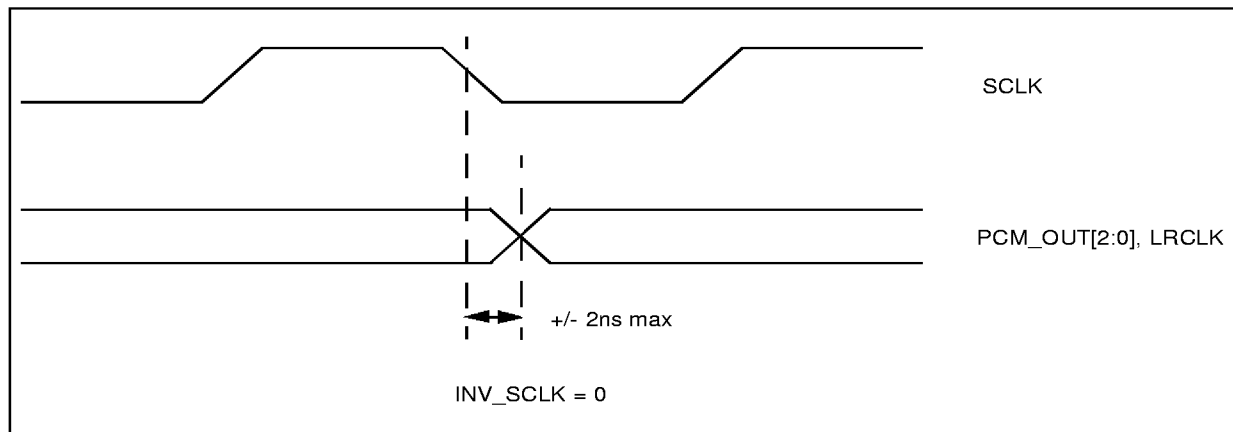
ELECTRICAL SPECIFICATIONS(Cont'd)

	Min	Max	
TSADR	5 ns		Hadr to $\overline{\text{DCS}}$ set-up time
TSDATA	5 ns		Hdata to $\overline{\text{DCS}}$ set-up time
TSRWB	5 ns		Hrwb to $\overline{\text{DCS}}$ set-up time
THADR	0 ns		Hadr to $\overline{\text{DCS}}$ hold time
THDATA	5 ns		Hdata to $\overline{\text{DCS}}$ hold time
THRWB	0 ns		Hrwb to $\overline{\text{DCS}}$ hold time
TWAITW	0.5 $T_{\text{sys}}+10$ 25 ns	1.5 $T_{\text{sys}}+10$ 55 ns	Maximum wait time when writing
TWAITR	1.5 $T_{\text{sys}}+10$ 55 ns	2.5 $T_{\text{sys}}+10$ 85 ns	Maximum wait time when reading
TCHCL	2 $T_{\text{sys}} + 10$: 70 ns		$\overline{\text{DCS}}$ high to $\overline{\text{DCS}}$ low
TWOFF		5 ns	$\overline{\text{DCS}}$ high to WAIT off
TWON		5 ns	$\overline{\text{DCS}}$ low to WAIT on
TWHCH	0 ns		WAIT high to $\overline{\text{DCS}}$ high
TACC	$T_{\text{sys}}+10$ 40 ns	2 $T_{\text{sys}}+10$ 70 ns	$\overline{\text{DCS}}$ low to Host Data ready

Note: T_{SYS} is the system clock period = 1/33 MHz = 30ns

ELECTRICAL SPECIFICATIONS (Cont'd)

4.4.5 PCM DATA Output Timing



Note: . Output pads SCLK, PCM_OUT[2:0] and LRCLK are assumed equally loaded.

5 REGISTER DESCRIPTION

5.1 INTRODUCTION

The STi4600 device includes 128 registers. In this document only the user registers are described. The undocumented registers are reserved. These registers must never be accessed (in Read or Write). The Read only registers must never be written.

Meaning of the abbreviations:

	COMMENT
NA	Not Applicable
UND	Undefined
NC	No Change
RO	Read Only
WO	Write Only
R/W	Read and Write
R/WS	Read, Write in specific mode

5.2 REGISTER MAP BY ADDRESS

Addr	Name	Addr	Name	Addr	Name
00	VERSION	40	SYNCSTATUS	60	IEC958_CONF
01	IDENT	41	ANCCOUNT	61	IEC958_STATUS
02	RESERVED	42	HEAD[31:24]	62	PDEC
03	RESERVED	43	HEAD[23:16]	63	BAL_SUR
04	RESERVED	44	HEAD[15:8]	64	PL_AB
05	SFREQ	45	HEAD[7:0]	65	PL_DWNX
06	EMPH	46	PTS[33]	66	OCFG
07	INTEL	47	PTS[31:24]	67	PCM_SCALE
08	INTEH	48	PTS[23:16]	68	DECODE_LFE/SKIP_LFE
09	INTL	49	PTS[15:8]	69	COMP_MOD/PROG_NO
0A	INTH	4A	PTS[7:0]	6A	HDR/DRC
0B	RESERVED	4B	USER	6B	LDR
0C	SIN_SETUP	4C	STREAMSEL	6C	RPC
0D	CAN_SETUP	4D	DECODESEL	6D	KARAMODE/MC_OFF
0E	DATAIN	4E	BAL_LR	6E	DUAL_MODE/MPEG_DUAL
0F	ERROR	4F	PACKET_LOCK	6F	DOWNMIX
10	SOFTRESET	50	AUDIO_ID_EN	70	DWSMODE
11	PLLSYS	51	AUDIO_ID	71	SOFTVER
12	PLLPCM	52	AUDIO_ID_EXT	72	RUN
13	PLAY	53	SYNC_LOCK	73	SKIP_FRAME
14	MUTE	54	PCMDIVIDER	74	REPEAT_FRAME
15	RESERVED	55	PCMCONF	75	IEC958-NULL-BURST
16	RESERVED	56	PCMPCROSS	76	STATUS0
17	RESERVED	57	LDLY	77	STATUS1
18	RESERVED	58	RDLY	78	STATUS2
19	RESERVED	59	CDLY	79	STATUS3
1A	RESERVED	5A	SUBDLY	7A	STATUS4
1B	RESERVED	5B	LSDLY	7B	STATUS5
1C	RESERVED	5C	RSDLY	7C	STATUS6
1D	RESERVED	5D	PCMUPDATE	7D	STATUS7
1E	RESERVED	5E	IEC958_CMD	7E	PCMCANCEL
1F	RESERVED	5F	IEC958_CAT	7F	PCMFORCECROSS

Note 1: Reserved Registers should not be written to.

Note 2: Addresses 20 through 3F contain reserved registers only.



REGISTER DESCRIPTION(Cont'd)**5.3 REGISTER MAP BY FUNCTION****Version (Section 1.4.1)**

HEX	DEC	NAME
0x00	0	VERSION
0x01	1	IDENT
0x71	113	SOFTVER

Setup + Inputs (Section 1.4.2)

0x11	17	PLLSYS
0x0C	12	SIN_SETUP
0x0D	13	CAN_SETUP
0x0E	14	DATAIN

PCM Configuration (Section 1.4.3)

0x54	84	PCMDIVIDER
0x55	85	PCMCONF
0x56	86	PCM CROSS
0x7E	126	PCM CANCEL
0x7F	127	PCM FORCECROSS

DAC and PLL Configuration (Section 1.4.4)

0x05	5	SFREQ
0x06	6	EMPH
0x12	18	PLLPCM

Channel Delay Setup (Section 1.4.5)

0x57	87	LDLY
0x58	88	RDLY
0x59	89	CDLY
0x5A	90	SUBDLY
0x5B	91	LSDLY
0x5C	92	RSDLY
0x5D	93	PCMUPDATE

IEC958 Output Setup (Section 1.4.6)

0x5E	94	IEC958_CMD
0x5F	95	IEC958_CAT
0x60	96	IEC958_CONF
0x61	97	IEC958_STATUS
0x75	117	IEC958-NULL-BURST

COMMAND (Section 1.4.7)

0x10	16	SOFTRESET
0x72	114	RUN
0x13	19	PLAY
0x14	20	MUTE
0x73	115	SKIP_FRAME
0x74	116	REPEAT_FRAME

Interrupt (Section 1.4.8)

0x07	7	INTEL
0x08	8	INTEH
0x09	9	INTL
0x0A	10	INTH

Interrupt Status (Section 1.4.9)

0x40	64	SYNCSTATUS
0x41	65	ANCCOUNT
0x42	66	HEAD[31:24]
0x43	67	HEAD[23:16]
0x44	68	HEAD[15:8]
0x45	69	HEAD[7:0]
0x46	70	PTS[33:32]
0x47	71	PTS[31:24]
0x48	72	PTS[23:16]
0x49	73	PTS[15:8]
0x4A	74	PTS[7:0]
0x4B	75	USER
0x0F	15	ERROR

Decoding (Section 1.4.10)

Decoding algorithm		
0x4C	76	STREAMSEL
0x4D	77	DECODESEL
System synchronization		
0x40	64	SYNCSTATUS
0x4F	79	PACKET_LOCK
0x50	80	AUDIO_ID_EN
0x51	81	AUDIO_ID
0x52	82	AUDIO_ID_EXT
0x53	83	SYNC_LOCK

REGISTER DESCRIPTION(Cont'd)**Post Decoding and Pro logic (Section 1.4.11)**

0x70	112	DWSMODE
0X62	98	PDEC
0X64	100	PL_AB
0X65	101	PL_DWNX

Note: The titles indicate the appropriate section of the specification.

Bass Redirection (Section 1.4.12)

0x66	102	OCFG
0X67	103	PCM_SCALE
0X4E	78	BAL_LR
0X63	100	BAL_SUR

AC3 Configuration (Section 1.4.13)

0x68	104	DECODE_LFE
0X69	105	COMP_MOD
0X6A	106	HDR
0X6B	107	LDR
0X6C	108	RPC
0X6D	109	KARAMODE
0X6E	110	DUAL_MODE
0X6F	111	DOWNMIX
0x76	118	AC3_STATUS0
0x77	119	AC3_STATUS1
0x78	120	AC3_STATUS2
0x79	121	AC3_STATUS3
0x7A	122	AC3_STATUS4
0x7B	123	AC3_STATUS5
0x7C	124	AC3_STATUS6
0x7C	125	AC3_STATUS7

MPEG Configuration (Section 1.4.14)

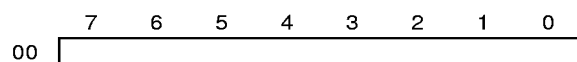
0x68	104	SKIP_LFE
0X69	105	PROG_NO
0X6E	106	MPEG_DUAL
0X6A	110	DRC
0X6D	109	MC_OFF
0X6F	111	DOWNMIX
0X76	118	MP_STATUS0
0X77	119	MP_STATUS1
0X78	120	MP_STATUS2
0X79	121	MP_STATUS3
0X7A	122	MP_STATUS4
0X7B	123	MP_STATUS5
0X7C	124	MP_STATUS6
0X7D	125	MP_STATUS7

REGISTER DESCRIPTION(Cont'd)

5.4 REGISTER MANUAL

5.4.1 Version registers

VERSION - Version



Address : 0x00
 Type : R0
 Software Reset: NA
 Hardware Reset: NA

Description

The VERSION register is read-only and is used to identify the IC on an application board.

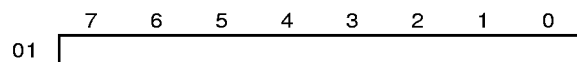
The version register holds the cut number (binary decimal encoded).

The version numbers are defined as below:

First PQFP120 cut, version number is: 0x10

First PQFP80 cut, version number is: 0x20

IDENT - Identify

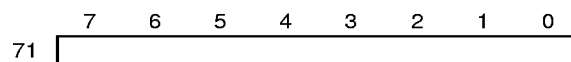


Address : 0x01
 Type : RO
 Software Reset: NA
 Hardware Reset: NA

Description

IDENT is a read-only register and is used to identify the IC on an application board. IDENT always has the value "0xAC".

SOFTVER - Software Version



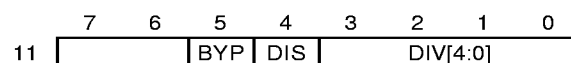
Address : 0x71
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

The SOFTVER register is the version of the micro-code which is running on the device. This register is updated just after a soft reset of the device. Today this register is not used.

5.4.2 Setup and Inputs

PLLSYS - System PLL Setup



Address : 0x11
 Type : R/W
 Software Reset: NC
 Hardware Reset: 0x16

Description

This PLL creates the system clock from the 27 MHz clock input.

The PLL can be bypassed and disabled. The frequency of the system clock is related to the value of the divider:

$\text{SYSCLK} = 1.5 \text{ MHz} \times \text{Div}$ Min freq : = 3 MHz, Max freq should be less or equal to 33 MHz

When a Hardreset occurs the PLL is enabled and runs at 33 MHz. When a "softreset" occurs this register is not changed and the PLL runs as before the softreset.

BYP : BYPASS. When set the PLL is bypassed CLKSYS= CLKIN

DIS : Disabled. When set the PLL is disabled (not running)

DIV[4:0] : Clock divider of the PLL

REGISTER DESCRIPTION(Cont'd)**SIN_SETUP - Input Data Setup**

	7	6	5	4	3	2	1	0
0C					X	POL		IMODE

Address : 0x0C
 Type : R/W
 Software Reset: NC
 Hardware Reset: 0

Description

This register is used to configure the input data interfaces. The register must be set before sending data to the IC. The mapping of the register is described below.

The two LSB of "SIN_SETUP" details which interface will be used. The bit (bit two of SIN_SETUP) is used to configure the polarity of the handshake signal "REQ". When the POL bit is high the "REQ" pin meaning is inverted, and the data must be input when "REQ" is "0". When POL is low, The data must be input when "REQ" is "1". The data must be sent to the device MSB first.

X : Reserved, not used

POL : Polarity of the REQ signal

IMODE[1:0]:Input Mode

IMODE is used to configure the data input interface. The configuration of the 3 possible interfaces is shown below:

Mode	Mode
0	Parallel input (DSTR + Data[7:0] + REQ)
1	Serial input (DSTR + SIN + REQ)
2	Not used
3	A/D input (DSTR + LRCLKIN + REQ + SIN)

When the IC is configured in mode 3, the input data comes from an A/D converter. In this case the "CAN_SETUP" register is used to configure the IC with respect to the A/D data format.

CAN_SETUP - A/D Converter Setup

	7	6	5	4	3	2	1	0
0D					16	SAM	FIR	PAD

Address : 0x0D
 Type : R/W
 Software Reset: NC
 Hardware Reset: 0

Description

CAN_SETUP is used to configure the STi4600 when receiving data from an A/D Converter. Also see SIN_SETUP register.

16 : When clear the slot count is 32 but only the 16th are extracted.

SAM : When set, data is sampled on the falling edge of the bit-clock (DSTR)

FIR : When set the first channel (Left) is with Lrclk= 1

PAD : When set the Lrclk is delayed by one cycle (Padding mode)

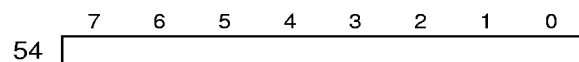
DATAIN - Data Input

	7	6	5	4	3	2	1	0
0E								

Address : 0x0E
 Type : WO
 Software Reset: NA
 Hardware Reset: NA

Description

Data can be fed into the STi4600 by using this register instead of the dedicated interface. There is no need to byte-align the bit-stream when using this register.

REGISTER DESCRIPTION(Cont'd)**5.4.3 PCM Configuration****PCMDIVIDER** - Divider for PCM Clock

Address : 0x54
 Type : R/W
 Software Reset: UND
 Hardware Reset: UND

Description

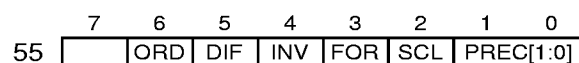
The PCM divider must be set according to the formula below, where Sclk is the bit clock for the DAC. When **Div** is set to 0, Sclk is equal to Pcm-Clk.

$$\text{Div} = (\text{PcmClk} / (2 \times \text{Sclk})) - 1$$

When the internal PLL is used, $\text{PcmClk} = 384 \times \text{fs}$.
 The formula becomes

$$\text{Div} = (192 \times \text{Fs} / \text{Sclk}) - 1$$

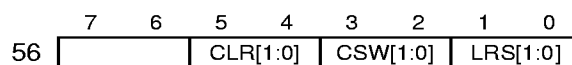
If Sclk is $32 \times \text{Fs}$ (common case with the 16 bit DAC), Div must be set to 5.

PCMCONF - PCM Configuration

Address : 0x55
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

ORD : PCM Order
 DIF : PCM_DIFF. If set to zero, right padded.
 INV : Invert LRCLK
 FOR : FORMAT. If 0 the format is I2S, if 1 the format is Sony format.
 SCL : INVERT SCLK
 PREC[1:0]: PCM Precision.
 0: 16 bit mode (16 slots)
 1: 18 bit mode (32 slots)
 2: 20 bit mode (32 slots)
 3: 24 bit mode (32 slots)

PCMCROSS - CROSS PCM CHANNELS

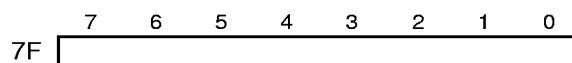
Address : 0x56
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

CLR[1:0] : Cross left and right channels.
 00: When 00, Left channel is mapped on the left output, Right channel is mapped on the Right output.
 01: When 01, Left channel is duplicated on both outputs.
 10: When 10, Right channel is duplicated on both outputs.
 11: When 11, Right channel and Left channel are toggled.

CSW[1:0]: Cross Centre and Subwoofer

LRS[1:0] : Cross Left and Right surround

PCMFORCECROSS - Enable PCMCROSS

Address : 0x7F
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

Enables the PCMCROSS Function.

REGISTER DESCRIPTION(Cont'd)**PCMCANCEL - FORCE PCM Output**

	7	6	5	4	3	2	1	0
7E			L	R	C	SW	LS	RS

Address : 0x7E

Type : R/W

Software Reset: NC

Hardware Reset: UND

Description

Used to force PCM output to zero.

- L : Force Left surround channel to zero when set.
- R : Force Right surround channel to zero when set.
- C : Force Centre surround channel to zero when set.
- SW : Force Subwoofer surround channel to zero when set.
- LS : Force Left surround channel to zero when set.
- RS : Force Right surround channel to zero when set.

5.4.4 DAC and PLL Configuration**SFREQ - Sampling Frequency**

	5	4	3	2	1	0
05						

Address : 0x05

Type : R/WS

Software Reset: NC

Hardware Reset: 0

Description

SFREQ is a status register which holds the code of the current sampling frequency. Bit 0 of SFREQ is directly connected to the pin SFREQ. The "SFREQ" pin is used to indicate if the sampling frequency is 48KHz or 44.1KHz (this information can be used by a DAC).

The value in SFREQ is associated with the following frequencies

Value	0	1	2	3	4	8*	9*	10*
FRE- QUENCY	48 KHz	44.1 KHz	32 KHz	not used	96 KHz	24 KHz	22.05 KHz	16 KHz

*Note: Values 8, 9, and 10 are intended for future versions of the STi4600. They are not supported in the current version.

EMPH - Emphasis

	5	4	3	2	1	0
06						E

Address : 0x06

Type : R/Ws

Software Reset: NC

Hardware Reset: 0

Description

- E : Bit 0 of the EMPH register is directly connected to the pin "DEEMPH".

REGISTER DESCRIPTION(Cont'd)**PLLPCM - PCM PLL Disable**

12

1	0
RP	DP

Address : 0x12
 Type : R/W
 Software Reset: NC
 Hardware Reset: 1

Description

When a Hard reset occurs the PLL is disabled. The host must write 0xD2 in this register to enable it.

When a Soft reset occurs the register remains unchanged.

RP : Run PLL. When high the DAC PLL is running.

DP : Disable pad. When low the PCM clock divider is enabled.

5.4.5 Channel Delay Setup

The unit for the delay is a group of 16 samples. The maximum delay is 35 ms. The sum of all the delays must be under $1680/16=35 \text{ ms} * 48 \text{ KHz}$.

When only one surround channel is present (Prologic or other mode), the right surround delay must be clear, the left delay channel is used for both surround channels.

LDLY - Left Channel

57

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

Address : 0x57
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

RDLY - Right Channel

58

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

Address : 0x58
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

CDLY - Centre Channel

59

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

Address : 0x59
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

SBDLY - Subwoofer Channel

5A

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

Address : 0x5A
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

LSDLY - Left Surround Channel

5B

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

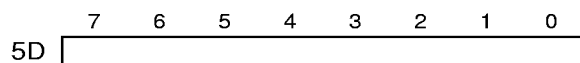
Address : 0x5B
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

RSDLY - Right Surround Channel

5C

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

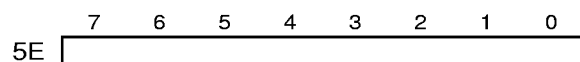
Address : 0x5C
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

REGISTER DESCRIPTION(Cont'd)**PCMPUPDATE - PCM Update**

Address : 0x5D
 Type : R/W
 Software Reset: 0
 Hardware Reset: 0

Description

Must be set to update the delay

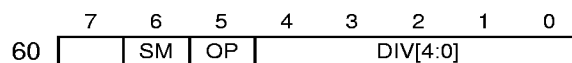
5.4.6 IEC958 Output Setup**IEC958_CMD - IEC958 Control**

Address : 0x5E
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

This register is the control register. Several modes are available, the mode is selected by value:

Value		Description
0	"Off" mode	The IEC958 is not working, the output line is idle. The value of the output line is determined by the value of bit 5 of the register IEC958_CONF. The line can be stuck to VDD or to GND.
1	MUT	"Muted" mode: The outputs are PCM null data.
2	PCM	"PCM" mode: The outputs are PCM data. Only the first two decoded channels (Left and Right) are transmitted.
3	ENC	"Encoded": The compressed bit-stream is transmitted (See IEC1937 standard)

IEC958_CONF - IEC958 PCMCLK Divider

Address : 0x60
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

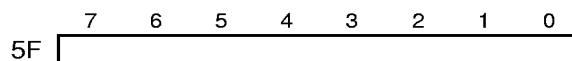
SM : SYNC MUTE Mode, must be set to zero.

OP : Line idle state level. The state of the interface when the interface is off.

DIV[4:0] : This field is the PCMCLK divider. It must be set according to the formula:
 In 16 bit mode:
 $IECDIV = (1 + PCMDIV) / 2 - 1$
 In 32 bit mode:
 $IECDIV = PCMDIV$

The table below shows the relationship between the value of the IEC divider and the value of the PCM divider described in Section 5.4.3.

PCM Divider Value	Mode Description	IEC Divider Value
5	PCMCLK=384 Fs, DAC is 16bit mode	2
3	PCMCLK= 256 Fs, DAC is 16 bit mode	1
2	PCMCLK= 384 Fs, DAC is 32 bit mode	2
1	PCMCLK= 256 Fs, DAC is 32 bit mode	1

IEC958_CAT - Category Code

Address : 0x5F
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

REGISTER DESCRIPTION(Cont'd)**IEC_STATUS** - IEC Status Bit

	7	6	5	4	3	2	1	0
61					SFR	PRE	COP	COM

Address : 0x61
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

This register is used to set the value of the status bit in the IEC958 data stream.

SFR : 44.1KHz sampling frequency bit
 PRE : Preemphasis data bit
 COP : Copy bit
 COM : Compress data bit
 This bit must be set to one in compressed mode and must be clear in non compressed mode.

IEC958_NULL_BURST - IEC958 Null Burst Data Length

	7	6	5	4	3	2	1	0
75								

Address : 0x75
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

In "compressed" mode, a burst of null data is sent when there is no more data to transmit (due to an error or a gap in the incoming bit-stream). This register is used to set the length of the burst. The length of the burst in "IEC958 sub-frame" unit. The length of the burst is (n+1), where n is the content of this register. This register must always be loaded with an odd value. We recommend to set this register to "7".

5.4.7 Command Registers**SOFTRESET** - SOFT RESET

	0
10	

Address : 0x10
 Type : W0
 Software Reset: NA
 Hardware Reset: NA

Description

When this register is written, a soft reset occurs. The command registers and the interrupt registers are cleared. The decoder goes into idle mode.

RUN - RUN Decoding

	0
72	

Address : 0x72
 Type : R/W
 Software Reset: 0
 Hardware Reset: 0

Description

After a soft or hard reset the decoder is in idle mode. The decoder stays in this mode until the register "RUN" is set. In run mode the decoder takes into account the state of all the configuration registers and begins to decode.

PLAY - PLAY

	0
13	

Address : 0x13
 Type : R/W
 Software Reset: 0
 Hardware Reset: 0

Description

The PLAY command is handled according to the state of the decoder (see section 3.3.1). PLAY only becomes active when the decoder is in DE-CODE mode.

REGISTER DESCRIPTION(Cont'd)**MUTE - MUTE**

14 0

Address : 0x14
 Type : R/W
 Software Reset: 0
 Hardware Reset: 0

Description

The MUTE command is handled according to the state of the decoder (see section 3.3.1). MUTE sets the clock running.

SKIP_FRAME - Skip a Frame

73 7 0

Address : 0x73
 Type : R/W
 Software Reset: 0
 Hardware Reset: 0

Description

When this register is set to one, the decoder clears it and then skips a frame. The number of samples in a frame depends on the nature of the frame, see table.

Decoding type	Sample count
AC3	1536
MPEG layer 2	1152
MPEG layer	384
L-PCM	80
PCM	NA

REPEAT_FRAME - Repeat a Frame

74 7 0

Address : 0x74
 Type : R/W
 Software Reset: 0
 Hardware Reset: 0

Description

In this case the previous frame is repeated. When the register is taken in account, the decoder clears it.

REGISTER DESCRIPTION(Cont'd)**5.4.8 Interrupt registers****INTE - Interrupt Enable**

	7	0
08	INTE[15:8]	
07	INTE[7:0]	

Address : 0x08-0x07
 Type : R/W
 Software Reset: 0
 Hardware Reset: 0

Description

The audio decoder contains a 16 bit interrupt register associated with a 16 bit "enable" register.

A bit set in this register will enable the corresponding interrupt. The interrupt associated with each bit is given in the register INT description.

INT - Interrupt

	7	0
0A	INT[15:8]	
09	INT[7:0]	

Address : 0x0A-0x09
 Type : RO
 Software Reset: 0
 Hardware Reset: 0

Description

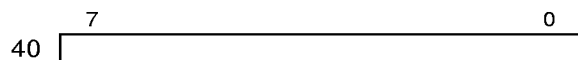
An interrupt is signalled whenever one of the bits of INT become set. This can only occur if the corresponding bit is set in the INTE register.

The Table below shows the condition indicated by each bit.

#	Name	Condition Signalled
0	SYN	Change in synchronization status (2)
1	HDR	Valid Header registered (2)
2	ERR	Error Detected(2)
3	SFR	Sampling frequency changed (1)
4	DEM	De-emphasis changed (1)
5	BOF	First bit of new frame at output stage (1)
6	PTS	First bit of new frame with PTS at output stage (2)
7	ANC	Ancillary data registered (2), Not implemented
8	PCM	Pcm output underflow (1)
9	FBF	Not implemented
10	FBE	Not implemented
11	FIO	FIFO input has overflowed (1)
12	TBD	Reserved (1)
13	TBD	Reserved (1)
14	USR	Reserved (2)
15	TBD	Reserved

(1) Cleared when the interrupt register is read or when a Reset occurs

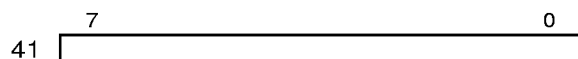
(2) Cleared when the corresponding register is read, or when a reset occurs

REGISTER DESCRIPTION(Cont'd)**5.4.9 Interrupt Status registers****SYNCSTATUS** - Synchronization Status

Address : 0x40
 Type : RO
 Software Reset: UND
 Hardware Reset: UND

Description

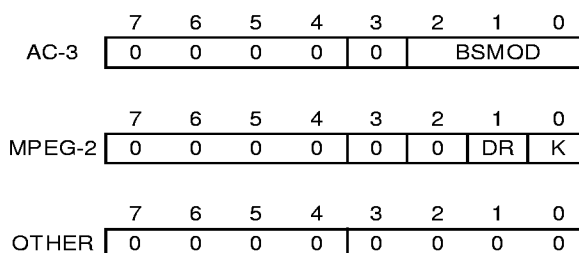
On read the synchronization status interrupt bit is cleared (INT.SYN is cleared).

ANCCOUNT - Ancillary Data

Address : 0x41
 Type : RO
 Software Reset: UND
 Hardware Reset: UND

Description

On read the ancillary data interrupt bit is cleared (INT.ANC is cleared).

HEAD4 - HEADER 4 register

Address : 0x42
 Type : RO
 Software Reset: UND
 Hardware Reset: UND

Description

This register contains header data HEAD[31:24]. The contents depend on the type of the frame.

HEAD4[7:3] = 0000 in all cases

AC-3

HEAD4[2:0] = BSMOD if an AC-3 frame

MPEG-2

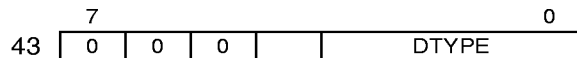
HEAD4[2] = 0,

HEAD4[1] = DR. Dynamic range exists

HEAD4[0] = K. K=0 in normal mode, K=1 in Karaoke mode.

OTHER

In all other types of frame HEAD4[2:0] = "000"

REGISTER DESCRIPTION(Cont'd)**HEAD3 - HEADER 3 register**

Address : 0x43
 Type : RO
 Software Reset: UND
 Hardware Reset: UND

Description

This register contains header data HEAD[23:16].

HEAD3[7:5] = "000" in all cases

HEAD3[4:0] = DTYPE

DTYPE is the data type and the meaning is as follows:

0000:	Null data or Linear PCM
0001:	AC-3
0100:	MPEG-1 Layer I
0101:	MPEG-1 Layer 2 or MPEG-2 wo extension
0110:	MPEG-2 Layer 2 with extension
1000:	MPEG-2 Layer I low sample rate
1001:	MPEG-2 Layer II low sample rate

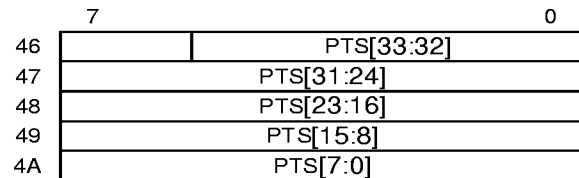
HEADLEN - Frame Length

Address : 0x44-0x45
 Type : RO
 Software Reset: UND
 Hardware Reset: UND

Description

The HEADLEN register contains the bit length of the compressed data frame HEAD[15:0].

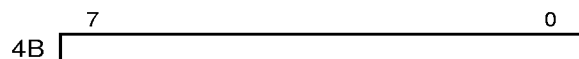
The HEADER registers are all updated as soon as the decoder begins to decode a frame.

PTS - PTS

Address : 0x46-0x47-0x48-0x49-0x4A
 Type : RO
 Software Reset: UND
 Hardware Reset: UND

Description

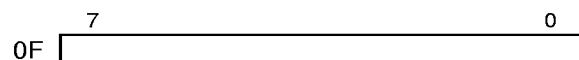
The 34 bit PTS register contains the PTS value. When this value is read the corresponding interrupt bit is cleared (INT.PTS is cleared).

USER - USER Data

Address : 0x4B
 Type : RO
 Software Reset: UND
 Hardware Reset: UND

Description

When this register is read, the user interrupt is cleared (INT.USR is cleared).

ERROR - ERROR Code

Address : 0x0F
 Type : RO
 Software Reset: 0
 Hardware Reset: 0

Description

This register is a status register, when the host reads this register, this register and the corresponding interrupt register are cleared.

The value in the ERROR register indicates the type of error that has occurred, see Table 1.

REGISTER DESCRIPTION(Cont'd)

Table 3. Error register list

Error Name	Value
AC3 Decoding	
NO_ERROR	0
EXPAND_DELTA_PAST_END_ARRAY	1
XDCALL_TRY_TO_REUSE_REMAT_FLG	2
XDCALL_TRY_TO_REUSE_COUPLING_STR A	3
XDCALL_CANT_COUPLE_IN_DUAL_MODE	4
XDCALL_TRY_TO_REUSE_CPL_LEAK	5
XDCALL_TRY_TO_REUSE_SNR	6
XDCALL_TRY_TO_REUSE_BIT_ALLOC	7
XDCALL_TRY_TO_REUSE_COUPLING_EXPONENT_STRA	8
XDCALL_TRY_TO_REUSE_EXPONENT_STR A	9
XDCALL_TRY_TO_REUSE_LFE_EXPONENT STRA	10
XDCALL_CHBWCOD_IS_TOO_HIGH	11
BSI_ERR_REV	12
BSI_ERR_CHANS	13
CRC_NOT_VALID	14
Packet synchronization	
SYNCHRO_PACKET_NOT_FOUND	16
BAD_MPEG1_RESERVED_WORD	17
BAD_MPEG2_RESERVED_WORD	18
DIFF_first_access_pointer_AP_LENGTH	19
UNKNOWN_STREAM_ID	20
MARKER_ERROR	21
UNKNOWN_SUB_STREAM_ID	22

Error Name	Value
Audio Synchronization	
UNKNOWN_SUB_STREAM_ID	32
BAD_CRC_AC3	33
BAD_quantization_wordlength	34
BAD_audio_sampling_freq	35
BAD_MPEG_LAYER	36
MPEG_BITRATE_FREE_FORMAT	37
NOT_SUPPORTED_FRMSIZECOD	38
BAD_CRC_MPEG_FRONT_END	39
BAD_BIT_AFTER_LENGTH_FIELD_IN_MPEG_EXTENDED	40
MPEG_EXTENDED_SYNC_NOT_FOUND	41
MPEG decoding	
MPEG_EXTENSION_ERROR	48
MPEG_MC_MUTE	49
NOT_USED (OLD MPEG_FS_CHANGE)	50
NOT_USED (OLD MPEG_EMPHASIS_CHANGE)	51
MPEG_LAYER_ERROR	52
MPEG_CHCONFIG_ERROR	53
MPEG_MC_PREDICTION_ERROR	54
MPEG_CRC_ERROR	55
MPEG_EXT_CRC_ERROR	56
MPEG_TOO_SMALL_FOR_MC_HEADER	57
MPEG_BITRATE_ERROR	58

REGISTER DESCRIPTION(Cont'd)**5.4.10 Decoding Registers****STREAMSEL - STREAM Selection**

4C 7 0

Address : 0x4C
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

Value	Mode
0	PES
1	PES DVD
2	Packet MPEG1
3	Elementary Stream

DECODESEL - Decoding Algorithm

4D 7 0

Address : 0x4D
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

bit(2:0)	Mode
0	AC3 Decoding
1	MPEG1/II
2	MPEG1/II extended
3	PCM
4	PINK NOISE generator

SYNCSTATUS - Synchronization Status

40 7 0

Address : 0x40
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

Status of the synchronization process.

PACKET_LOCK - Packet Lock

4F 7 0

Address : 0x4F
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

Number of packet use for synchronisation, max=1 min=0.

AUDIO_ID_EN - Enable audio ID

50 7 0

Address : 0x50
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

If set the decoders decode only the matching ID.

AUDIO_ID - Audio ID

51 7 0

Address : 0x51
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

Matching ID for the Packet.

REGISTER DESCRIPTION(Cont'd)**AUDIO_ID_EXT** - Audio Extension

52 7 0

Address : 0x52
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

Matching ID for the Packet extension part.

SYNC_LOCK - SYNC Lock

53 7 0

Address : 0x53
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

Number of Audio frame use for synchronisation, max=3 min=0.

Table 4. Sync Status bit mapping

Bit number	selected mode	
1:0	Frame Status	0 research syn word 1 Wait for confirmation 2 Synchronized 3 Not used
3:2	Packet Status	0 research syn word 1 Wait for confirmation 2 Synchronized 3 Not used

5.4.11 Post Decoding and Prologic**DWSMODE** - Downsampling Filter

70 7 0

Address : 0x70
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

This is an 8 bit register whose value controls the downsampling filter.

Value	Meaning
0	Automatic (according to bitstream)
1	Force Downsampling
2	Suppress Downsampling

PDEC - Post Decoder Register

62 7 6 5 4 3 2 1 0

DEM
DCF

PL

Address : 0x62
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

This register is used to control the post decoder operations.

DEM : When high the deemphasis filter is activated.
 DCF : When high the DC filter is activated
 PL : When high Prologic decoding is forced, when low the PL decoder is activated only if the output of the previous decoding stage is Pro Logic encoded.

REGISTER DESCRIPTION(Cont'd)**PL_AB** - Prologic auto balance

64 7 0

Address : 0x64
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

Setting this 8-bit register enables the auto balance function. The default value is zero (auto balance off).

PL_DWNX - Prologic Downmix

65 7 0

Address : 0x65
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

This value in this register controls the function of the Prologic Downmix, see Table 3.

Table 5. Prologic Downmix

Value	Comment
0, 1, 2	Prologic is disabled
3	3/0 (L,C,R) three stereo
4	2/1 (L,R,S) phantom
5	3/1 (L,C,R,S)
6	2/2 (L,R,Sl, Sr) phantom
7	3/2 (L,C,R,Sl, Sl)

5.4.12 Bass Redirection**OCFG** - Output Configuration

66 7 0

Address : 0x66
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

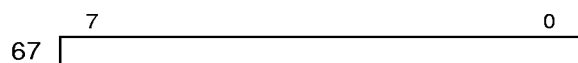
Description

This register is 8 bit and should be loaded with a decimal number with value between 0 and 6. The values 5 and 6 are reserved for future variants.

LP means Low pass filter.

HP means High pass filter

Value	Meaning	
4	SUM	The subwoofer is equal to the sum of all input channels. SUB=L+R+Ls+Rs+C+LFE
3	SLP	Low frequencies are extracted from the input channels and redirected to the sub-woofer. SUB=LP(L+R+Ls+Rs+C+LFE)
2	LLR	Low frequencies are extracted from C, LFE, Ls and Rs channels and redirected to left and right channels. L=L+LP(C,LFE,Ls,Rs) R=R+LP(C,LFE,Ls,Rs)
1	LSW	Low frequencies are extracted from the input channels and redirected to the sub-woofer. SUB=LP(L,R,Ls,Rs,C,LFE) Low frequencies are removed from all channels. L=HP(L) R=HP(R) C=HP(C) Ls=HP(Ls) Rs=HP(Rs)
0	ALL	All channels are rounded and scaled

REGISTER DESCRIPTION(Cont'd)**PCMSCALE** - PCM Scale Factor

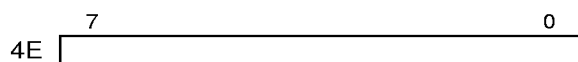
Address : 0x67
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

This register is an 8 bit and loaded with the value of PCM scale.

PCM scale is a master scale factor. It is expressed in 2 dB attenuation.

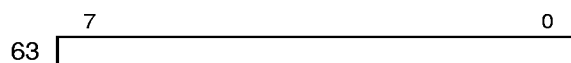
Attenuation = -2k dB (where k is the register content). When k=0 the attenuation is not exactly 0 dB but it corresponds to a scale of 255/256.

BAL_LR - Left/Right Balance

Address : 0x4E
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

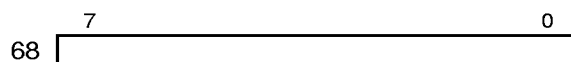
This register is an 8 bit signed byte register (-128, +127) and controls the Left/Right channel balance. When the value is positive the Left channel is attenuated, when the value is negative the right channel is attenuated. The attenuation is done in steps of 0.5 dB.

BAL_SUR - L/R Surround Balance

Address : 0x63
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

This register is an 8 bit signed byte register (-128, +127) and controls the Left/Right surround balance. When the value is positive the Left channel is attenuated, when the value is negative the right channel is attenuated. The attenuation is done in steps of 0.5 dB.

5.4.13 AC3 Decoding**DECODE_LFE** - Decode LFE

Address : 0x68
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

When high decode LFE channel (if present)

REGISTER DESCRIPTION(Cont'd)**COMP_MOD** - Compression Mode

69 7 0

Address : 0x69
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

The value of this register defines the compression mode

Value	Meaning
0	Line Out
1	RF mode
2	Custom 1
3	Custom 2

HDR - High Dynamic Range

6A 7 0

Address : 0x6A
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

0x7F (0,99)
 0x00 => no level

LDR - Low Dynamic Range

6B 7 0

Address : 0x6B
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

0x7F (0,99)
 0x00 => no level

RPC - Repeat Count

6C 7 0

Address : 0x6C
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

Repeat Count

KARAMODE - Karaoke Downmix

6D 7 0

Address : 0x6D
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

Karaoke Downmix

Value	Comment	Capable
0	Aware	
1	Multichannel reproduction	
2	Downmix AC3 karaoke, Do not reproduce V1/V2	
3	Downmix AC3 karaoke, Reproduce V1	
4	Downmix AC3 karaoke, Reproduce V2	
5	Downmix AC3 karaoke, Reproduce V1 & V2	

REGISTER DESCRIPTION(Cont'd)**DUALMODE - Dual Downmix**

7 0
6E

Address : 0x6E
Type : R/W
Software Reset: NC
Hardware Reset: UND

Description

Dual (1+1) Downmixr

Value	Comment
0	Output as Stereo
1	Output channel 1 on both output L/R
2	Output channel 2 on both output L/R
3	Mix channel 1 and 2 to monophonic and output on both L/R

DOWNMIX - Downmix

7 0
6F

Address : 0x6F
Type : R/W
Software Reset: NC
Hardware Reset: UND

Description

Downmix register, see table.

Value	Comment
0	2/0 Dolby Surround
1	1/0 Centre
2	2/0 (L,R)
3	3/0 (L,C,R)
4	2/1 (L,R,S)
5	3/1 (L,C,R,S)
6	2/2 (L,R,LS,RS)
7	3/2 (L,C,R,Ls,Rs)
8	TBD

AC3_STATUS0 - AC-3 Status Register

7 0
76

Address : 0x76
Type : RO
Software Reset: NC
Hardware Reset: UND

Bit number	Name
7	Not-Used
6:5	fs_cod
4:0	Bitrate code

AC3_STATUS1 - AC-3 Status Register 1

7 0
77

Address : 0x77
Type : RO
Software Reset: NC
Hardware Reset: UND

Bit number	Name
7:4	Not-Used
3	Lfe
2:0	Acmod

AC3_STATUS2 - AC-3 Status Register 2

7 0
78

Address : 0x78
Type : RO
Software Reset: NC
Hardware Reset: UND

Bit number	Name	Comment
7:5	Bsmode	
4:0	Bsid	

REGISTER DESCRIPTION(Cont'd)**AC3_STATUS3** - AC-3 Status Register 3

79 7 0

Address : 0x79
 Type : RO
 Software Reset: NC
 Hardware Reset: UND

Bit number	Name	Comment
7:4	Not used	
3:2	Cmixlevel	
1:0	SurMixlevel	

AC3_STATUS4 - AC-3 Status Register 4

7A 7 0

Address : 0x7A
 Type : RO
 Software Reset: NC
 Hardware Reset: UND

Bit number	Name
7:5	Not used
4:3	Dsurmod
2	Copyright
1	Origbs
0	Lancode

AC3_STATUS5 - AC-3 Status Register 5

7B 7 0

Address : 0x7B
 Type : RO
 Software Reset: NC
 Hardware Reset: UND

Bit number	Name
7:0	Langcod

AC3_STATUS6 - AC-3 Status Register 6

7C 7 0

Address : 0x7C
 Type : RO
 Software Reset: NC
 Hardware Reset: UND

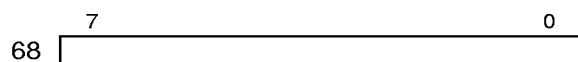
Bit number	Name
4:0	DialNorm

AC3_STATUS7 - AC-3 Status Register 7

7D 7 0

Address : 0x7D
 Type : RO
 Software Reset: NC
 Hardware Reset: UND

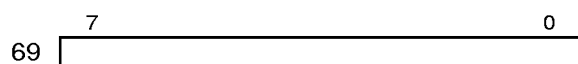
Bit number	Name
7:6	Room type
5:1	Mix level
0	Audprodie

REGISTER DESCRIPTION(Cont'd)**5.4.14 MPEG decoding****SKIP_LFE** - SKIP LFE Channel

Address : 0x68
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

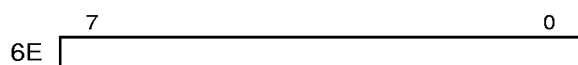
Skip LFE channel when On
 Decode Lfe channel when Off

PROG_NUMBER - PROGRAM NUMBER

Address : 0x69
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

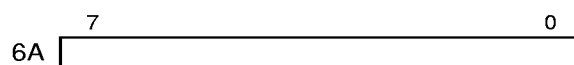
Select the Program #0 or #1
 0: L0,R0 in front channels
 1: L2,R2 in front channels

MPEG_DUAL - MPEG Setup DUAL MODE

Address : 0x6E
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

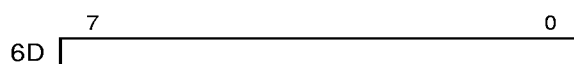
When Dual mode bitstream:
 0 play only channel#1
 1 play only channel #2

DRC - Dynamic Range Control

Address : 0x6A
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

Dynamic range control
 (Future extension)

MC_OFF - Multichannel

Address : 0x6D
 Type : R/W
 Software Reset: NC
 Hardware Reset: UND

Description

When set the multi channel part of the bitstream is not decoded,
 Only the MPEG1 compatible bitstream is decoded.

REGISTER DESCRIPTION(Cont'd)**DOWNMIX - MPEG Setup**

7 0
6F

Address : 0x6F
Type : R/W
Software Reset: NC
Hardware Reset: UND

Description

See Table below.

Karaoke Aware mode is defined for the DVD system by applying "second stereo" mode if MPEGII.

MPEG Downmix

Value	Comment
0	1/0
1	2/0 (L,R)
2	3/0 (L,C,R)
3	2/1 (L,R,S)
4	3/1 (L,C,R,S)
5	2/2 (L,R,LS,RS)
6	3/2 (L,C,R,Ls,Rs)

MP_STATUS0 - MPEG Status Register 0

7 6 5 4 3 2 1 0
76

Address : 0x76
Type : RO
Software Reset: NC
Hardware Reset: UND

Description

ID : Identifier
LAY[1:0] : Layer
P : Protection Bit
BRI[3:0] : Bit rate index

MP_STATUS1 - MPEG Status Register 1

7 6 5 4 3 2 1 0
77

Address : 0x77
Type : RO
Software Reset: NC
Hardware Reset: UND

Description

SFR[1:0] : Sampling Frequency
PAD : Padding Bit
PRI : Private Bit
MOD[1:0] : Mode
MEX[1:0] : Mode Extension

MP_STATUS2 - MPEG Status Register 2

7 6 5 4 3 2 1 0
78

Address : 0x78
Type : RO
Software Reset: NC
Hardware Reset: UND

Description

Bits[7:4] : Not used
C : Copyright
OCB : Original/Copy Bit
EMP[1:0] : Emphasis rate index

REGISTER DESCRIPTION(Cont'd)**MP_STATUS3** - MPEG Status Register 3

	7	6	5	4	3	2	1	0
79	CEN[1:0]	SUR[1:0]	LFE	AMX	DEM[1:0]			

Address : 0x79

Type : RO

Software Reset: NC

Hardware Reset: UND

Description

CEN[1:0] : Centre

SUR[1:0] : Surround

LFE : LFE

AMX : Audio mix

DEM[1:0] : Dematrix procedure

MP_STATUS4 - MPEG Status Register 4

	7	6	5	4	3	2	1	0
7A	EXT	NML[2:0]	MFS	MLY	CIB	CIS		

Address : 0x7A

Type : RO

Software Reset: NC

Hardware Reset: UND

Description

EXT : Extension bitstream present

NML[2:0] : Number of Multi-lingual Channels

MFS : Multi-lingual FS

MLY : Multi-lingual Layer

CIB : Copyright ID Bit

CIS : Copyright ID Start

MP_STATUS5 - MPEG Status Register 5

	7	6	5	4	3	2	1	0
7B								

Address : 0x7B

Type : RO

Software Reset: NC

Hardware Reset: UND

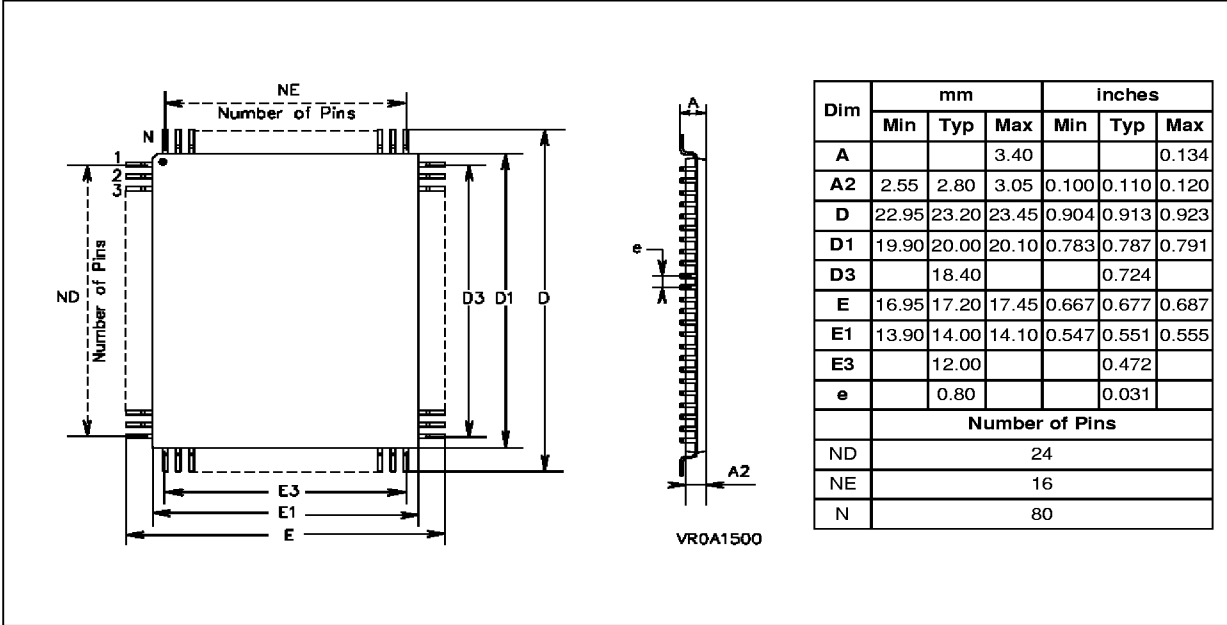
Description

The number of extended ancillary data bytes is contained in this register

6 GENERAL INFORMATION

6.1 PACKAGE MECHANICAL DATA

Figure 14. 80-Pin Plastic Quad Flat Package



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