Z86L03/L06/L16

CONSUMER CONTROLLER PROCESSOR

FEATURES

Part	ROM (KB)	RAM* (Bytes)	I/O	Voltage Range
Z86L03	0.5	60	14	2.0V to 3.6V
Z86L06	1.0	124	14	2.0V to 3.6V
Z86L16	1.0	124	14	2.0V to 3.6V

Note: *General-Purpose

- Fast Instruction Pointer: 1.5 µs @ 8 MHz
- Expanded Register File Control Registers
- One/Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Watch-Dog/Power-On Reset Timers
- Two Standby Modes: STOP and HALT
- Two Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.
- Software Programmable Low EMI Mode (4 MHz only)
- ROM Protect Option

GENERAL DESCRIPTION

Zilog's Z86L03/L06/L16 CCP™ (Consumer Controller Processors) are members of Zilog's two volt Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 0.5 and 1K bytes of ROM and 60 and 124 bytes of general-purpose RAM, respectively, these 18-pin CMOS CCPs offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with cost-effective and low power consumption.

The Z86L03/L06/L16 architecture is characterized by Zilog's 8-bit microcontroller core with the addition of an Expanded Register File to allow easy access to register mapped peripheral and I/O circuits. The Z86L03/L06/L16 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, and industrial applications.

For applications demanding powerful I/O capabilities, the Z86L03/L06/L16 provides 14 pins dedicated to input and output. These lines are grouped into two ports and are configurable under software control to provide timing, status signals, or parallel I/O (Figure 1).

Three basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File. The register file is composed of 60/124 bytes of general-purpose registers, two I/O port registers, and 13/15 control and status registers. The Expanded Register File consists of three control registers in the Z86L03, and four control registers in the Z86L06/L16.

With powerful peripheral features, such as on-board comparators, counter/timer(s), Watch-Dog Timer (WDT), and software programmable Low EMI Mode, the Z86L03/L06/L16 meets the needs of a variety of sophisticated controller applications.

GENERAL DESCRIPTION (Continued)

Notes: All Signals with a preceding front slash, "/", are active Low, e.g.:B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

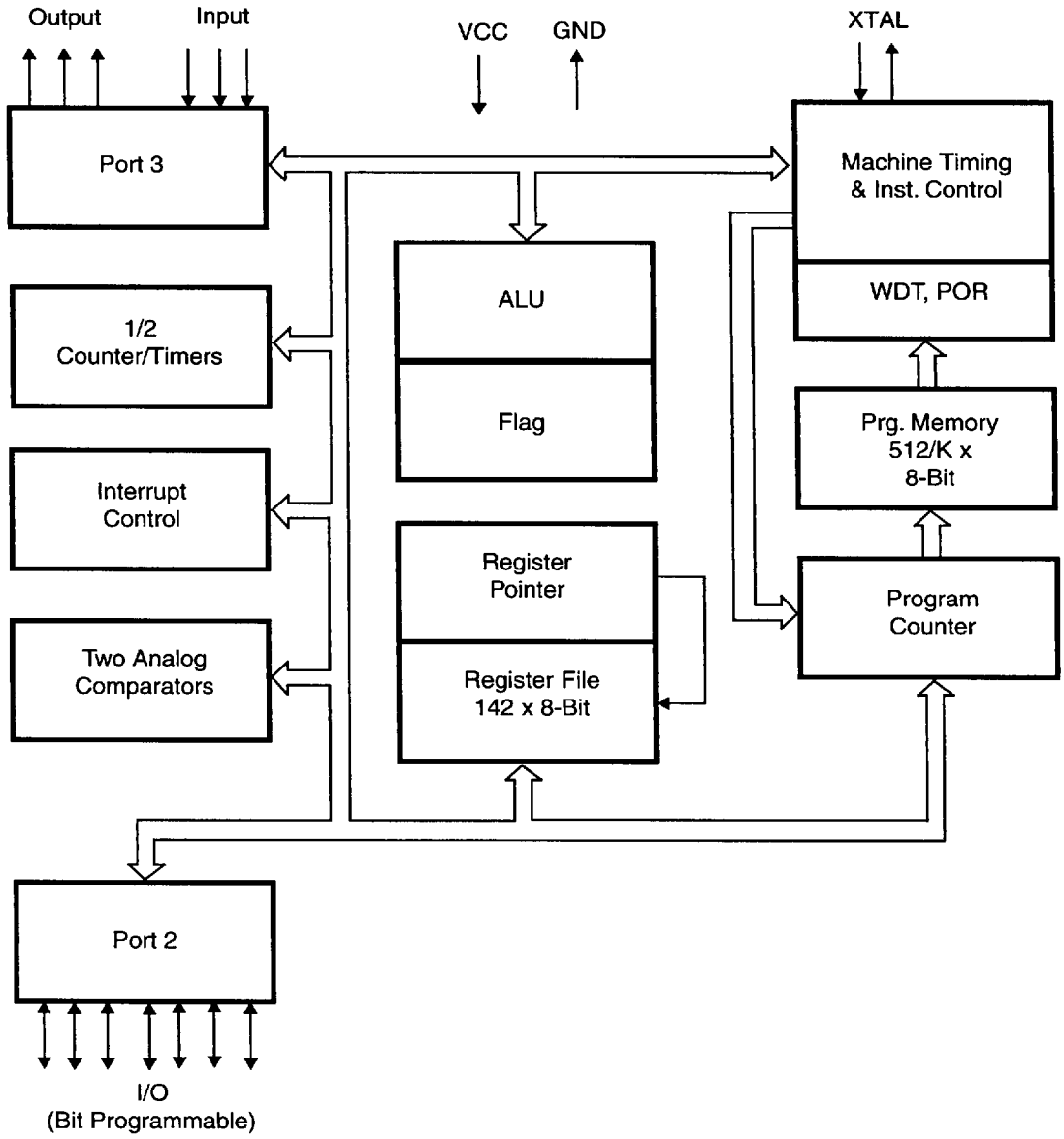


Figure 1. Functional Block Diagram

PIN DESCRIPTION

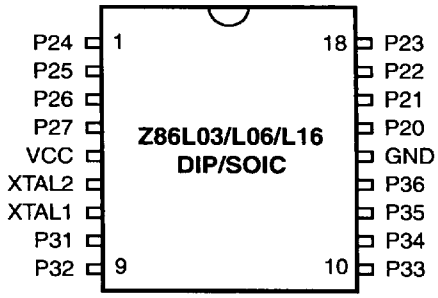


Figure 2. 18-Pin DIP/SOIC Configuration

Table 1. 18-Pin DIP/SOIC Pin Identification

No	Symbol	Function	Direction
1-4	P24-27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8-10	P31-33	Port 3, Pins 1, 2, 3	Fixed Input
11-13	P34-36	Port 3, Pins 4, 5, 6	Fixed Output
14	GND	Ground	
15-18	P20-23	Port 2, Pins 0, 1, 2, 3	In/Output

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	°C
T_A	Oper Ambient Temp	†		°C

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 3).

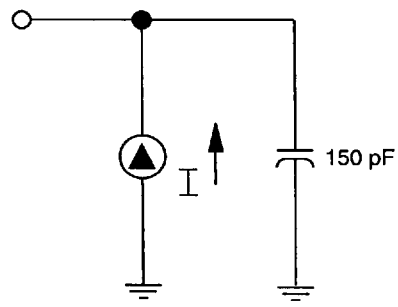


Figure 3. Test Load Configuration

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Max
Input Capacitance	12 pF
Output Capacitance	20 pF
I/O Capacitance	25 pF

DC ELECTRICAL CHARACTERISTICS
Z86L03/L06/L16

			T_A = 0°C to +70°C		Typical			
Sym	Parameter	V_{CC}	Min	Max	@ 25°C	Units	Conditions	Notes
	Max Input Voltage	2.0V	V_{SS} –0.3	V_{CC} +0.3		V		
		3.6V	V_{SS} –0.3	V_{CC}+0.3		V		
V_{CH}	Clock Input High Voltage	2.0V	0.9 V_{CC}	V_{CC} +0.3	0.9	V	Driven by External Clock Generator	
		3.6V	0.9 V_{CC}	V_{CC} +0.3	2.0	V		
V_{CL}	Clock Input Low Voltage	2.0V	V_{SS} –0.3	0.1 V_{CC}	0.9	V	Driven by External Clock Generator	
		3.6V	V_{SS} –0.3	0.1 V_{CC}	1.8	V		
V_{IH}	Input High Voltage Port 2	2.0V	0.9 V_{CC}	V_{CC} +0.3	1.2	V		
		3.6V	0.9 V_{CC}	V_{CC} +0.3	1.9	V		
V_{IH}	Input High Voltage Port 3	2.0V	0.7 V_{CC}	V_{CC} +0.3	0.9	V		
		3.6V	0.7 V_{CC}	V_{CC} +0.3	1.9	V		
V_{IL}	Input Low Voltage Port 2	2.0V	V_{SS} –0.3	0.1 V_{CC}	0.6	V		
		3.6V	V_{SS} –0.3	0.1 V_{CC}	1.2	V		
V_{IL}	Input Low Voltage Port 3	2.0V	V_{SS} –0.3	0.2 V_{CC}	0.9	V		
		3.6V	V_{SS} –0.3	0.2 V_{CC}	1.7	V		
V_{OH1}	Output High Voltage	2.0V	V_{CC} –0.4		1.9	V	I_{OH} = 500 µA	6
		3.6V	V_{CC} –0.4		3.5	V	I_{OH} = 500 µA	6
V_{OH}	Output High Voltage Low EMI Mode	2.0V	V_{CC} –0.4		1.9	V	I_{OH} = –125 µA	
		3.6V	V_{CC} –0.4		3.5	V	I_{OH} = –125 µA	
V_{OL}	Output Low Voltage Low EMI Mode	2.0V		0.4	0.1	V	I_{OL} = 250 µA	
		3.6V		0.4	0.04	V	I_{OL} = 250 µA	
V_{OL1}	Output Low Voltage	2.0V		0.4	0.1	V	I_{OL} = 1.0 mA	6
		3.6V		0.4	0.04	V	I_{OL} = 1.0 mA	6
V_{OL2}	Output Low Voltage	2.0V		1.0	0.5	V	I_{OL} = 3 mA,	6
		3.6V		1.0	0.3	V	3 Pin Max	6
V_{OFFSET}	Comparator Input	2.0V		25	6	mV		
		3.6V		25	6	mV		
I_{IL}	Input Leakage (Input bias current of comparator)	2.0V	–1.0	1.0	.001	µA	V_{IN} = O_V, V_{CC}	7
		3.6V	–1.0	1.0	.001	µA	V_{IN} = O_V, V_{CC}	7
I_{OL}	Output Leakage	2.0V	–1.0	1.0	.001	µA	V_{IN} = O_V, V_{CC}	
		3.6V	–1.0	1.0	.001	µA	V_{IN} = O_V, V_{CC}	
I_{CC}	Supply Current	2.0V		6	1.2	mA	@ 8 MHz	3,4,8,9
		3.6V		11.0	6	mA	@ 8 MHz	

Sym	Parameter	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current	2.0V	2.0	0.5	mA	HALT Mode $V_{IN} = O_V$,	3,4,8,9
		3.6V	4	1.5	mA	V_{CC} @ 8 MHz	
		2.0V	1.0	0.4	mA	Clock Divide by 16	3,4,8,9
		3.6V	3.0	1.0	mA	@ 8 MHz	3,4,8,9
I_{CC2}	Standby Current	2.0V	15	1.0	µA	STOP Mode $V_{IN} = O_V$,	5
		3.6V	15	3.0	µA	V_{CC} WDT is not Running ,	
		2.0V	115	30	µA	STOP Mode $V_{IN} = O_V$,	5,8
		3.6V	350	180	µA	V_{CC} WDT is Running	
V_{ICR}	Comparator Input Common Mode Voltage Range		V_{CC} –1.5V				

Notes:
1. $V_{SS} = 0_V$ = GND
2. V_{CC} range 3.6V to 2.0V
3. All outputs unloaded, I/O pins floating, inputs at rail.
4. CL1 = CL2 = 47 pF
5. Same as note [4] except inputs at V_{CC}
6. STD MODE (not low noise)
7. Input bias currents for comparator inputs P31, P32, P33.
8. Internal on-board RC is driving WDT.
9. System clock is external XTAL frequency divided by 2.

AC ELECTRICAL CHARACTERISTICS

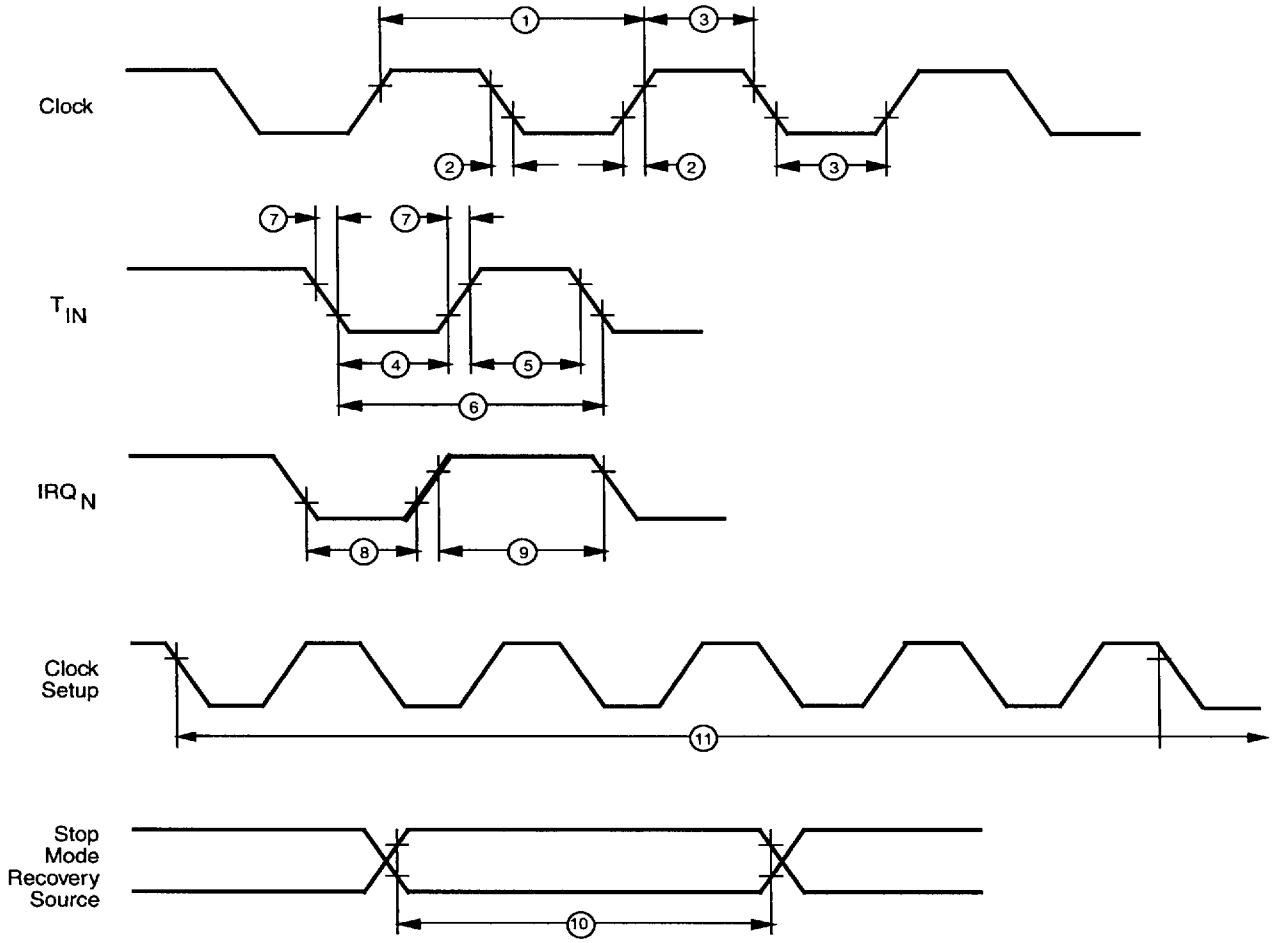


Figure 4. Additional Timing

AC CHARACTERISTICS

Additional Timing Table
(Divide-By-One Mode, SCLK/TCLK = EXTERNAL)

				T_A = 0°C to +70°C			
No	Symbol	Parameter	V_{CC}	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	ns	1,7,8
			5.5V	250	DC	ns	1,7,8
2	TrC, TfC	Clock Input Rise and	3.0V		25	ns	1,7,8
		Fall Times	5.5V		25	ns	1,7,8
3	TwC	Input Clock Width	3.0V	125		ns	1,7,8
			5.5V	124		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.0V	100		ns	1,7,8
			5.5V	70		ns	1,7,8
5	TwTinH	Timer Input High Width	3.0V	3TpC			1,7,8
			5.5V	3TpC			1,7,8
6	TpTin	Timer Input Period	3.0V	4TpC			1,7,8
			5.5V	4Tpc			1,7,8
7	TrTin,TfTin	Timer Input Rise and	3.0V		100	ns	1,7,8
		Fall Timer	5.5V		100	ns	1,7,8
8	TwIL	Int. Request Low Time	3.0V	100		ns	1,2,7,8
			5.5V	70		ns	1,7,8
9	TwIH	Int. Request Input	3.0V	3TpC			1,2,7,8
		High Time	5.5V	3TpC			1,2,7,8
10	Twsm	Stop-Mode Recovery	3.0V	12		ns	4,8
		Width Spec	5.5V	12		ns	4,8
11	Tost	Oscillator Startup Time	3.0V		5TpC		3,8,9
			5.5V		5TpC		3,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P33-P31).
3. SMR-D5=0.
4. SMR-D5=1, POR STOP mode delay is on.
5. Reg. WDTMR
6. SMR D1=1.
7. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
8. For RC and LC oscillator driven by clock driver.

AC CHARACTERISTICS

Additional Timing Table

No	Symbol	Parameter	V_{CC}	T_A =0°C to70°C 8 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	2.0V	125	DC	ns	1,7
			3.6V	125	DC	ns	1,7
2	TrC,TfC	Clock Input Rise	2.0V		25	ns	1
		and Fall Times	3.6V		25	ns	1
3	TwC	Input Clock Width	2.0V	62		ns	1, 7
			3.6V	62		ns	1, 7
4	TwTinL	Timer Input Low	2.0V	250		ns	1,7
		Width	3.6V	250		ns	1,7
5	TwTinH	Timer Input High	2.0V	5TpC			1, 7
		Width	3.6V	5TpC			1,7
6	TpTin	Timer Input Period	2.0V	8TpC			1,7
			3.6V	8TpC			1,7
7	TrTin,	Timer Input Rise	2.0V		100	ns	1
	TtTin	and Fall Timer	3.6V		100	ns	1
8	TwIL	Int. Request Input	2.0V	100		ns	1,2
		Low Time	3.6V	70		ns	1,2
9	TwIH	Int. Request Input	2.0V	5TpC			1,2,7
		High Time	3.6V	5TpC			1,2,7
10	Twsm	Stop-Mode	2.0V	70		ns	
		Recovery Width	3.6V	70		ns	
		Spec					
11	Tost	Oscillator Start-up	2.0V	5TpC			4,7,8
		Time	3.6V	5TpC			
12	Twdt	Watch-Dog Timer	2.0V	30	150	ms	5
		Refresh Time	3.6V	10	40	ms	D0 = 0 6
							D0 = 0 6
			2.0V	60	300	ms	D0 = 1 6
			3.6V	20	80	ms	D1 = 0 6
			2.0V	120	600	ms	D0 = 0 6
			3.6V	40	160	ms	D1 = 1 6
			2.0V	480	2400	ms	D0 = 1 6
			3.6V	160	610	ms	D1 = 1 6
13	T_{POR}	Power On Reset	2.0V	15	75	ms	5
		Time	3.6V	4	20	ms	D0 = 0 6

Notes:

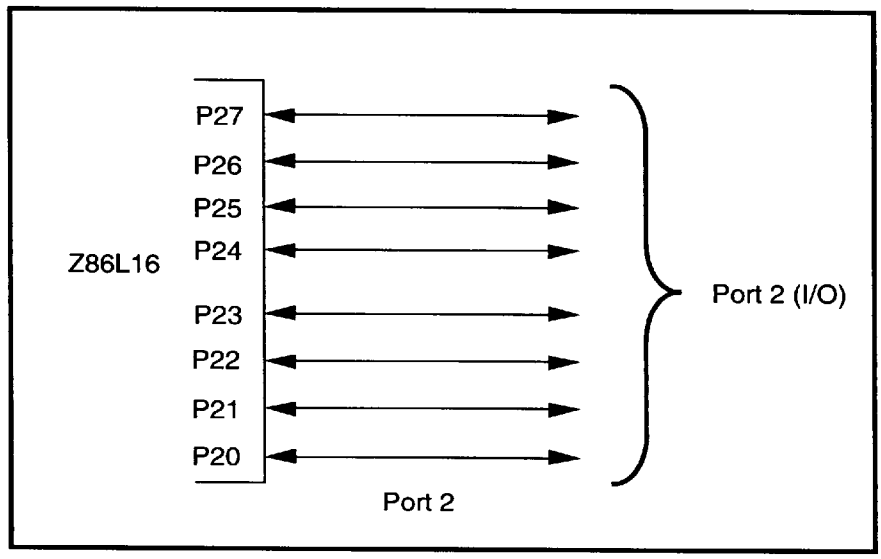
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. SMR-D5 = 0
4. Reg. WDTMR
5. Internal RC Oscillator only.
6. System clock is XTAL frequency divided by 2. (SMR Bit D1=0)
7. Driving XTAL with clock driver.

PIN FUNCTIONS

XTAL1. Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open drain (Figure 5). Low EMI output buffers can be globally programmed by the software.



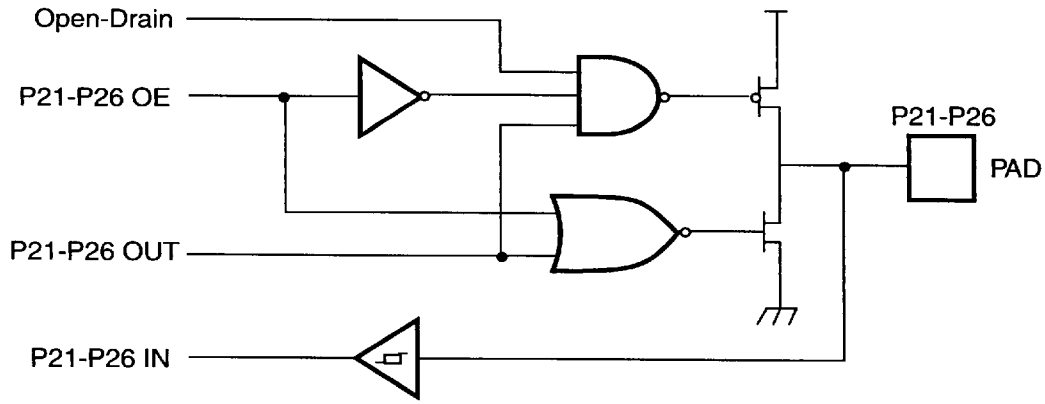


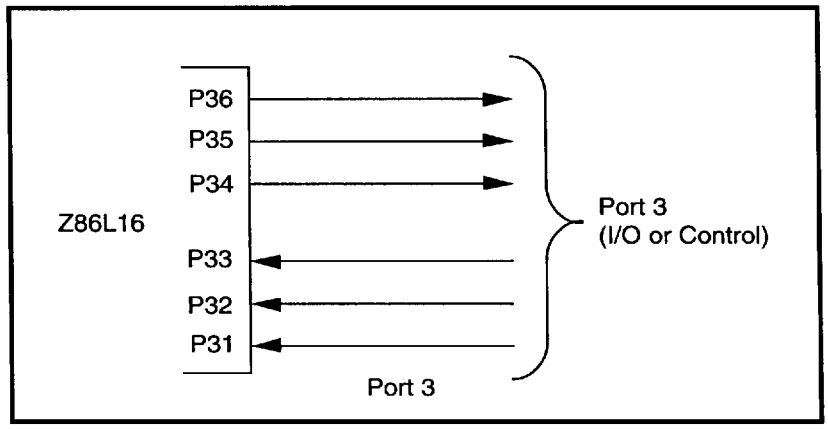
Figure 5. Port 2 Configuration

Port 3 (P36-P31). Port 3 is a 6-bit, CMOS compatible port. These six lines consist of three fixed inputs (P31-P33) and three fixed outputs (P34-P36). Pins P31, P32, and P33 are standard CMOS inputs and pins P34, P35, and P36 are push-pull outputs. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M bit D1). Pins P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input when the analog mode is selected. P33 is a falling edge interrupt input only.

Note: P33 is available as an interrupt input only in the digital mode. P31 and P32 are valid interrupt inputs and P31 is the T_{IN} input when the analog or digital input mode is selected.

The outputs from the analog comparator can be globally programmed to output from P34 and P35 by setting PCON (F) 00 bit D0 = 1.

Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}).



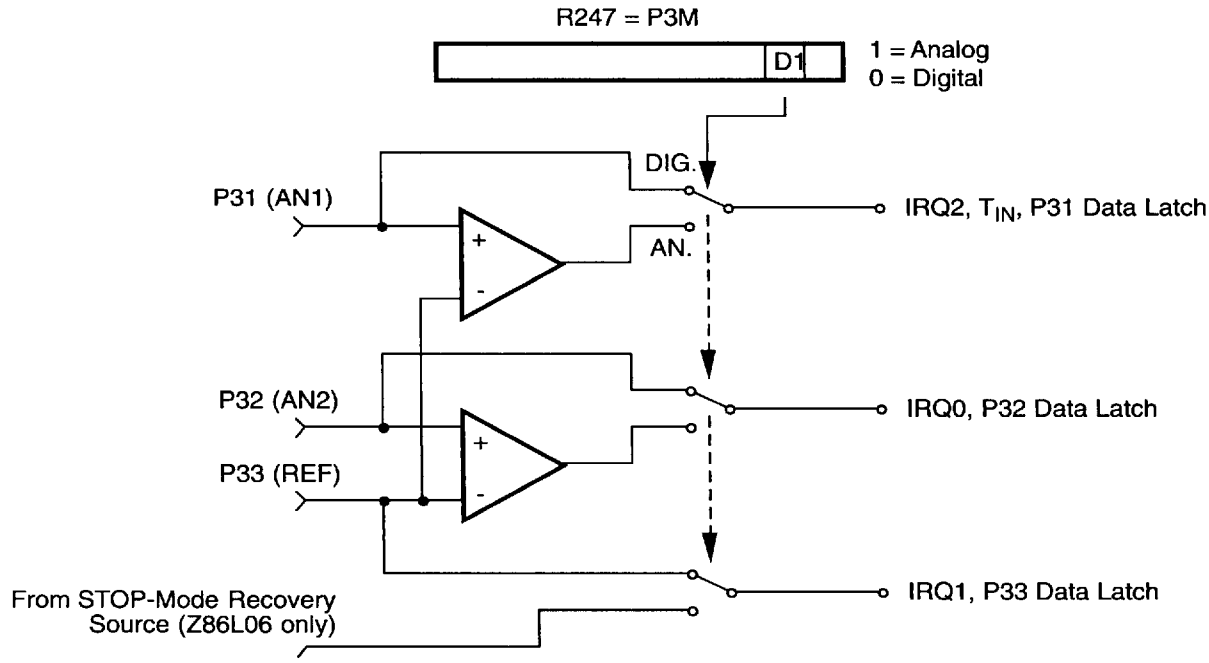


Figure 6. Port 3 Configuration

FUNCTIONAL DESCRIPTION

Low EMI Emission. The Z86L03/L06/L16 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

1. The pre-drivers slew rate reduced to 10 ns (typical).
2. Low EMI output drivers resistance of 200 ohms (typical).
3. Low EMI Oscillator.
4. Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz (250 ns cycle time) when the low EMI oscillator is selected and SCLK = External (SMR Register Bit D1=1).

Comparator Inputs. Port 3 Pin P31 and P32 each have a comparator front end. The comparator reference voltage pin P33 is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators, and P33 is the reference voltage supplied to both comparators. In digital mode, Pin P33 can be used as a P33 register input or IRQ1 source.

RESET. The device is reset in one of the following conditions:

1. Power-On Reset
2. Watch-Dog Timer
3. Stop-Mode Recovery Source
4. Low Voltage Protection

Having the Auto Power-On Reset circuitry built-in, the Z86L03/06 does not require an external reset circuit. The reset time is 5 ms (typical) plus 18 clock cycles.

The device does not re-initialize the WDTMR, SMR, P2M, or P3M registers to their reset values on a Stop-Mode Recovery operation.

Program Memory. Z86L03/06 can address up to 512/1K bytes of internal program memory (Figure 7). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Byte 13 to byte 511/1023 consists of on-chip, user program mask ROM.

ROM Protect. The 512/1K bytes of Program Memory is mask programmable. A ROM protect feature will prevent "dumping" of the ROM contents by inhibiting execution of the LDC and LDCI instructions to program memory in all modes.

ROM protect is mask-programmable. It is selected by the customer when the ROM code is submitted. Selecting ROM protect disables the LDC and LDCI instructions in all modes. ROM lookup tables are not supported in this mode.

Expanded Register File. The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 8). These register groups are known as the Expanded Register File (ERF).

Bits 3-0 of the Register Pointer (RP) select the active ERF group. Bits 7-4 of register RP select the working register group (Figure 9). For the Z86L03, three system configuration registers reside in the ERF address space Bank F. For the Z86L06, three system configuration registers reside in the ERF address space Bank F. The rest of the Expanded Register File address space is not physically implemented and is open for future expansion.

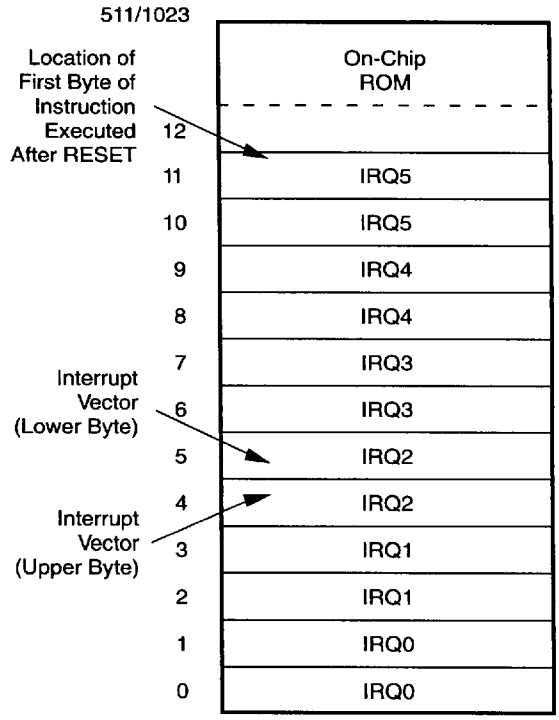


Figure 7. Program Memory Map

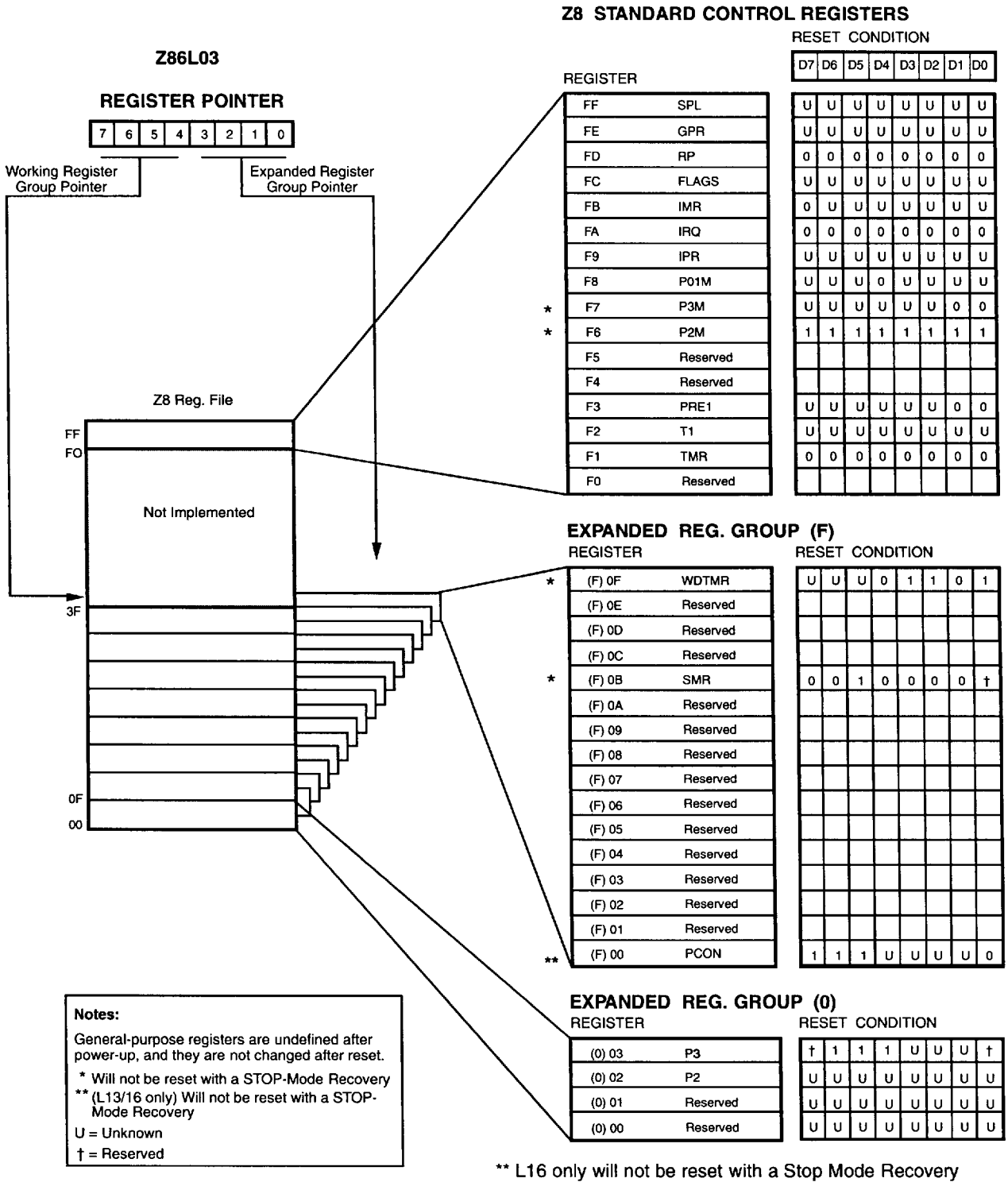


Figure 8. Expanded Register File Architecture

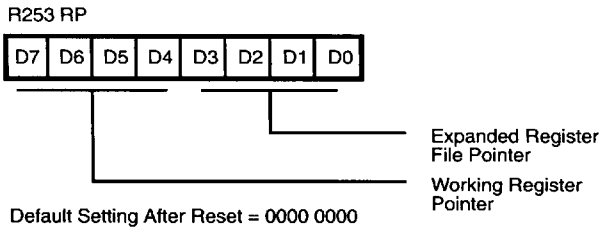


Figure 9. Register Pointer

Register File. The Register File consists of two I/O port registers, 60/124 general-purpose registers, and 13/15 control and status registers. The Z86L03 General-Purpose Register file ranges from address 00 to 3F while the Z86L06/L16 General-Purpose Register file ranges from address 00 to 7F (see Figure 8). The instructions can access registers directly or indirectly via an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 10). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range.

Note: Register R254 has been designated as a general-purpose register.

Stack. An 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60/124 general-purpose registers.

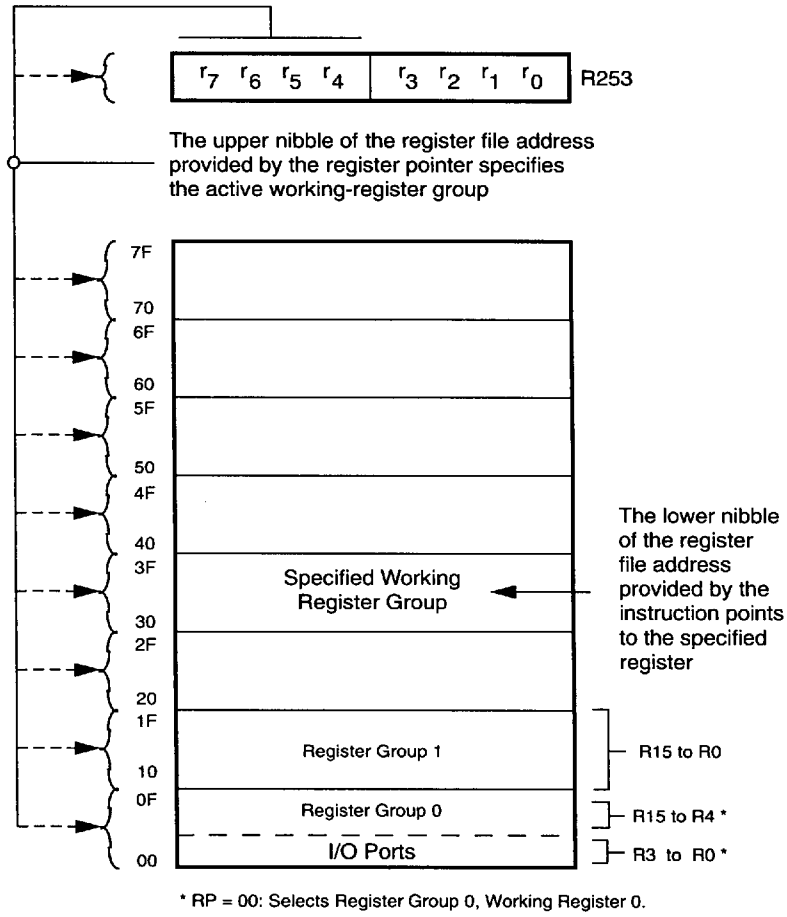


Figure 10. Register Pointer

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler (Z86L03 only has T1). The T1 prescaler can be driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 11).

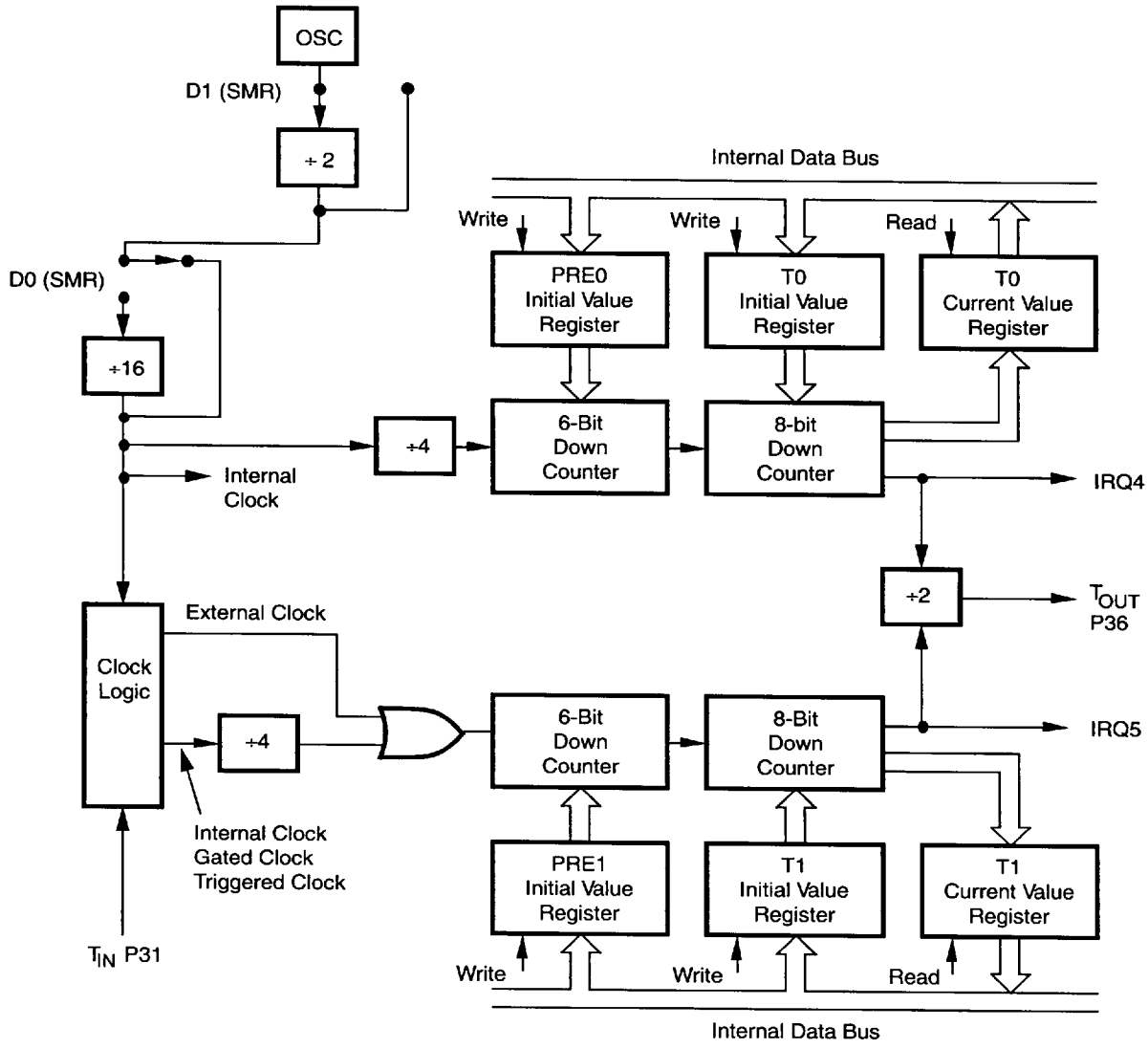


Figure 11. Counter/Timer Block Diagram

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request—IRQ4 (T0) or IRQ5 (T1), is generated. Note that IRQ4 is software-generated in the Z86L03.

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36 serves as a timer output (T_{OUT}) through which T0 (L06 only), T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1 (L06 only). The TIN mode is enabled by setting PRE1 bit D1 (R243) to 0.

Interrupts. The Z86L03/06 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 12). The six sources are divided as follows; three sources are claimed by Port 3 lines P31-P33, two sources in the counter/timers, and one source for the SPI. The Interrupt Mask Register globally or singularly enables or disables the six interrupt requests (Table 2).

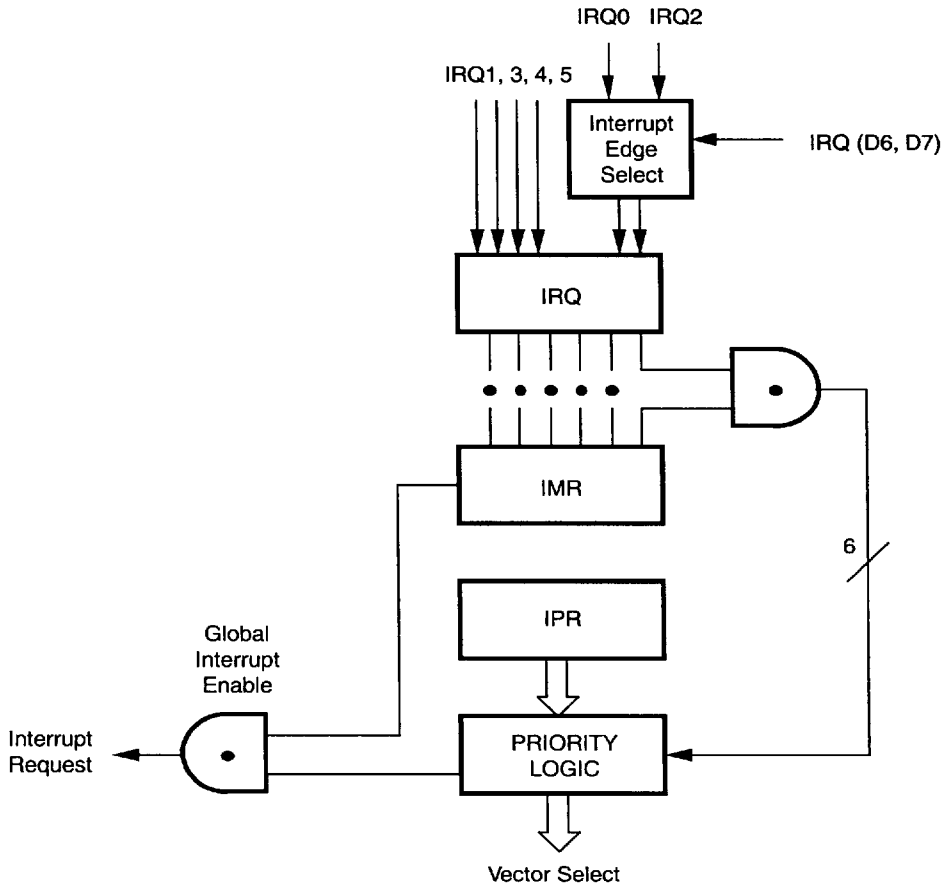


Figure 12. Interrupt Block Diagram

Table 2. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	IRQ2, T_{IN}	4,5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	Software Generated
IRQ4	T0/IRQ 4	8, 9	Internal for L06 and Software Generated for L03
IRQ5	TI	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86L03/06 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service. IRQ3 has no hardware source, but can be invoked by software (write to IRQ3 Register).

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

The programming bits for the Interrupt Edge Select are located in the IRQ register (R250), bits D7 and D6. The configuration is shown in Table 3.

Table 3. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z86L03/06 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 8 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to the device Ground (pin 14). The layout is important to reduce ground noise injection.

The RC oscillator option is mask-programmable, to be selected by the customer at the time ROM code is submitted. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 14).

In addition, a special feature has been incorporated into the Z86L03/06; in low EMI noise mode (bit 7 of PCON register=0) with the RC option selected, the oscillator is targeted to consume considerately less ICC current at frequencies of 10 kHz or less.

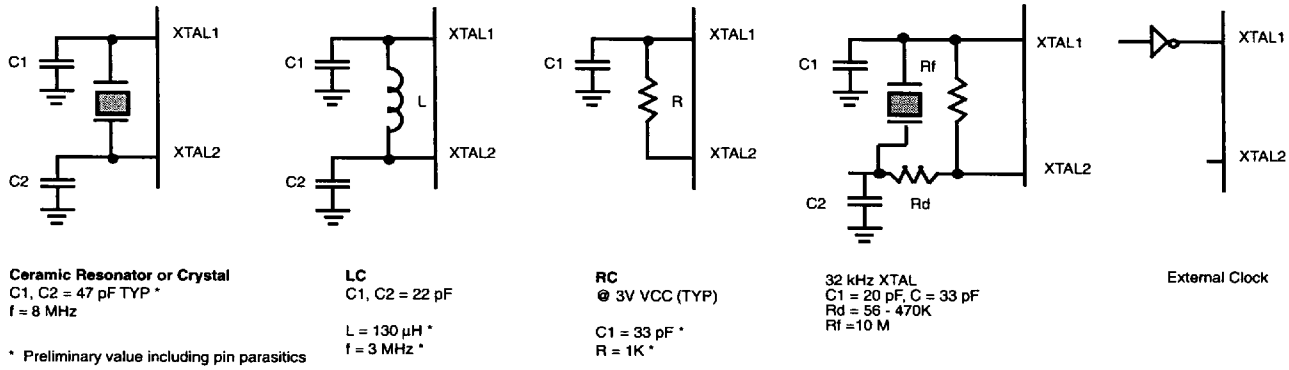


Figure 13. Oscillator Configuration

Power-On Reset. A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the three conditions:

1. Power-Fail to Power-OK Status
2. Stop-Mode Recovery (If D5 of SMR=1)
3. WDT Time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. The Halt instruction will turn off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device may be recovered by interrupts either externally or internally generated. The global interrupts must be enabled.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current. The STOP mode is terminated by a RESET (WDT time-out, POR, or SMR recovery). This causes the processor to restart the application program at address 000C (HEX). Note, the crystal remains active in STOP mode if bits 3 and 4 of the WDTMR are enabled. In this mode, only the Watch-Dog Timer runs in STOP mode.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF      NOP     ;clear the pipeline
6F      STOP    ;enter STOP mode
            or
FF      NOP     ;clear the pipeline
7F      HALT    ;enter HALT mode
```

PORT Configuration Register (PCON). The PCON configures the ports individually for comparator output on Port 3, low EMI noise on Ports 2 and 3, and low EMI noise oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 15).

Comparator Output Port 3 (D0). Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34, and P35 and a 0 releases the Port to its standard I/O configuration.

Bits D4-D1. These bits are reserved and must be 1.

Low EMI Port 2 (D5). Port 2 is configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting D5=1. The default value is 1.

Low EMI Port 3 (D6). Port 3 is configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting D6=1. The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive. While a 0 configures the oscillator with low noise drive, it does not affect the relationship of SCLK and XTAL.

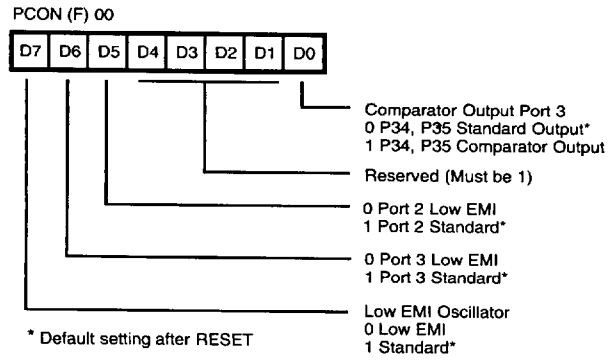


Figure 14. Port Configuration Register (PCON) (Write Only)

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figures 15 and 16). All bits are Write Only except bit 7, which is Read Only. Bit 7 is a flag bit that is hardware set on the condition of a STOP recovery and reset on a power-on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR specify the source of the Stop-Mode Recovery signal. Bit 1 determines whether the XTAL is divided by 1 or 2. A 0 in this location uses XTAL divide-by-two, and a 1 uses XTAL. The default for this bit is XTAL divide by two. Bit 0 controls the divide-by-16 prescaler of SCLK/TCLK. The SMR is located in bank F of the Expanded Register Group at address 0BH.

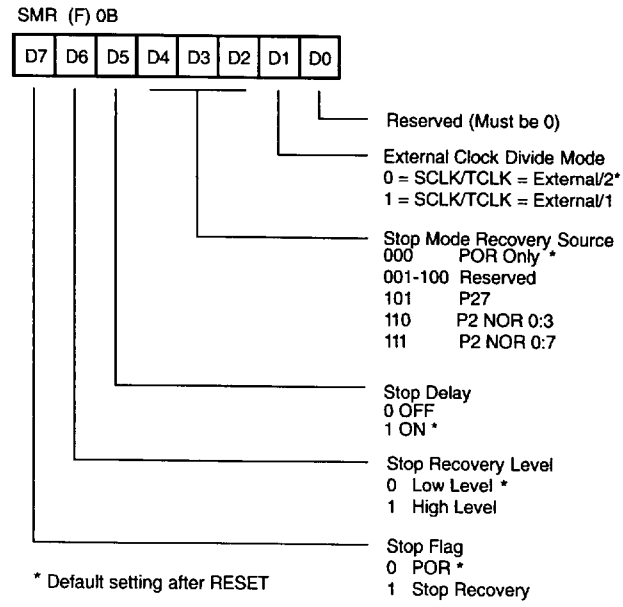


Figure 15. Stop-Mode Recovery Register (Write Only except D7, which is Read Only.) (Z86L03/L16)

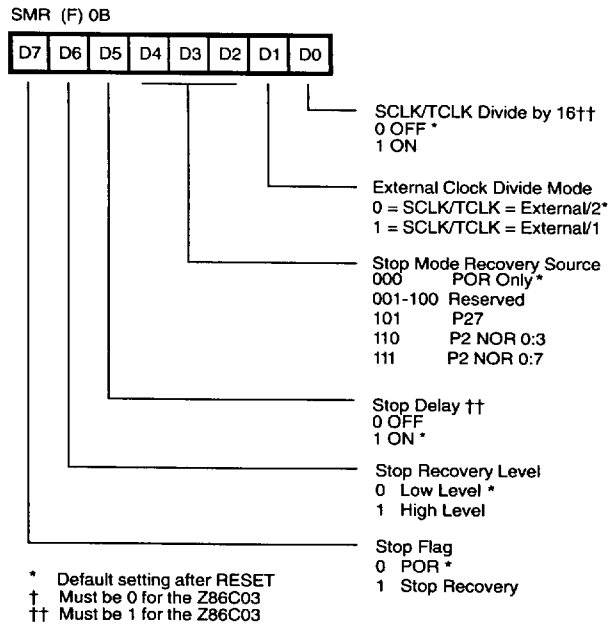


Figure 16. Stop-Mode Recovery Register (Write Only except bit D7, which Is Read Only.) (Z86L06/16)

SCLK/TCLK Divide-by-16 Select (D0)—Z86L06 Only. D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources the counter/timers and interrupt logic). After Stop-Mode Recovery, this bit is reset to 0 (off).

External Clock Divide Mode (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, SCLK (System Clock) and TCLK (Timer Clock) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit, together with D7 of PCON, helps further lower EMI [i.e., D7 (PCON)=0, D1 (SMR=1]. The default setting is 0. Max XTAL frequency is 4 MHz when oscillator divide by two circuitry is eliminated (XTAL=SCLK).

Stop-Mode Recovery Source (D2,D3,D4). These three bits of the SMR specify the wake-up source of the Stop-Mode Recovery (Table 4 and Figures 17 and 18).

Table 4. Stop-Mode Recovery Source

SMR			Operation
D4	D3	D2	Description of Action
0	0	0	POR recovery only
0	0	1	POR recovery only (L03=Reserved)
0	1	0	P31 transition (L03 =Reserved)
0	1	1	P32 transition (L03 =Reserved)
1	0	0	P33 transition (L03 =Reserved)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0:3
1	1	1	Logical NOR of Port 2 bits 0:7

P31-P33 cannot wake up from STOP Mode if the input lines are configured as analog inputs. Note: Stop-Mode Recovery sources have to be active level Low (bit D6 in SMR set to 0 if P31, P32, P33, and P27 selected, or bit D6 in SMR set to 1 if logical NOR of Port 2 is selected).

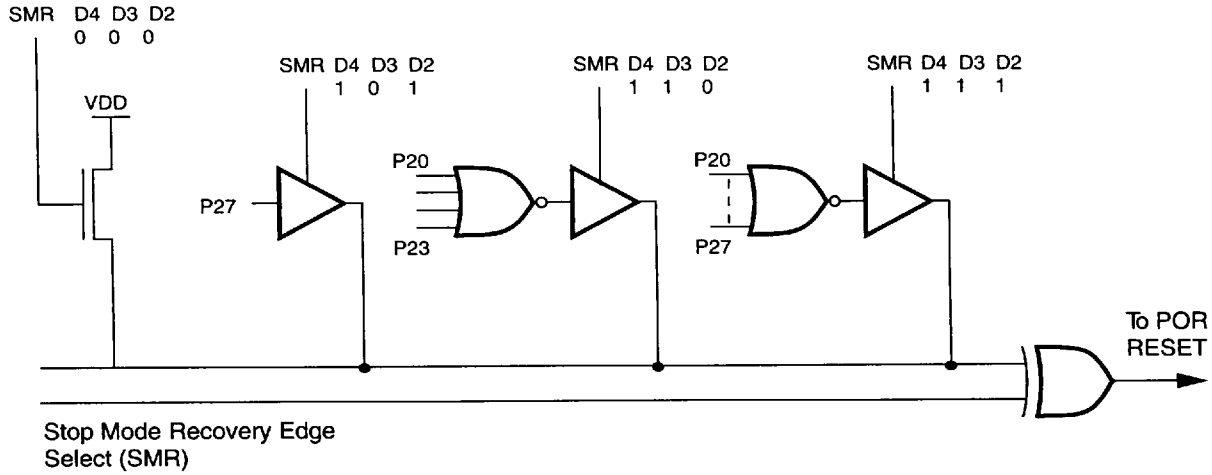


Figure 17. STOP-Mode Recovery Source (Z86L03)

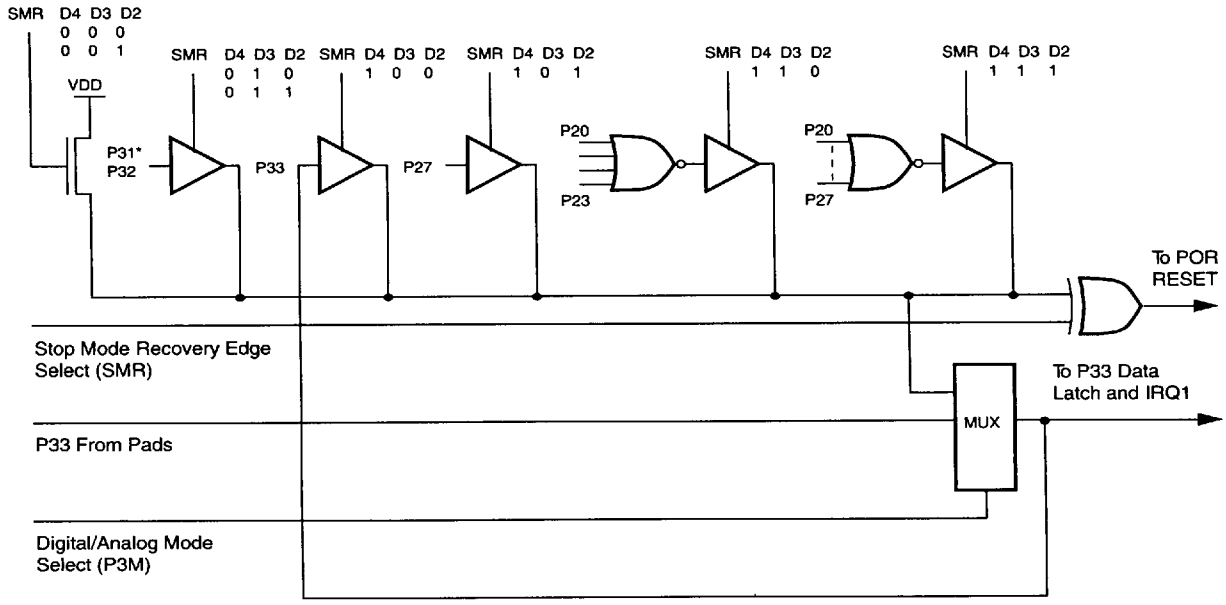


Figure 18. Stop-Mode Recovery Source (Z86L06/16)

Stop-Mode Recovery Delay Select (D5). This bit disables the 5 ms RESET delay after Stop-Mode Recovery. The default condition of this bit is 1. If the "fast" wake-up is selected, the Stop-Mode Recovery source needs to be kept active for at least 5 TpC.

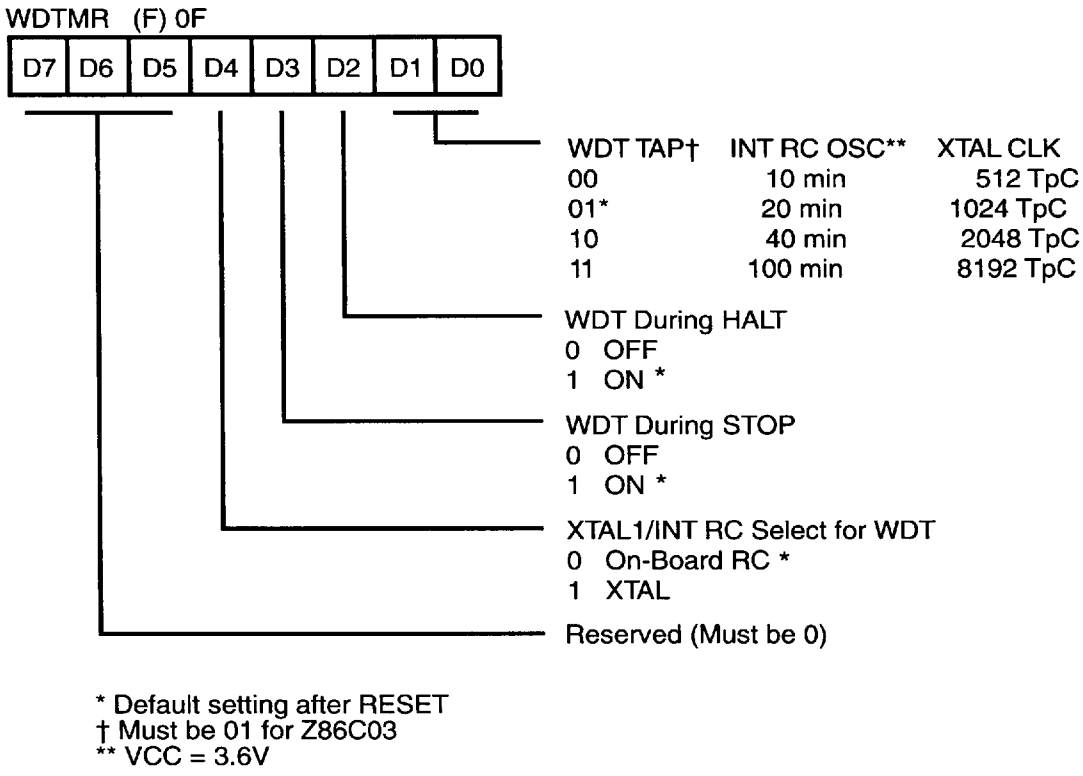
Stop-Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the device from STOP Mode. A 0 indicates low level recovery. The default is 0 on POR (Figures 17 and 18).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. It is active High, and is 0 (cold) on POR/WDT RESET. This bit is Read Only. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled after it has been initially enabled. The WDT circuit is driven by an on-board RC oscillator or external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDTMR register.

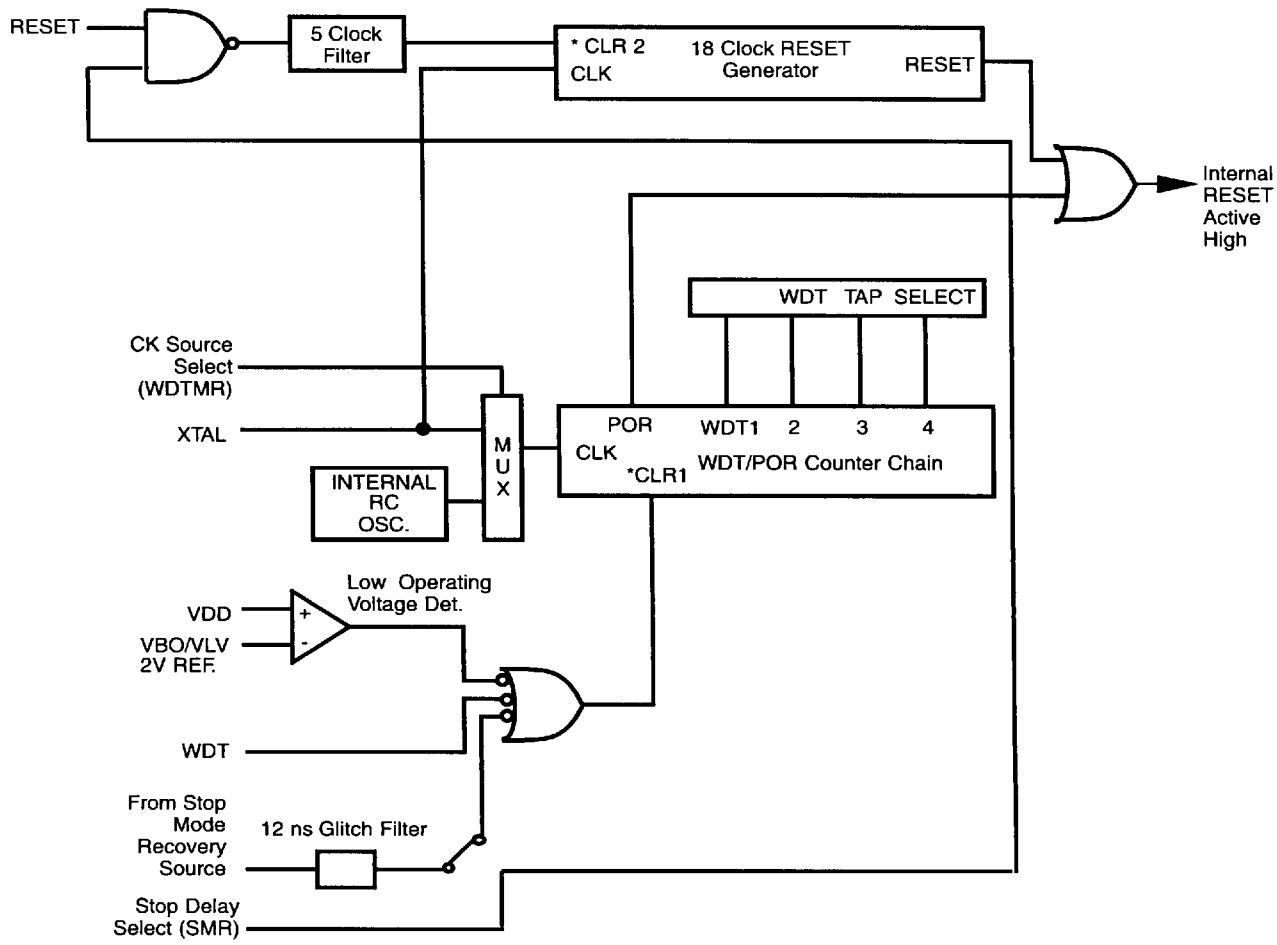
Note: Execution of the WDT instruction affects the Z (zero), S (sign), and V (overflow) flags.

Bits 0 and 1 of the WDTMR register control a tap circuit that determines the time-out period (on Z86L06 only). Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to 1, the WDT is only driven by the external clock during STOP mode. This feature makes it possible to wake-up from STOP mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 20). This register is accessible only during the first 64 processor cycles (64 SCLKs) from the execution of the first instruction after Power-On Reset, Watch-Dog Reset or a Stop-Mode Recovery (Figure 21). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location 0FH. It is organized as follows:



* Default setting after RESET
† Must be 01 for Z86C03
** VCC = 3.6V

Figure 19. Watch-Dog Timer Mode Register (Write Only)



* /CLR1 and /CLR2 enable the WDT/POR and 18 Clock Reset timers upon a Low to High input translation.

Figure 20. Resets and WDT

WDT Time Select (D1, D0). Bits 0 and 1 control a tap circuit that determines the time-out period. Table 5 shows the different values that can be obtained. The default value of D0 and D1 are 1 and 0, respectively. These select bits are present in the Z86L06 only.

Table 5. Time-Out Period of the WDT (Z86L06)

D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	10 ms min	512TpC
0	1	20 ms min	1024TpC
1	0	40 ms min	2098TpC
1	1	160 ms min	8192TpC

Notes:
1. TpC = XTAL clock cycle
2. The default on reset is 20 ms, D0 = 1 and D1 = 0.
3. The values given are for V_{CC} = 3.6V
4. For the Z86L03, the WDT time-out value is fixed at 1024 TpC (depending on WDTMR bit D4) period. When writing to the WDTMR in the Z86L03, bit D0 must be 1 and D1 must be 0.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Since XTAL clock is stopped during STOP Mode, unless as specified below, the on-board RC has to be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1. If bits D3 and D4 are both set to 1, only the WDT is driven by the external clock during STOP mode.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the internal RC oscillator.

Bits 5, 6 and 7. These bits are reserved.

V_{CC} Voltage Comparator. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below the specified voltage.

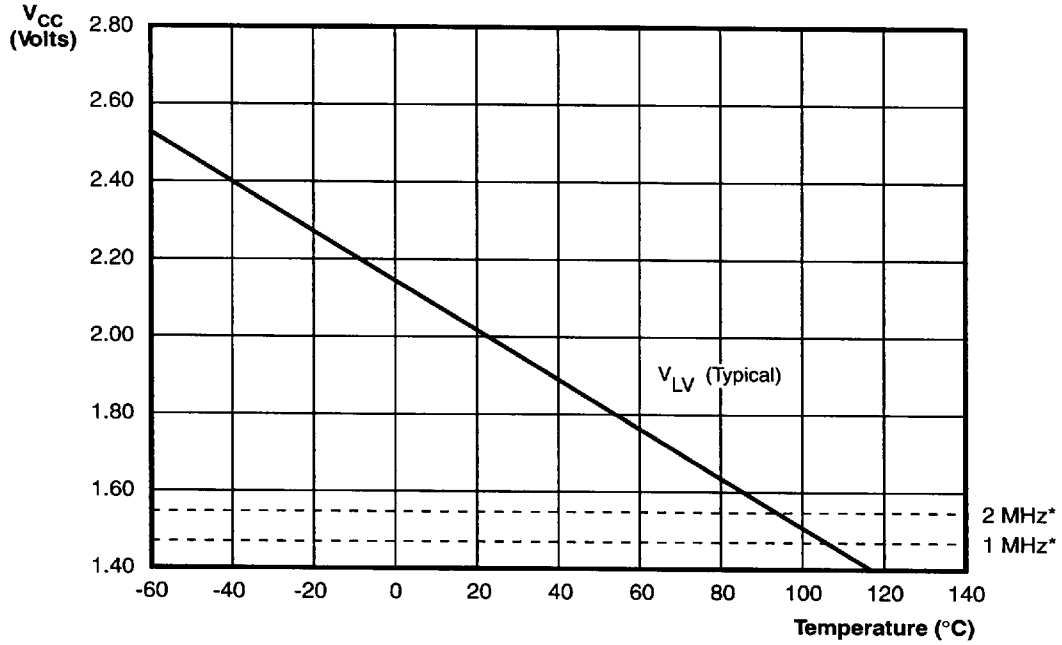
Low Voltage Protection (V_{LV}). The Low Voltage Protection trip point (V_{LV}) will be less than 2 volts and above 1.4 volts under the following conditions.

Maximum (V_{LV}) Conditions:

T_A = -40° to +85°C, Internal Clock (SCLK)
Frequency equal or less than 2 MHz

Note: The internal clock frequency (SCLK) is determined by SMR (F) OBH bit D1.

The device functions normally at or above 2.0V under all conditions. Below 2.0V, the device is guaranteed to function normally until the Low Voltage Protection trip point (V_{LV}) is reached. The actual low voltage trip point is a function of temperature and process parameters (Figure 22).



Note: * The typical minimum operating Vcc voltage at that frequency.

Figure 21. Typical Z86L03/L06/L16 V_{LV} Voltage vs Temperature

EXPANDED REGISTER FILE CONTROL REGISTERS

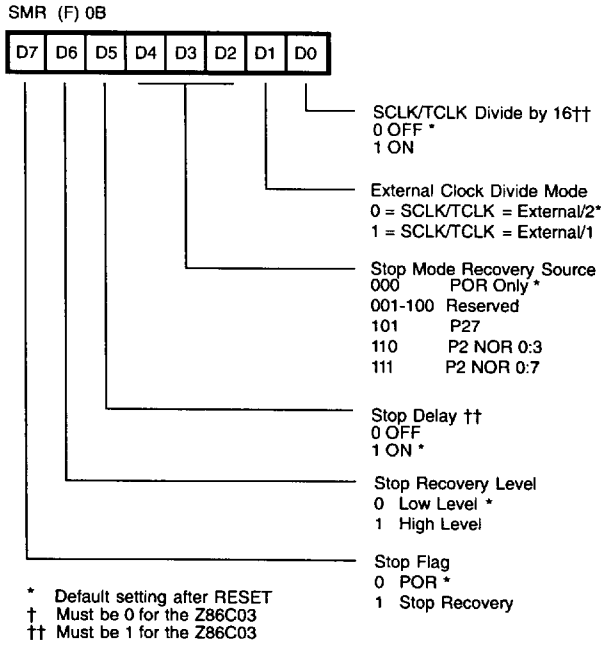


Figure 22. Stop-Mode Recovery Register (Write Only except bit D7, which is Read Only)

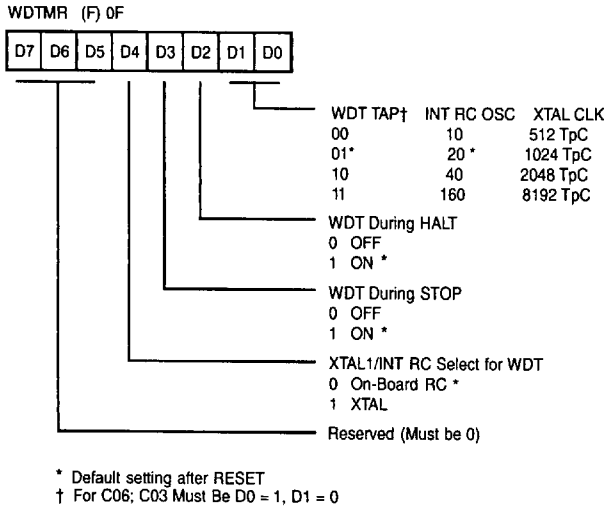


Figure 23. Watch-Dog Timer Mode Register (Write Only)

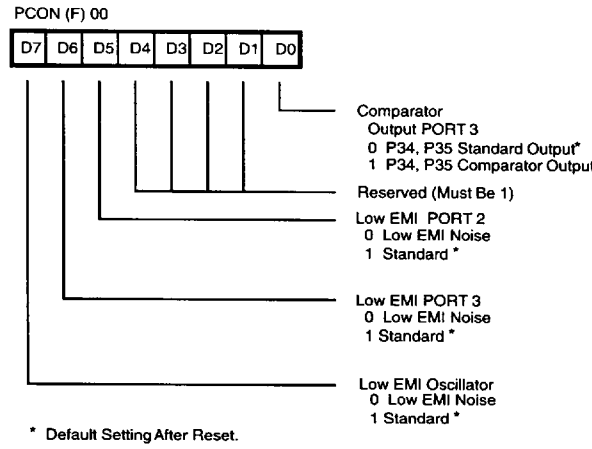


Figure 24. PORT Control Register (Write Only)

Z8® CONTROL REGISTER DIAGRAMS

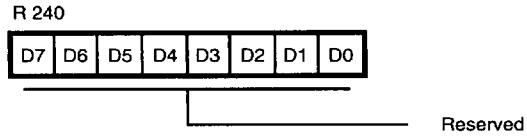


Figure 25. Reserved

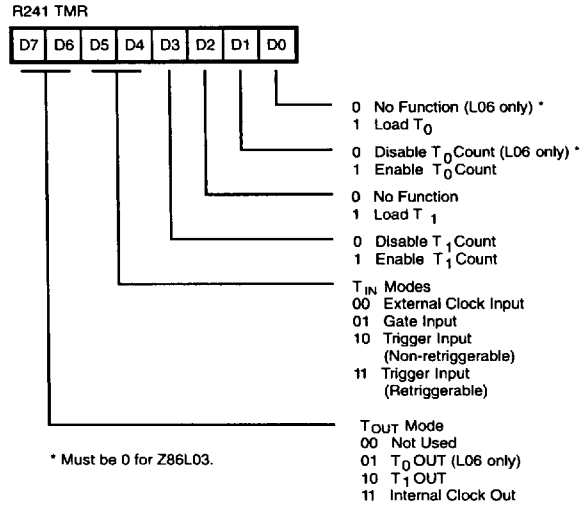


Figure 26. Timer Mode Register (F1H: Read/Write)

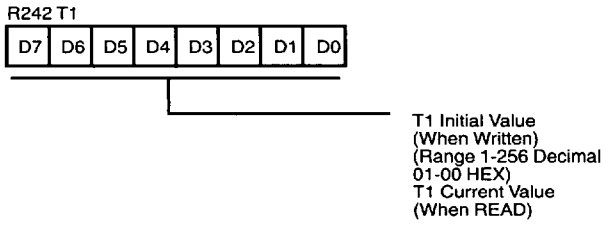


Figure 27. Counter Timer 1 Register (F2H: Read/Write)

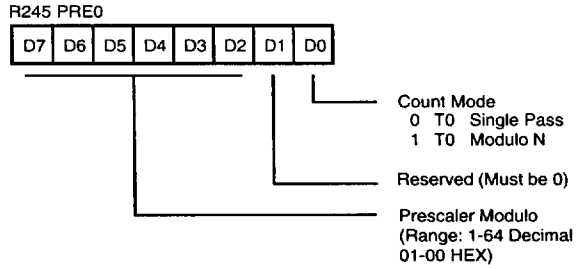


Figure 28. Prescaler 1 Register (F3H: Write Only)

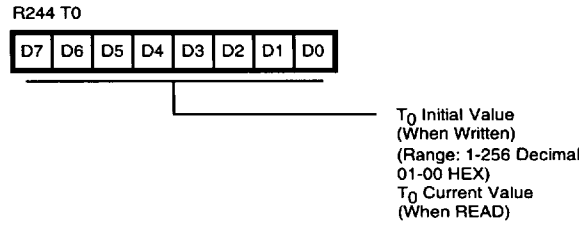


Figure 29. Counter/Timer 0 Register (F4H: Read/Write; Z86L06 Only)

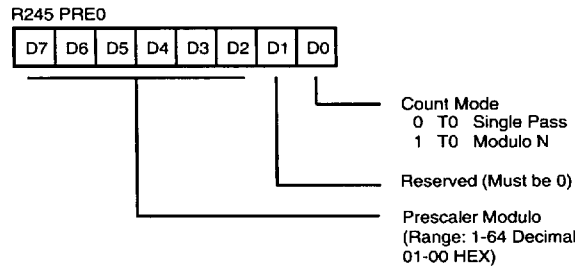


Figure 30. Prescaler 0 Register (F5H: Write Only; Z86L06 Only)

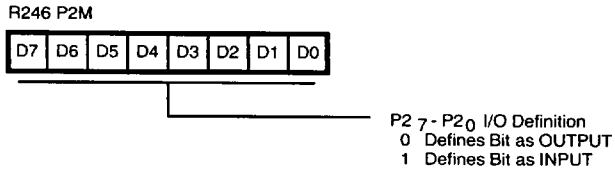


Figure 31. Port 2 Mode Register (F6H: Write Only)

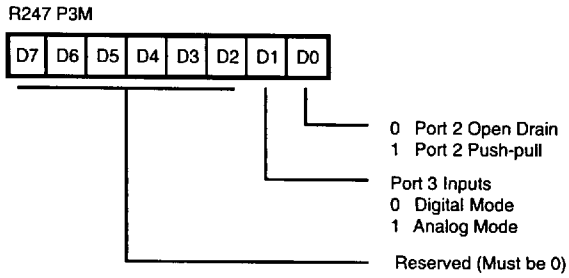


Figure 32. Port 3 Mode Register (F7H: Write Only)

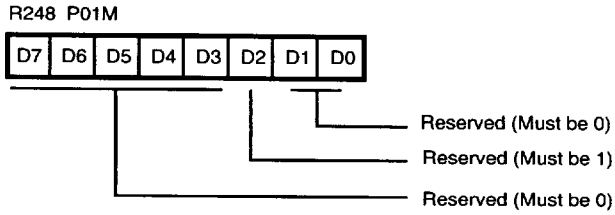


Figure 33. Port 0 and 1 Mode Register (F8H: Write Only)

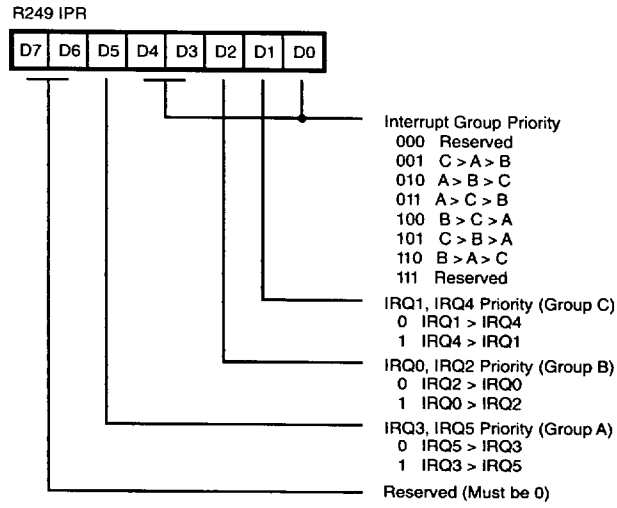


Figure 34. Interrupt Priority Register (F9H: Write Only)

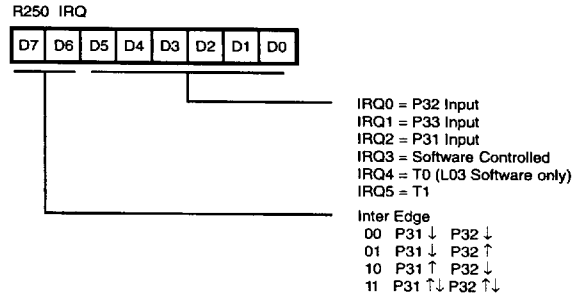


Figure 35. Interrupt Request Register (FAH: Read/Write)

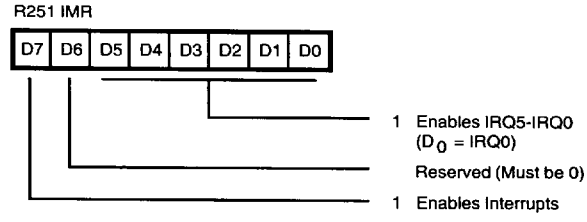


Figure 36. Interrupt Mask Register (FBH: Read/Write)

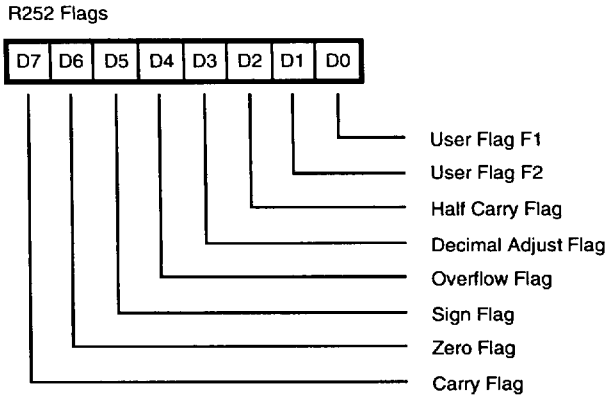


Figure 37. Flag Register (FCH: Read/Write)

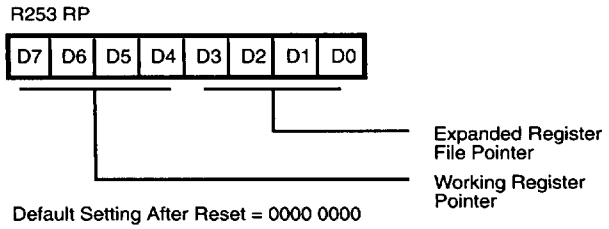


Figure 38. Register Pointer (FDH: Read/Write)

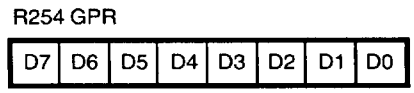


Figure 39. General-Purpose Register

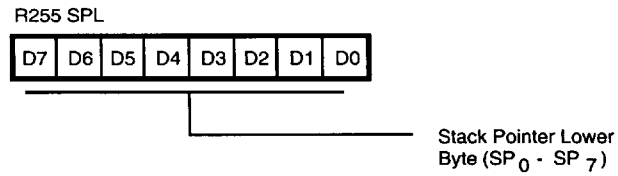
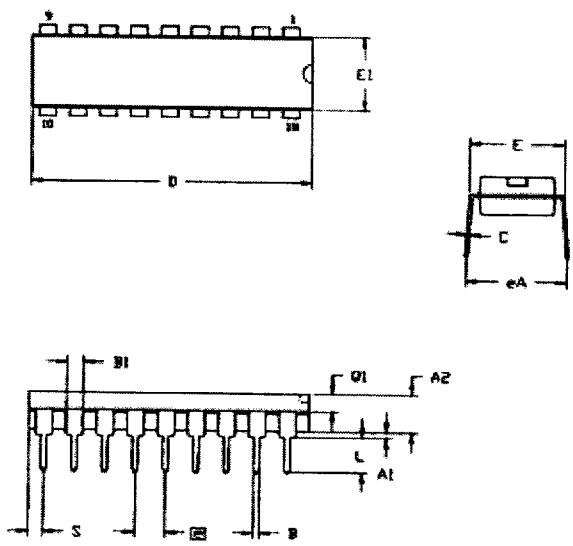


Figure 40. Stack Pointer (FFH: Read/Write)

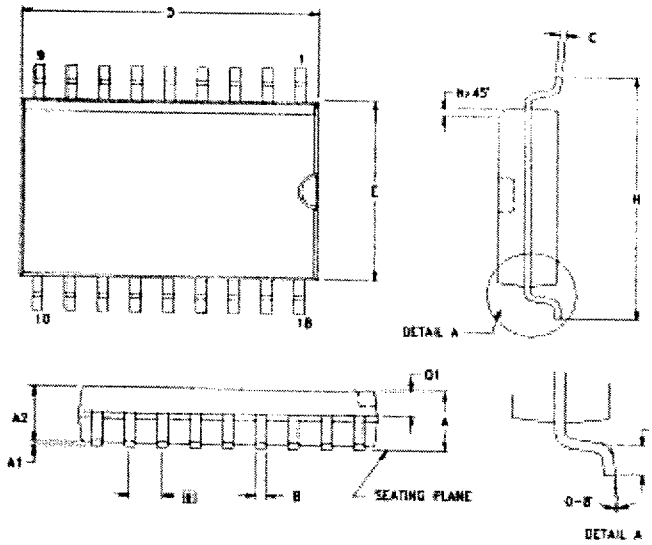
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	128	135
B	0.38	0.53	.015	021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	015
D	22.35	23.37	880	920
E	7.62	8.13	.300	.320
E1	6.22	6.48	245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	125	.150
Q1	1.52	1.65	060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 41. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.50	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 42. 18-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86L03/L06/L16

8 MHz
18-pin DIP
Z86L0308PSC
Z86L0608PSC
Z86L1608PSC

8 MHz
18-pin SOIC
Z86L0308SSC
Z86L0608SSC
Z86L1608SSC

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

Codes

Package

P = Plastic DIP
S = Plastic SOIC

Temperature

S = 0°C to +70°C

Speed

8 = 8 MHz

Environmental

C = Plastic Standard

Example:

Z 86L03 08 P S C is a Z86L03, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow