Z86L70/L71/L72/L75/L76

ZILOG INFRARED REMOTE CONTROLLER FAMILY (ZIRC™)

FEATURES

- ROM/Package Options:
  - Z86L70 2K ROM, 128 RAM, 18-Pin SOIC/DIP
  - Z86L75 4K ROM, 256 RAM, 20-Pin SOIC/DIP
  - Z86L71 8K ROM, 256 RAM, 20-Pin SOIC/DIP
  - Z86L76 12K ROM, 768 RAM 40-Pin DIP or 44-Pin PLCC/QFP
  - Z86L72 16K ROM, 768 RAM, 40-Pin DIP or 44-Pin PLCC/QFP
  - Z86E72 16K OTP, 768 RAM 40-Pin DIP or 44-Pin PLCC/QFP (3V)
- 2.0V to 3.9V Operating Range (8.0 MHz)
- Two Standby Modes (Typical)
  - STOP - 2 µA
  - HALT - 0.8 mA
- Expanded Register File Control Registers
- Automatic External ROM Access Beyond 16K (Z86L72/76/E72 Versions)
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Registers
  - One Programmable 16-Bit Counter/Timer with One Capture Register
  - Programmable Input Glitch Filter for Pulse Reception
- Five Priority Interrupts
- Low Voltage Detection and Protection
- Programmable Watch-Dog/Power-On Reset Circuits
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive
- Mask Selectable 200 kOhms Pull-Ups on Ports 0, 2, 3
  - All Eight Port 2 Bits at One Time or Not
  - Pull-Ups Automatically Disabled Upon Selecting Individual Pins as Outputs.
- Maskable Mouse/Trackball Interface on P00 Through P03.
- Extra RAM on L72/76 is Usable as Instruction/Program Memory

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GENERAL DESCRIPTION

The ZIRC™ (Z86L7X) family of IR (Infrared) CCP™ (Consumer Controller Processor) Controllers are ROM-based members of the Z8® single-chip microcontroller family with 768/256/128 bytes of general-purpose RAM. The only differentiating factor between the five versions (Z86L70/71/72/75/76) is the availability of RAM, ROM, and package options. The ZIRC™ family of ROM devices (L72/76 versions) offers the use of external memory which enables this Z8 microcontroller to be used where code flexibility is required. Zilog's CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion along with low cost and low power consumption.

GENERAL DESCRIPTION (Continued)

The Z86L7X architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The CCP offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery operated hand-held applications.

CCP™ applications demand powerful I/O capabilities. The Z86L7X family fulfills this with three package options in which the L72/76 version provides 31 pins of dedicated input and output. These lines are grouped into four ports. Each port consists of eight lines (Port 3 has seven lines) and is configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and an address/data bus for interfacing external memory. The lower pin count version reduces the I/O count as shown in the pin descriptions while maintaining hardware and software compatibility, thereby providing the user a wide spectrum of I/O options without major rework/changes when migrating to different family versions.

There are four basic address spaces available to support a wide range of configurations: Program Memory, Register File, Data Memory, and Expanded Register File. The Register File is composed of 768/256/128 bytes of RAM. It includes four I/O port registers, ten control and status registers, and the rest are general purpose registers. The Expanded Register File consists of three register groups.

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86L7X family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

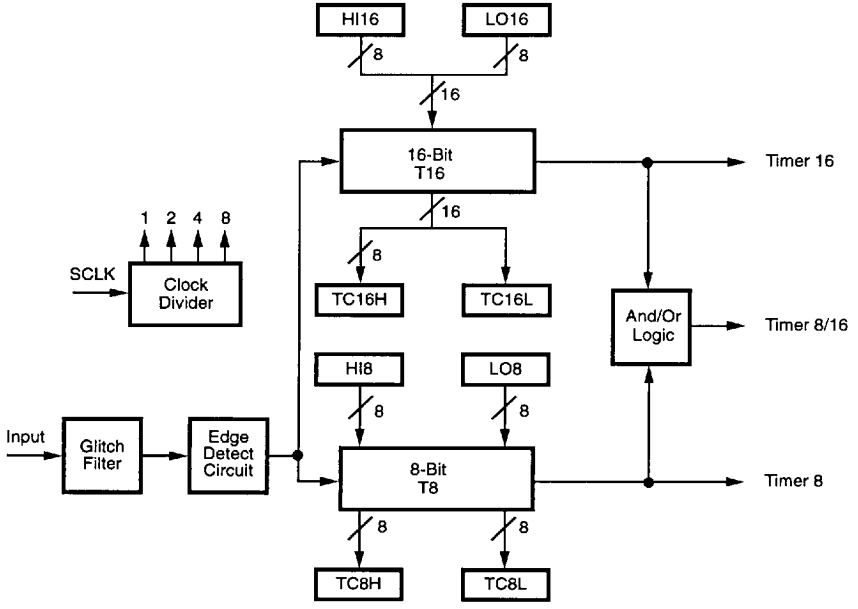

Figure 1. Counter/Timer Block Diagram

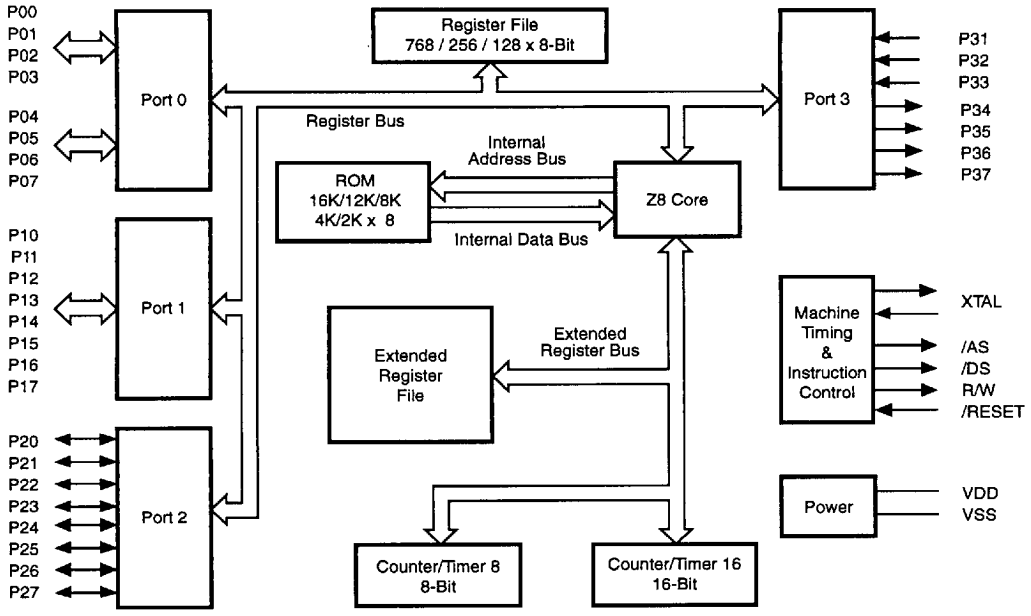

Figure 2. Functional Block Diagram

PIN DESCRIPTION

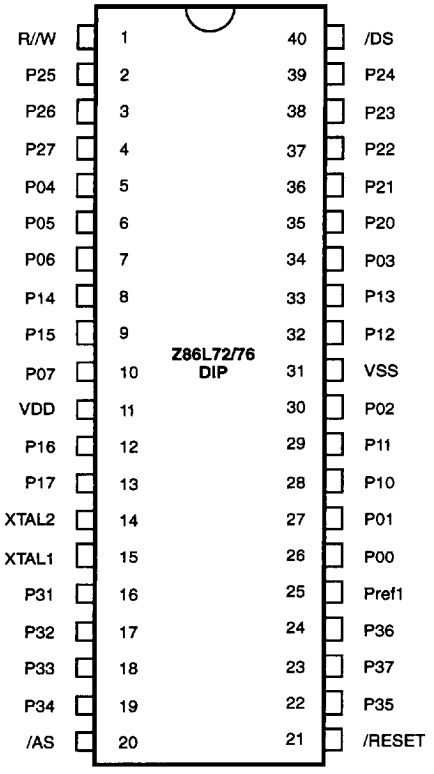

Figure 3. 40-Pin DIP Pin Assignments

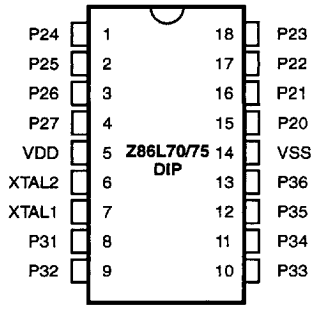

Figure 4. 18-Pin DIP Pin Assignments

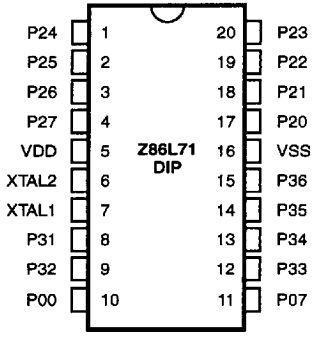

Figure 5. 20-Pin DIP Pin Assignments

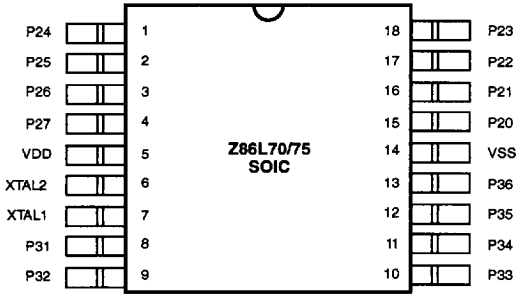

Figure 6a. 18-Pin SOIC Pin Assignments

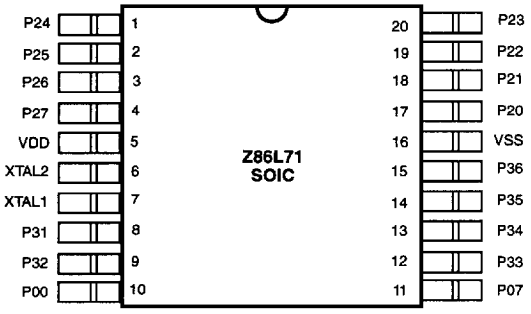

Figure 6b. 20-Pin SOIC Pin Assignments

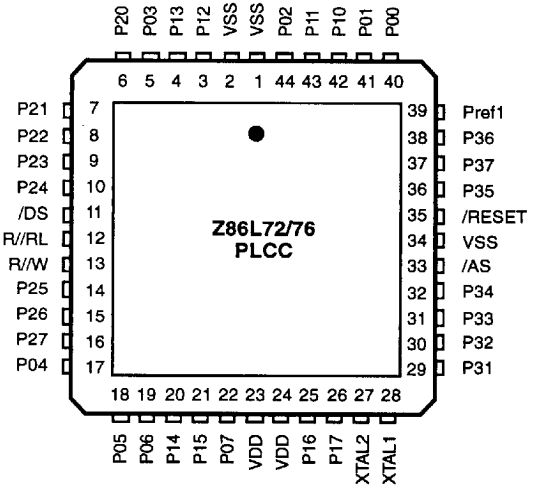

Figure 7. 44-Pin PLCC Pin Assignments

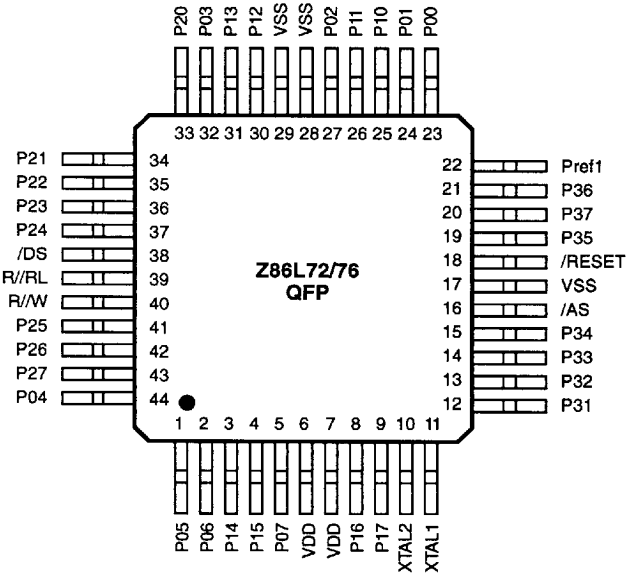

Figure 8. 44-Pin QFP Pin Assignments

PIN DESCRIPTION (Continued)

Table 1. Pin Identification

20-Pin DIP & SOIC #	40-Pin DIP#	18-Pin DIP & SOIC#	44-Pin PLCC#	44-Pin QFP#	Symbol	Direction	Description
10	26		40	23	P00	Input/Output	Port 0 is Nibble Programmable.
	27		41	24	P01	Input/Output	Port 0 can be configured as
	30		44	27	P02	Input/Output	A15-A8 external program
	34		5	32	P03	Input/Output	ROM Address Bus.
	5		17	44	P04	Input/Output	Port 0 can be configured as a
	6		18	1	P05	Input/Output	mouse/trackball input.
	7		19	2	P06	Input/Output	
11	10		22	5	P07	Input/Output	
	28		42	25	P10	Input/Output	Port 1 is byte programmable.
	29		43	26	P11	Input/Output	Port 1 can be configured as
	32		3	30	P12	Input/Output	multiplexed A7-A0/D7-D0
	33		4	31	P13	Input/Output	external program ROM
	8		20	3	P14	Input/Output	Address/Data Bus.
	9		21	4	P15	Input/Output	
	12		25	8	P16	Input/Output	
	13		26	9	P17	Input/Output	
17	35	15	6	33	P20	Input/Output	Port 2 pins are individually
18	36	16	7	34	P21	Input/Output	configurable as input or output.
19	37	17	8	35	P22	Input/Output	
20	38	18	9	36	P23	Input/Output	
1	39	1	10	37	P24	Input/Output	
2	2	2	14	41	P25	Input/Output	
3	3	3	15	42	P26	Input/Output	
4	4	4	16	43	P27	Input/Output	
8	16	8	29	12	P31	Input	IRQ2/Modulator input
9	17	9	30	13	P32	Input	IRQ0
12	18	10	31	14	P33	Input	IRQ1
13	19	11	32	15	P34	Output	T8 output
14	22	12	36	19	P35	Output	T16 output
15	24	13	38	21	P36	Output	T8/T16 output
	23		37	20	P37	Output	
	20		33	16	/AS	Output	Address Strobe
	40		11	38	/DS	Output	Data Strobe
	1		13	40	R//W	Output	Read/Write
	21		35	18	/RESET	Input	Reset
7	15	7	28	11	XTAL1	Input	Crystal, Oscillator Clock
6	14	6	27	10	XTAL2	Output	Crystal, Oscillator Clock
5	11	5	23, 24	6, 7	V_{DD}		Power Supply
16	31	14	1, 2, 34	17, 28, 29	V_{SS}		Ground
	25		39	22	Pref1	Input	Comparator 1 Reference
			12	39	R//RL		ROM//ROMless

FUNCTIONAL DESCRIPTION

/DS *(Output, active Low).* Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS *(Output, active Low).* Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1 *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2 *Crystal 2* (time-based output). This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R/W *Read/Write* (output, write Low). The R/W signal is Low when the CCP is writing to the external program or data memory.

R/RL (output, write Low). This pin, when connected to GND, disables the internal ROM and forces the device to function as a ROMless Z8. (Note that, when left unconnected or pulled high to V_{CC}, the part functions normally as a Z8 ROM version.)

Port 0 *(P07-P00).* Port 0 is an 8-bit, bi-directional, CMOS compatible port. These eight I/O lines are configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The output drivers are push-pull. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is dictated by the I/O direction to Port 0 of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

Port 0 is set in the high-impedance mode if selected as an address output state along with Port 1 and the control signals /AS, /DS, and R/W (Figure 9).

Port 00-03 can be programmed to allow direct interface to mouse/trackball IR sensors. POIM, DI, DO = 11 will enable the trip Point Buffers on these inputs.

An optional 200 kOhms pull-up is available as a mask option on all bits for the L72 versions and on P00 and P07 only for the L71 version.

These pull-ups are disabled when configured (bit by bit) as an output.

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FUNCTIONAL DESCRIPTION (Continued)

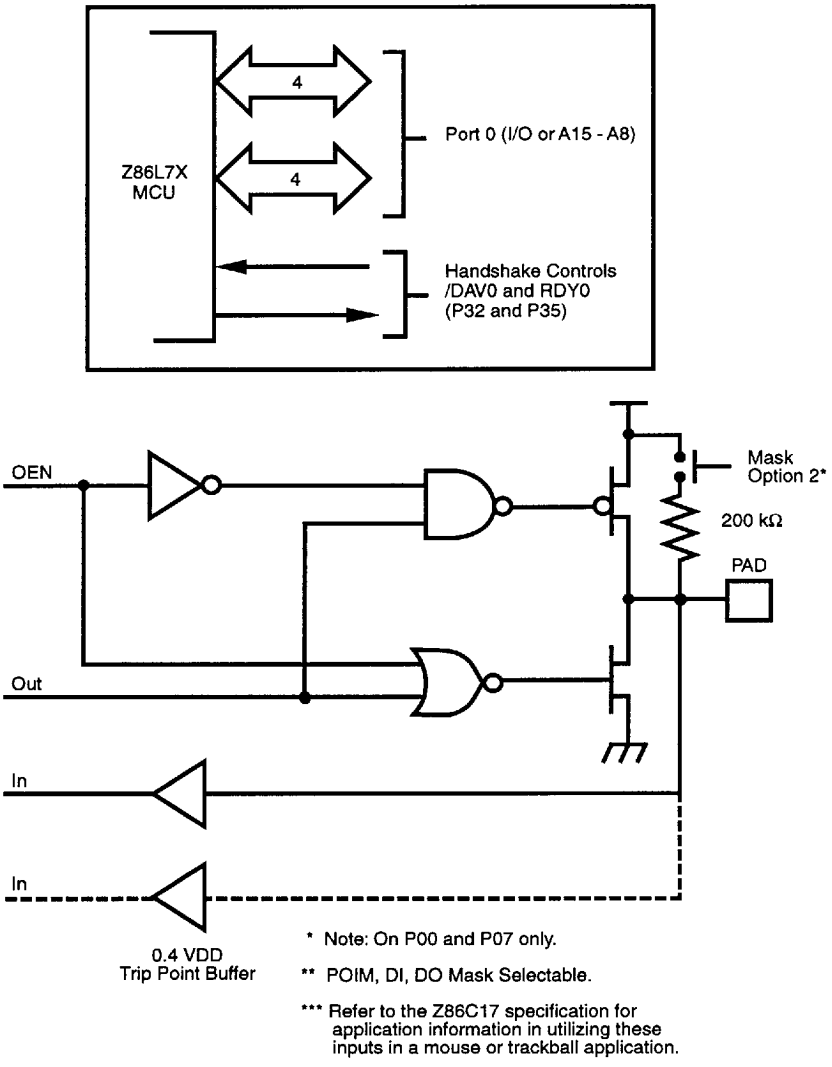


Figure 9. Port 0 Configuration

Port 1 *(P17-P10)*. Port 1 is a multiplexed Address (A7-A0) and Data (D7-D0), CMOS compatible port. Port 1 is dedicated to the Zilog ZBus®-compatible memory interface. The operations of Port 1 are supported by the Address Strobe (/AS) and Data Strobe (/DS) lines, and by the Read/Write (R/W) and Data Memory (/DM) control lines. Data memory read/write operations are done through this port (Figure 10). If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS, and R/W, allowing the Z86L7X to share common resources in multiprocessor and DMA applications.

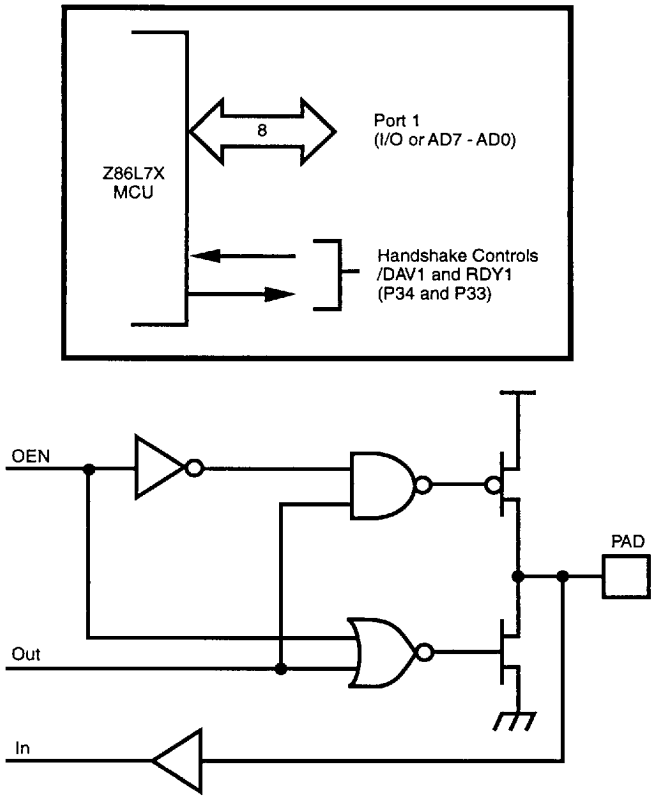


Figure 10. Port 1 Configuration

FUNCTIONAL DESCRIPTION (Continued)

Port 2 *(P27-P20).* Port 2 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight 200 kOhms (±50%) pull-up resistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. Port 2 may be placed under handshake control. In this configuration, Port 3 lines, P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3, lines P31 and P36 is dictated by the direction (input or output) assigned to Bit 7, Port 2 (Figure 11). The CCP wakes up with the eight bits of Port 2 configured as inputs with open-drain outputs.

Port 2 also has an 8-bit input OR and an AND gate which can be used to wake up the part (Figure 38). P20 can be programmed to access the edge selection circuitry (Figure 20).

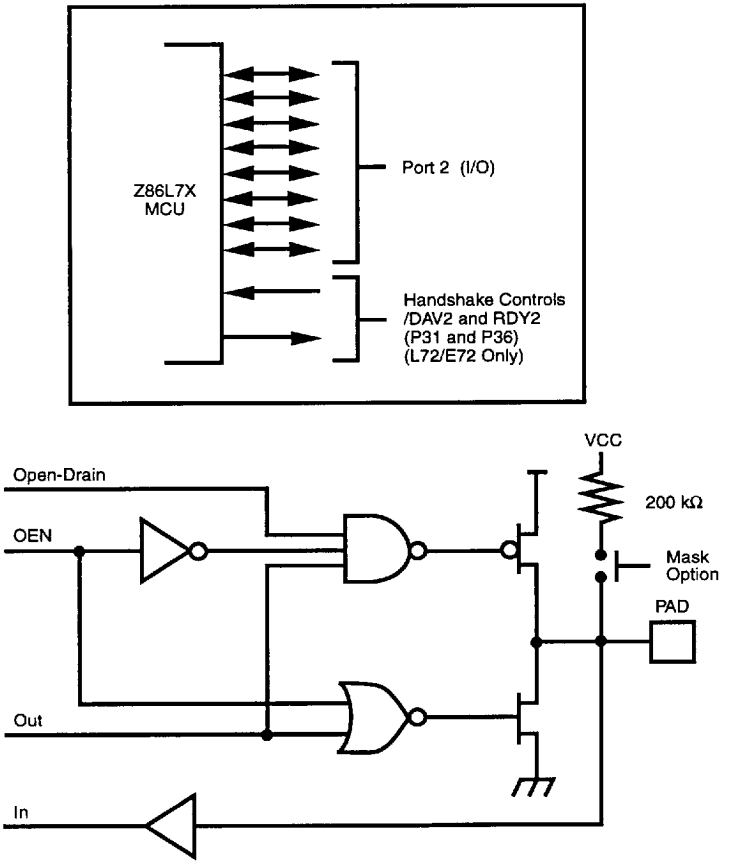


Figure 11. Port 2 Configuration

Port 3 *(P37-P31).* Port 3 is a 7-bit, CMOS compatible three fixed input and four fixed output port. Port 3 consists of three fixed input (P33-P31) and four fixed output (P37-P34), and can be configured under software control for Input/Output, Interrupt, Port handshake, Data Memory functions and output from the counter/timers. P31, P32, and P33 are standard CMOS inputs; outputs are push-pull, except for P34, 35 which are controlled by P3M, D0.

Two on-board comparators process analog signals on P31 and P32 with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the edge detection circuit is through P31 or P20. Handshake lines Ports 0, 1, and 2 are available on P31 through P36. Pref2 (P33) will be in common to both comparators for versions L70/L71/75/76 and separate for versions L72.

Port 3 provides the following control functions: handshake for Ports 0, 1, and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); Data Memory Select (/DM) (Table 4).

Port 3 also provides output for each of the counter/timers and the AND/OR Logic. Control is performed by programming bits D5-D4 of CTRI, bit 0 of CTR0 and bit 0 of CTR2.

Table 4. Pin Assignments

Pin	I/O	C/T	Comp.	Int.	P0 HS	P1 HS	P2 HS	Ext
Pref1	IN		RF1					
P31	IN	ISP	AN1	IRQ2			D/R	
P32	IN		AN2	IRQ0	D/R			
P33	IN		RF2	IRQ1		D/R		
P34	OUT	T8	A01			R/D		DM
P35	OUT	T16			R/D			
P36	OUT	T8/16					R/D	
P37	OUT		A02					
P00	I/O							

Notes:
HS = Handshake Signals
D = /DAV
R = RDY

Comparator Inputs. Port 3, P31 and P32 all have a comparator front end. The comparator reference voltages are on P33 and Pref1. The internal P33 register and its corresponding IRQ1 is connected to the Stop-Mode Recovery source selected by the SMR. In this mode, any of the Stop-Mode Recovery sources can be used to toggle the P33 bit or generate IRQ1. In digital mode, P33 can be used as a Port 3 register input or IRQ1 for P33 (Figure 13).

Comparator Outputs. These may be programmed to be outputted on P34 and P37 through the PCON register (Figure 12).

/RESET *(Input, active Low).* Initializes the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer, Stop-Mode Recovery, Low Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the reset line should be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. There is no condition internal to the L7X that will not allow an external reset to occur.

FUNCTIONAL DESCRIPTION (Continued)

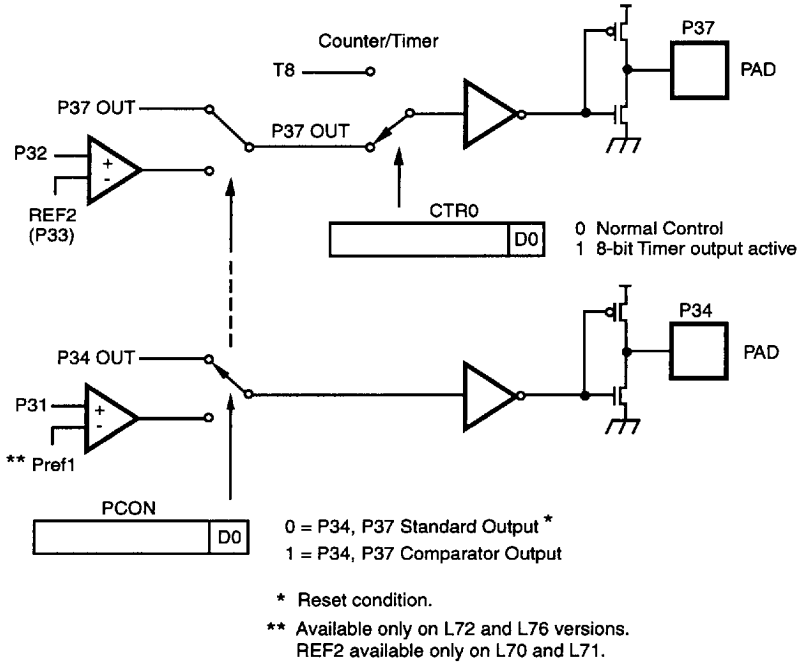


Figure 12. Port 3 Configuration

After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z86L7X is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer.

During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000CH, 5-10 TpC cycles after the RST is released. For Power-On Reset, the typical reset output time is 5 ms. The Z86L7X does not reset WDTMR, SMR, P2M, or P3M registers on a Stop-Mode Recovery operation.

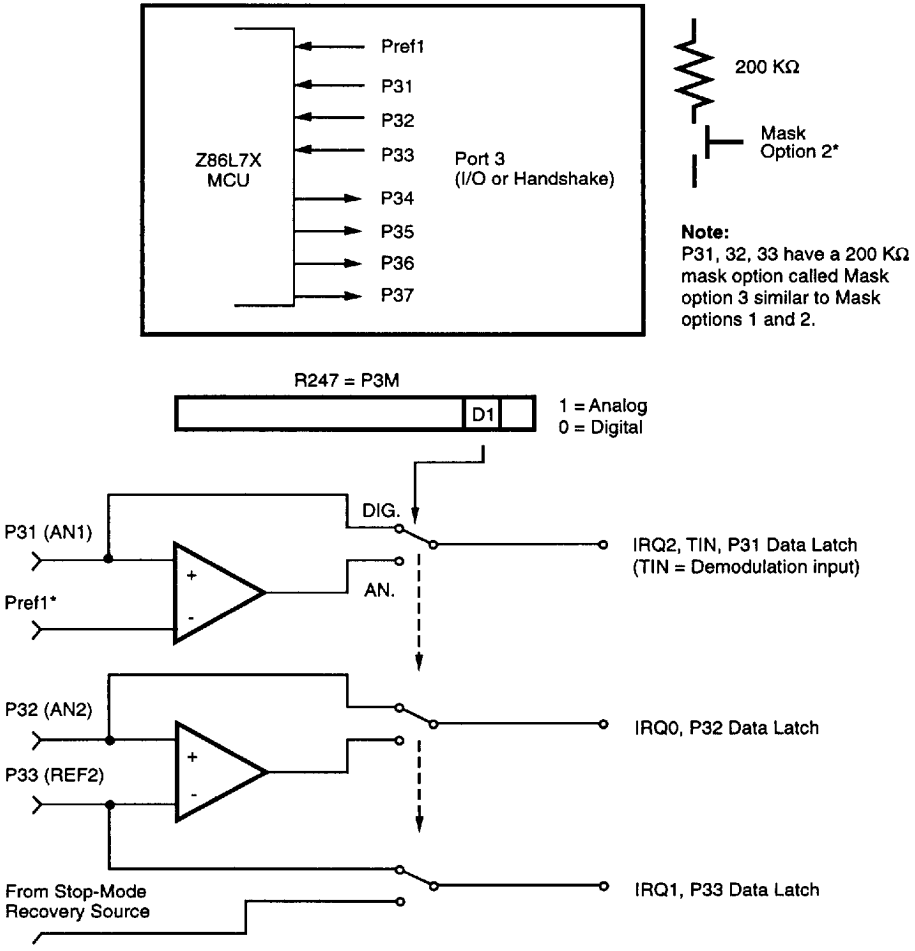


Figure 13. Port 3 Configuration

FUNCTIONAL DESCRIPTION (Continued)

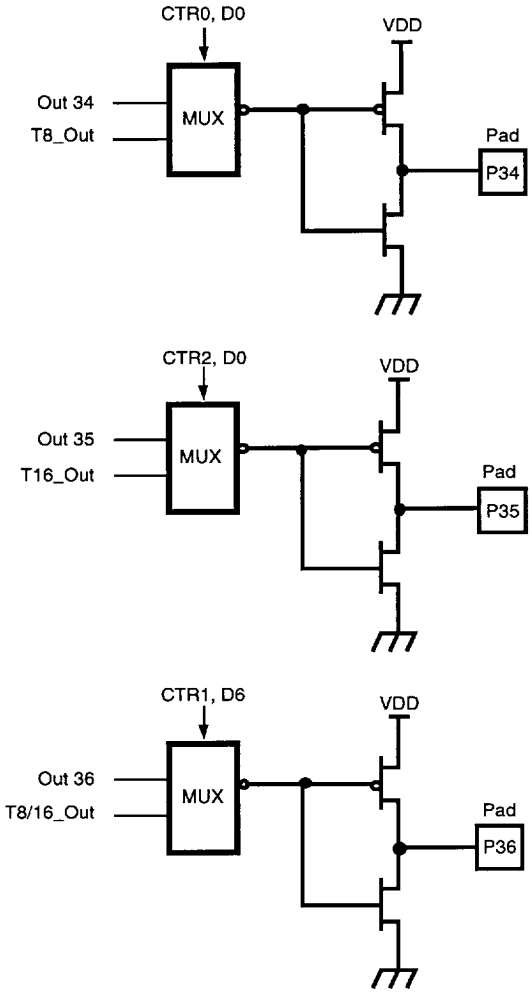


Figure 14. Port 3 Configuration

The Z8 CCP incorporates special functions to enhance the Z8's functionality in consumer and battery operated applications.

Reset. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- Low Voltage Detection
- External Reset (Z86L72,76 and E72 only)

Program Memory. The Z86L7X addresses up to 2K, 4K, 8K, and 16 Kbytes of internal program memory, with the remainder being external memory (Figure 15). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain five 16-bit vectors that correspond to the five available interrupts. Addresses 12 to 2K, 4K, 8K, 12K or 16K (dependent on version) consist of on-chip mask-programmed ROM. At addresses 16K and greater, the Z86L72/76 executes external program memory fetches (refer to external memory timing specifications).

Note: The Z86L76 will not work on accesses between 12K and 16K but will access external memory only above 16K as described above.

RAM. The Z86L72 and L76 and versions have 768-byte RAM. 256 of them are in the register file. The other 512 bytes are mapped into the External ROM address between 65023 through 65535. Accessing the 512 bytes is accomplished through the LDE instructions.

Note: This additional 512 bytes of RAM may also be utilized for instruction code memory.

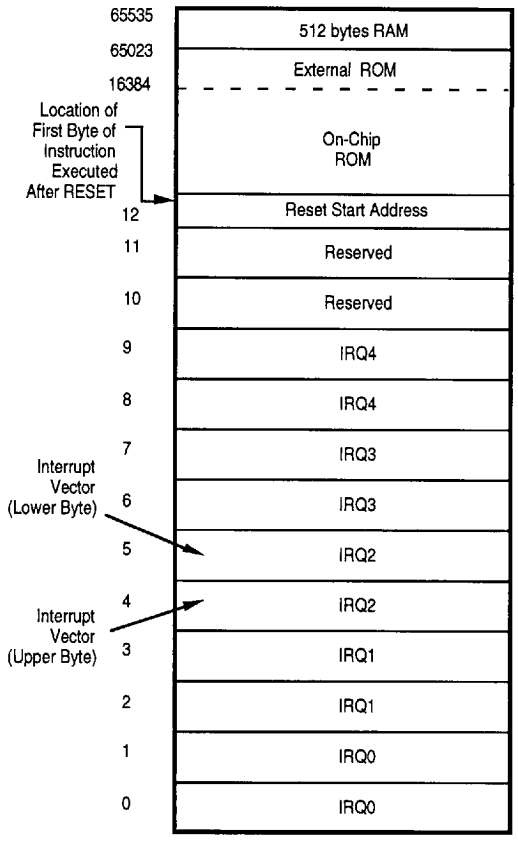


Figure 15. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)

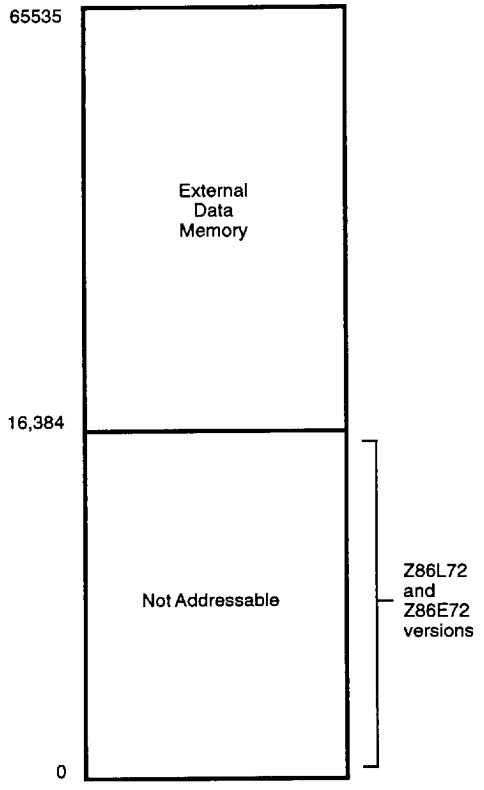


Figure 16. Data Memory Map

External Data Memory *(/DM).* The Z86L7X addresses up to 48K, 52K, 56K, 60K or 62 Kbytes of external data memory beginning at location 000CH (Figure 16). External data memory is included with, or separated from, the external program memory space. /DM, an optional I/O function that is programmed to appear on P34, is used to distinguish between data and program memory space. The state of the /DM signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory.

Expanded Register File. The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 17).

The upper nibble of the register pointer (Figure 19) selects which group of 16 bytes in the register file, out of the full 256, will be accessed. The lower nibble selects the expanded register file bank and, in the case of the Z86L70/71/72/75/76, Banks F and D are implemented. A 0H in the lower nibble will allow the normal register file to be addressed, but any other value from 1H to FH will exchange the lower 16 registers in favor of an expanded register group of 16 registers.

For example:

Z86L71: (See Figure 17)

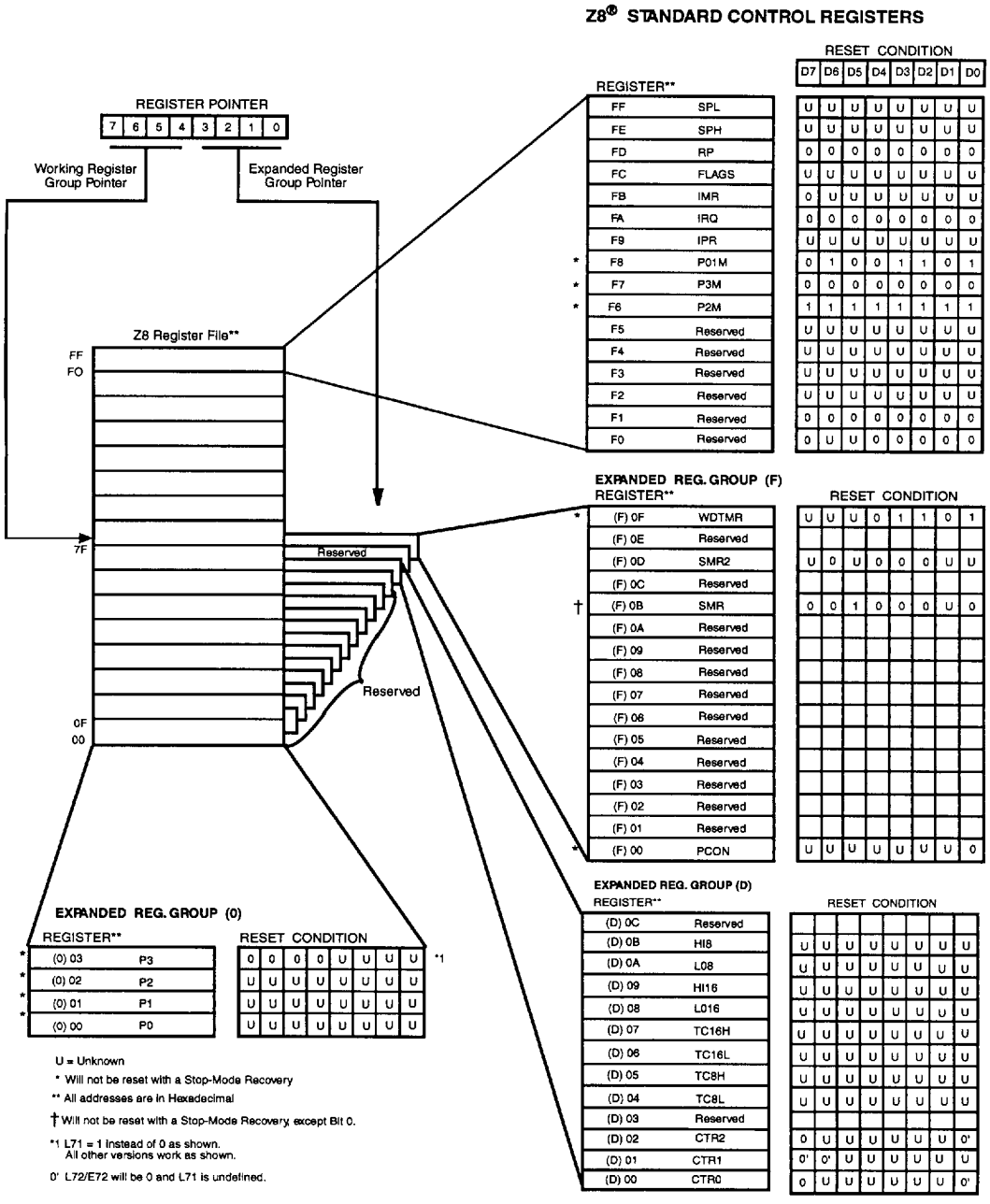
R253 RP = 00H
R0 = Port 0
R1 = Port 1
R2 = Port 2
R3 = Port 3

But if:

R253 RP = 0DH
R0 = CTRL0
R1 = CTRL1
R2 = CTRL2
R3 = Reserved

The counter/timers are mapped into ERF group D. Access is easily done using the following example:

```
LD    RP, #0DH     Select ERF D for access and
                   register Bank 0 as
                   the working register group
LD    R0,#xx       access CTRL0
LD    1, #xx       access CTRL1
LD    RP, #7DH     Select expanded register group
                   (ERF) group D for access and
                   register Bank 7 as the working
                   register bank
LD    R1, 2        CTRL2 → register 71H
```



U = Unknown

* Will not be reset with a Stop-Mode Recovery

** All addresses are in Hexadecimal

† Will not be reset with a Stop-Mode Recovery, except Bit 0.

*1 L71 = 1 Instead of 0 as shown.
All other versions work as shown.

0' L72/E72 will be 0 and L71 is undefined.

Figure 17. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

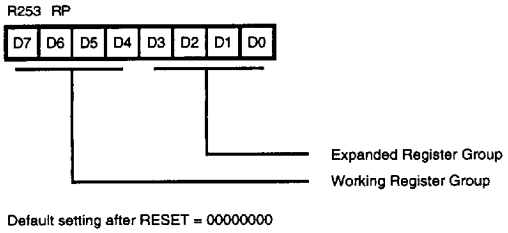


Figure 18. Register Pointer Register

Register File. The register file consists of four I/O port registers, 124, 256, or 768 general-purpose registers with 15 control and status registers (R3-R0, R239-R4, and R255-R240, respectively), plus three Expanded Register Groups (0, D, and F) which reside in the expanded register group. Instructions can access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 19). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: Register Bank E0-EF is only accessed through working registers and indirect addressing modes.

Stack. The Z86L7X external data memory or the internal register file is used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the general-purpose registers (R4-R112/239/748). SPH is used as a general-purpose register only when using internal stacks.

Note: When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH will be loaded into Port 0 whenever the internal stack is accessed.

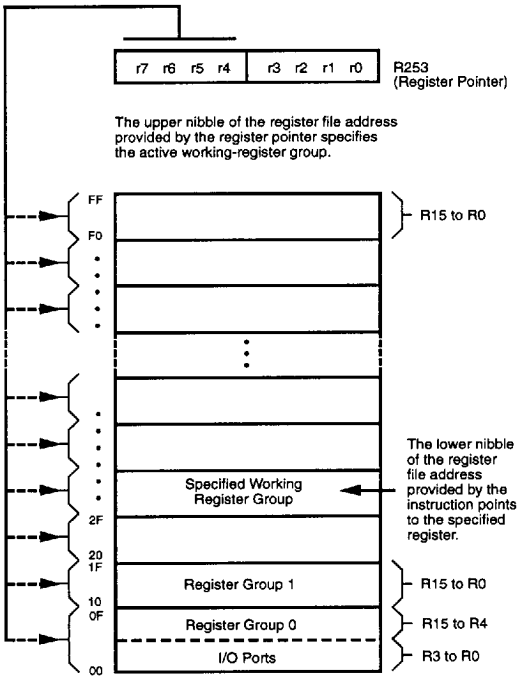


Figure 19. Register Pointer

COUNTER/TIMER REGISTER DESCRIPTION

Expanded Register Group D			
(D)%0C	Reserved	(D)%05	TC8H
(D)%0B	HI8	(D)%04	TC8L
(D)%0A	LO8	(D)%03	Reserved
(D)%09	HI16	(D)%02	CTR2
(D)%08	LO16	(D)%01	CTR1
(D)%07	TC16H	(D)%00	CTR0
(D)%06	TC16L		

Register Description

HI8(D)%0B: Holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 1.

Field	Bit Position		Value	Description
T8_Capture_HI	76543210	R		Captured Data
		W		No Effect

LO8(D)%0A: Holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 0.

Field	Bit Position		Value	Description
T8_Capture_LO	76543210	R		Captured Data
		W		No Effect

HI16(D)%09: Holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Value	Description
T16_Capture_HI	76543210	R		Captured Data
		W		No Effect

L016(D)%08: Holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Value	Description
T16_Capture_LO	76543210	R		Captured Data
		W		No Effect

COUNTER/TIMER REGISTER DESCRIPTION (Continued)

TC16H(D)%07: Counter/Timer2 MS-Byte Hold Register.

Field	Bit Position		Value	Description
T16_Data_HI	76543210	R/W		Data

TC16L(D)%06: Counter/Timer2 LS-Byte Hold Register.

Field	Bit Position		Value	Description
T16_Data_LO	76543210	R/W		Data

TC8H(D)%05: Counter/Timer8 High Hold Register.

Field	Bit Position		Value	Description
T8_Level_HI	76543210	R/W		Data

TC8L(D)%04: Counter/Timer8 Low Hold Register.

Field	Bit Position		Value	Description
T8_Level_LO	76543210	R/W		Data

CTR0 (D)00: Counter/Timer8 Control Register.

Field	Bit Position		Value	Description
T8_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-------	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	--5------	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T8 _Clock	---43---	R/W	0 0*	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_MASK	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
			1	Enable Time-Out Int.
P34_Out	-------0	R/W	0	P34 as Port Output
			1	T8 Output on P34

Notes:
* Indicates the value upon Power-On Reset.

CTR0: Counter/Timer8 Control Register Description

T8 Enable. This field enables T8 when set (written) to 1.

Single/Modulo-N. When set to 0 (modulo-n), the counter reloads the initial value when the terminal count is reached. When set to 1 (single pass), the counter stops when the terminal count is reached.

Time-Out. This bit is set when T8 times out (terminal count reached). To reset this bit, a 1 should be written to this location. ***This is the only way to reset this status condition, therefore, care should be taken to reset this bit prior to using/enabling the counter/timers.***

Note:
Care must be taken when utilizing the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers will be ORed or ANDed with the designated value and then written back into the registers. Example: When the status of bit 5 is 1, a reset condition will occur.

T8 Clock. Defines the frequency of the input signal to T8.

Capture_INT_Mask. Set this bit to allow interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask. Set this bit to allow interrupt when T8 has a time out.

P34_Out. This bit defines whether P34 is used as a normal output pin or the T8 output.

3

COUNTER/TIMER REGISTER DESCRIPTION (Continued)

CTR1(D)%01: Controls the functions in common with the T8 and T16.

Field	Bit Position		Value	Description
Mode	7-------	R/W	0	Transmit Mode
			1	Demodulation Mode
P36_Out/	-6------	R/W		Transmit Mode
Demodulator_Input			0	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/	--54----	R/W		Transmit Mode
Edge _Detect			00	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved
Transmit_Submode/	----32--	R/W		Transmit Mode
Glitch_Filter			00	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	16 SCLK Cycle
Initial_T8_Out/	------1-			Transmit Mode
Rising_Edge		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/	-------0			Transmit Mode
Falling _Edge		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

CTR1 Register Description

Mode. If it is 0, the Counter/Timers are in the transmit mode, otherwise they are in the demodulation mode.

P36_Out/Demodulator_Input. In Transmit Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In Demodulation Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

T8/T16_Logic/Edge _Detect. In Transmit Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In Demodulation Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter. In Transmit Mode, this field defines whether T8 and T16 are in the "Ping-Pong" mode or in independent normal operation mode. Setting this field to "Normal Operation Mode" terminates the "Ping-Pong Mode" operation. When set to 1, T16 is immediately functional and can cause interrupts. The output is forced to a 0. When set to 11, T16 is immediately forced to a 1.

In Demodulation Mode, this field defines the width of the glitch that should be filtered out.

Initial_T8_Out/Rising_Edge. In Transmit Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count.

In Demodulation Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge. In Transmit Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or Ping-Pong Mode (CTR1, D3, D2).

In Demodulation Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

3

COUNTER/TIMER REGISTER DESCRIPTION (Continued)

CTR2 (D)%02: Counter/Timer16 Control Register.

Field	Bit Position		Value	Description
T16_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Submode	-6------	R/W		Transmit Mode
			0	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	--5-----	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	---43---	R/W	00	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
			1	Enable Time-Out Int.
P35_Out	-------0	R/W	0	P35 as Port Output
			1	T16 Output on P35

Notes:
* Indicates the value upon Power-On Reset.

CTR2 Description

T16_Enable. This field enables T16 when set to 1.

Single/Modulo-N. In Transmit Mode, when set to 0, the counter reloads the initial value when terminal count is reached. When set to 1, the counter stops when the terminal count is reached.

In Demodulation Mode, when set to 0 , T16 captures and reloads on detection of all the edges; when set to 1, T16 captures and detects on the first edge, but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode.

Time_Out. This bit is set when T16 times out (terminal count reached). In order to reset it, a 1 should be written to this location.

T16_Clock. Defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask. Set this bit to allow interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask. Set this bit to allow interrupt when T16 times out.

P35_Out. This bit defines whether P35 is used as a normal output pin or T16 output.

SMR2(F)%0D: Stop-Mode Recovery Register 2.

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0* 1	Low High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000* 001 010 011 100 101 110 111	A. POR Only B. NAND of P23-P20 C. NAND or P27-P20 D. NOR of P33-P31 E. NAND of P33-P31 F. NOR of P33-P31, P00,P07 G. NAND of P33-P31,P00,P07 H. NAND of P33-P31,P22-P20
Reserved	------10		00	Reserved (Must be 0)

Notes:
* Indicates the value upon Power-On Reset.

Port pins configured as outputs are ignored as an SMR2 recover source. For example, if NAND of P23-P20 is selected as the recover source and P20 is configured as output, then P20 is ignored as a recover source. The effective recover source in this case is NAND of P23-P21.

3

FUNCTIONAL DESCRIPTION (Continued)
Counter/Timer Functional Blocks

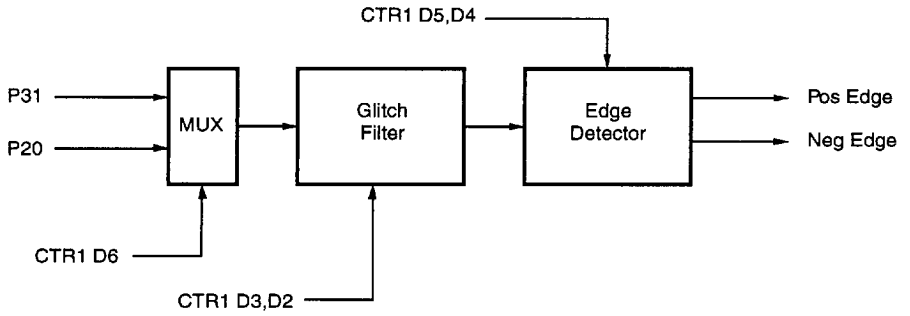


Figure 20. Glitch Filter Circuitry

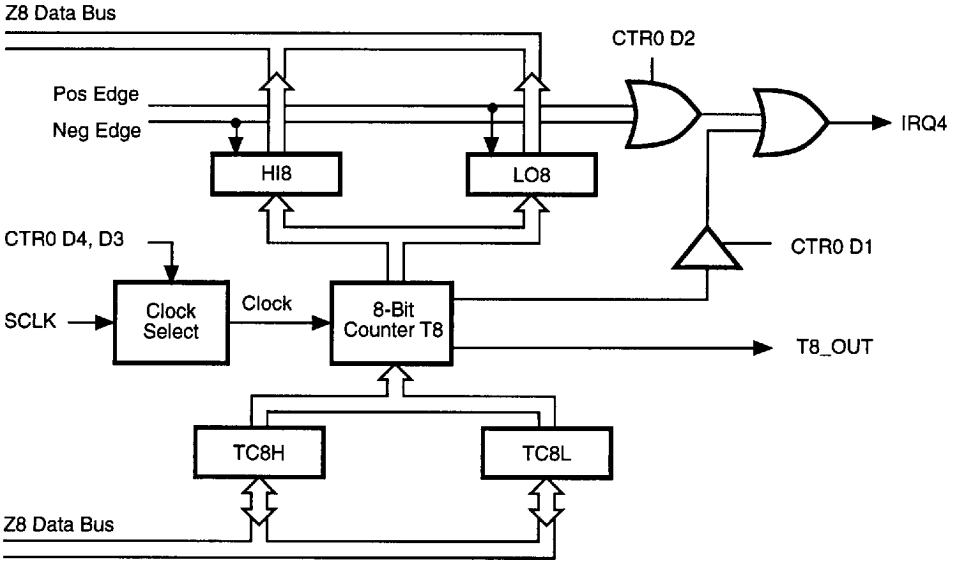


Figure 21. 8-bit Counter/Timer Circuits

Input Circuit
The edge detector monitors the input signal on P31 or P21. Based on CTR1 D5-D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal which have a width less than specified (CTR1 D3, D2) are filtered out.

T8 Transmit Mode
When T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1. If it is 1, T8_OUT is 0.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1 D1). If the initial value (CTR1 D1) is 0, TC8L is loaded, otherwise TC8H is loaded into the counter. In Single-Pass Mode (CTR0 D6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0 D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0 D1) (Figure 22). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. Then T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, sets the time-out status bit (CTR0 D5) and generates an interrupt if enabled (CTR0 D1) (Figure 23). This completes one cycle. T8 then loads from TC8H or TC8L according to the T8_OUT level, and repeats the cycle.

The user can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded. Care must be taken not to write these registers at the time the values are to be loaded into the counter/timer, to ensure known operation. ***An initial count of 1 is not allowed (a non-function will occur).*** An initial count of 0 will cause TC8 to count from 0 to %FF to %FE (Note, % is used for hexadecimal values). Transition from 0 to %FF is not a time-out condition.

Note:
Using the same instructions for stopping the counter/timers and setting the status bits is not recommended. Two successive commands, first stopping the counter/timers, then resetting the status bits is necessary. This is required because it takes one counter/timer clock interval for the initiated event to actually occur.

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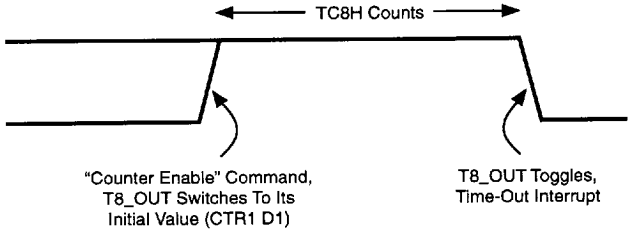

Figure 22. T8_OUT in Single-Pass Mode

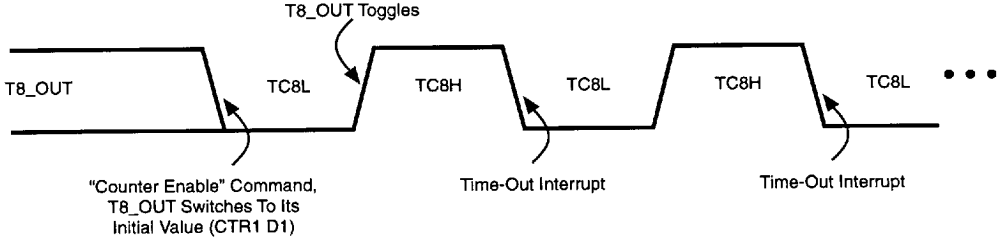

Figure 23. T8_OUT in Modulo-N Mode

FUNCTIONAL DESCRIPTION (Continued)

T8 Demodulation Mode

The user should program TC8L and TC8H to %FF. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8, if negative edge, HI8. One of the edge detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with %FF and starts counting again. Should T8 reach 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from %FF (Figure 24).

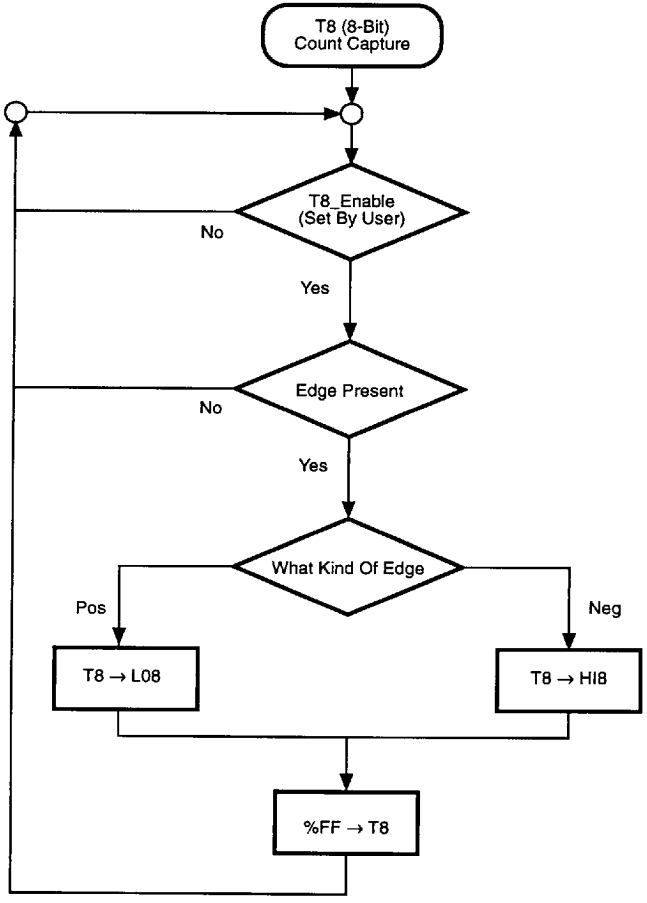

Figure 24. Demodulation Mode Count Capture Flowchart

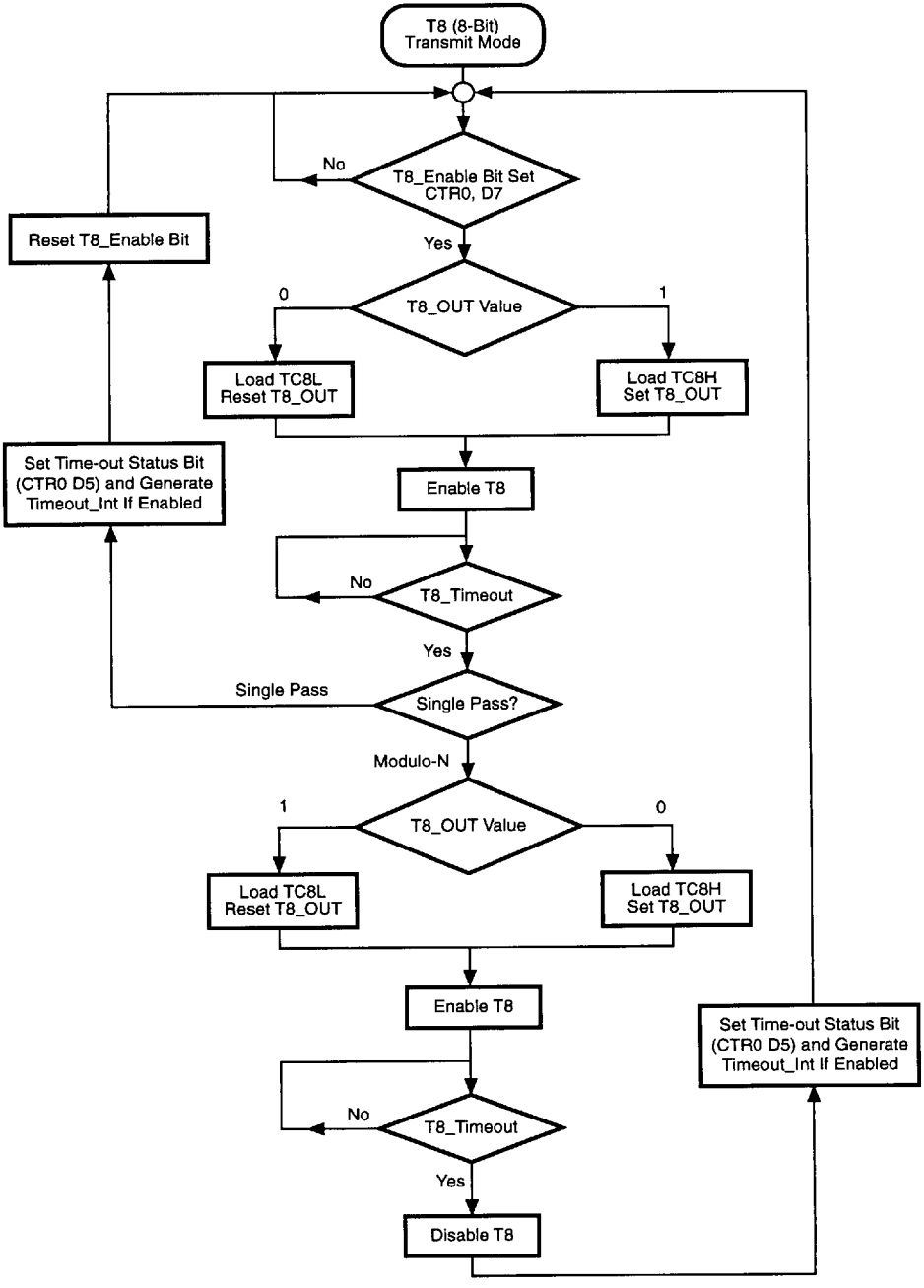

Figure 25. Transmit Mode Flowchart

FUNCTIONAL DESCRIPTION (Continued)

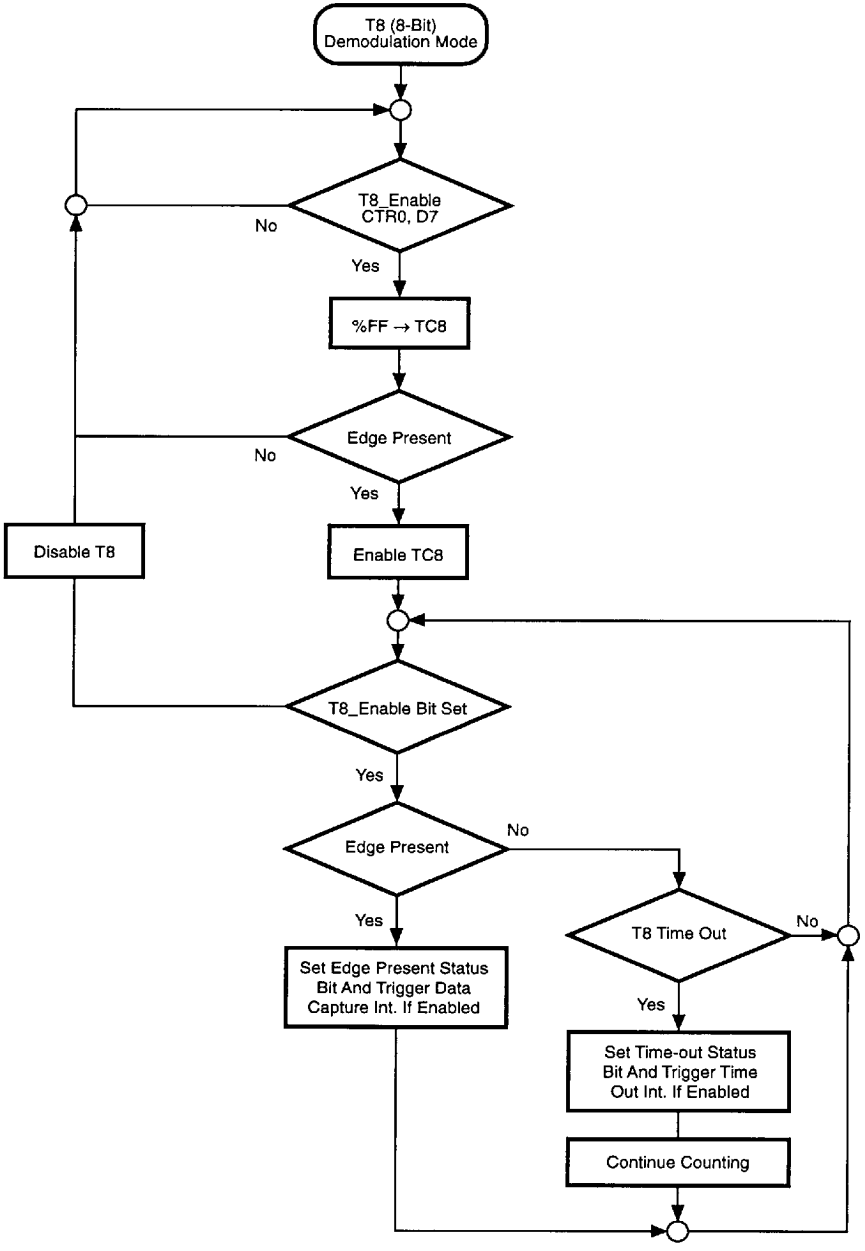

Figure 26. Demodulation Mode Flowchart

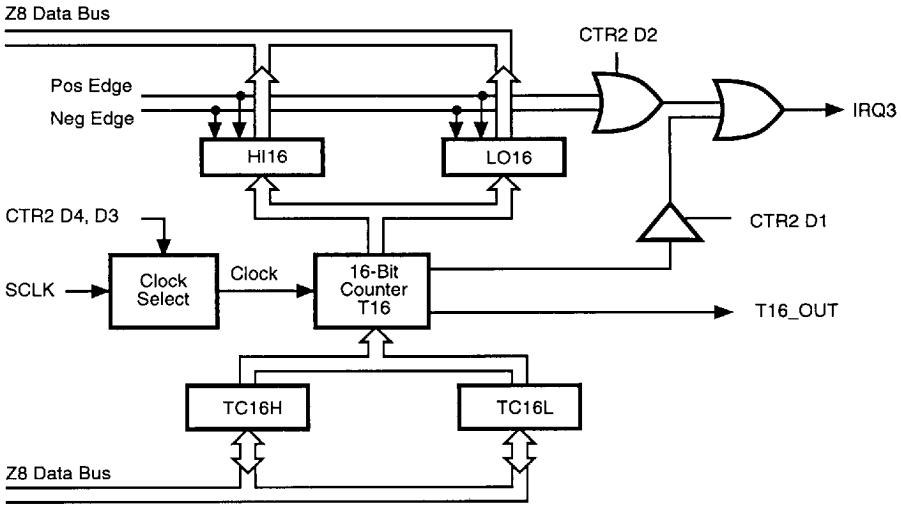

Figure 27. 16-bit Counter/Timer Circuits

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T16 Transmit Mode

In Normal or Ping-Pong Mode, the output of T16 when not enabled is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. The user can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3, D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1 D0). When T16 counts down to 0, T16_OUT is toggled (in Normal or Ping-Pong Mode), an interrupt is generated if enabled (CTR2 D1), and a status bit (CTR2 D5) is set. Note that global interrupts will override this function as described in the interrupts section. If T16 is in Single-Pass Mode, it is stopped at this point. If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L and the counting continues.

The user can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded. Care must be taken not to load these registers at the time the values are to be loaded into the counter/timer, to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 will cause T16 to count from 0 to %FF FF to %FFFE. Transition from 0 to %FFFF is not a time-out condition.

FUNCTIONAL DESCRIPTION (Continued)

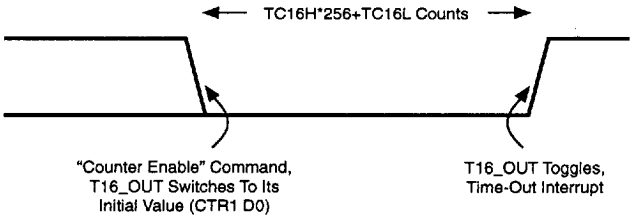


Figure 28. T16_OUT in Single-Pass Mode

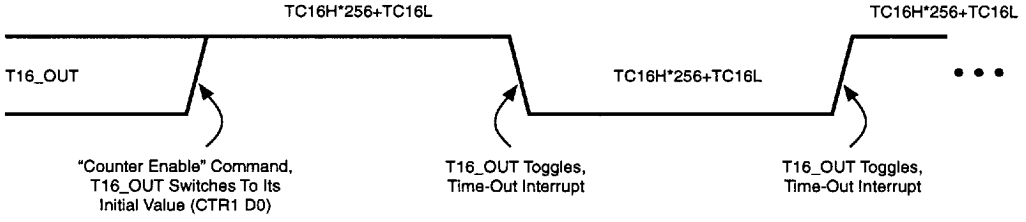


Figure 29. T16_OUT in Modulo-N Mode

T16 Demodulation Mode

The user should program TC16L and TC16H to %FF. After T16 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, T16 captures HI16 and LO16 and then reloads.

If D6 of CTR2 is 0: When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current count in T16 is one's complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1 D1, D0) is set and an interrupt is generated if enabled (CTR2 D2). T16 is loaded with %FFFF and starts again.

If D6 of CTR2 is 1: T16 ignores the subsequent edges in the input signal and continues counting down. A time out of T8 will cause T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 will capture and reload on the next edge (rising, falling, or both depending on CTR1 D5, D4) but continue to ignore subsequent edges.

Should T16 reach 0, it continues counting from %FFFF; meanwhile, a status bit (CTR2 D5) is set and an interrupt time-out can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in Transmit Mode. T8 and T16 need to be programmed in Single-Pass Mode (CTR0 D6, CTR2 D6) and Ping-Pong Mode needs to be programmed in CTR1 D3, D2. The user can begin the operation by enabling either T8 or T16 (CTR0 D1 or CTR2 D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1 D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled and T16 is enabled. T16_OUT switches to its initial value (CTR1 D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count it stops, T8 is enabled again, and the whole cycle repeats. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0 D1, CTR2 D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1.

Note:
Enabling Ping-Pong operation while the counter/timers are running may cause intermittent counter/timer function. Disable the counter/timers, then reset the status flags prior to instituting this operation.

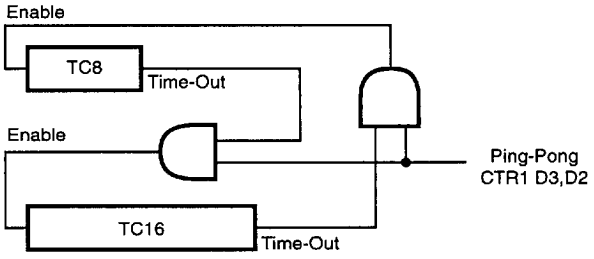


Figure 30. Ping-Pong Mode

To Initiate Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) will be cleared by hardware. The time-out bits (CTR0 D5, CTR2 D5) will be set every time the counter/timers reach the terminal count.

FUNCTIONAL DESCRIPTION (Continued)

To Terminate Ping-Pong Mode

Change Transmit Mode to Normal Mode (CTR1 D2, D3). Notice that Ping-Pong Mode is not actually stopped until one of the timer/counter's time-out. Before the actual termination of Ping-Pong Mode, the user should not change the value of CTR0 or CTR2, except for resetting the time-out status bit. Here is an example for terminating Ping-Pong Mode safely:

```
        or      CTR0,#%20           ;reset T8 time-out status bit
loop_a:
        tm      CTR0,#%20
        jr      z,loop_a            ;wait until T8 times-out

        ld      CTR1,#00000000b     ;change to Normal Mode

        or      CTR2,#%20           ;reset T16 time-out status bit
loop_b:
        tm      CTR2,#%20
        jr      z,loop_b            ;wait until T16 times-out

                                    ;now Ping-Pong Mode is actually
        ld      CTR0,#00100000b     ;terminated and user can re-program T8
        ld      CTR2,#00100000b     ;and T16
```

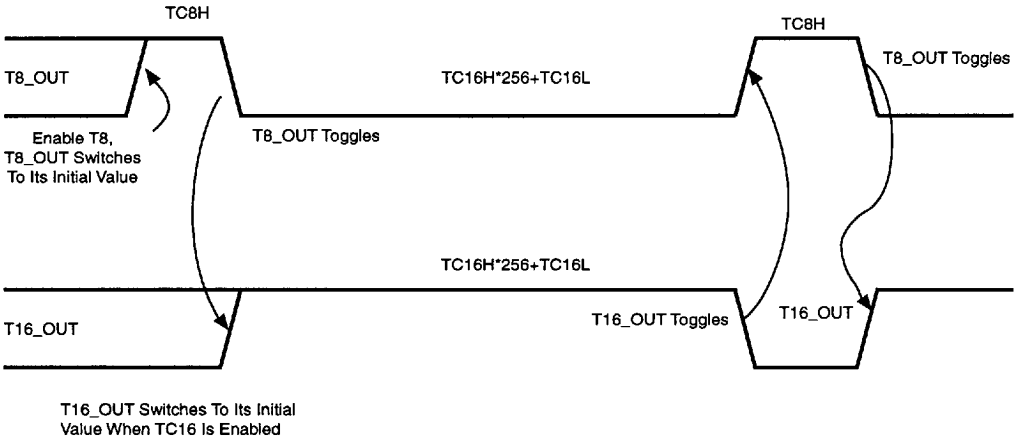


Figure 31. T8_OUT and T16_OUT in Ping-Pong Mode

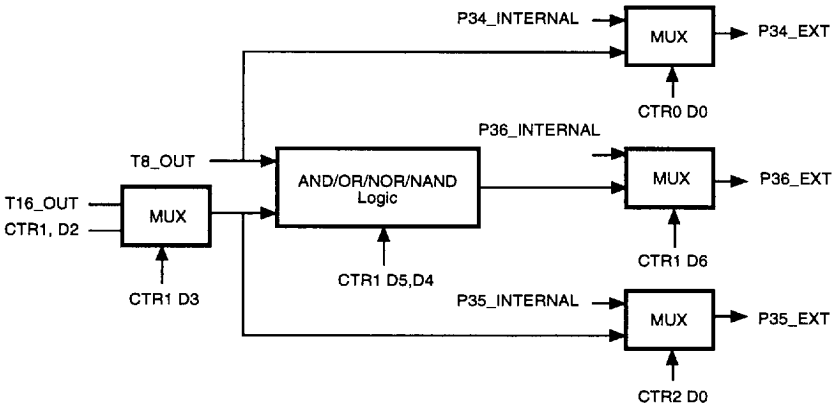


Figure 32. Output Circuit

Interrupts. The Z86L7X has five different interrupts. The interrupts are maskable and prioritized (Figure 33). The five sources are divided as follows: three sources are claimed by Port 3 lines P33-P31, the remaining two by the counter/timers (Table 5). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.

3

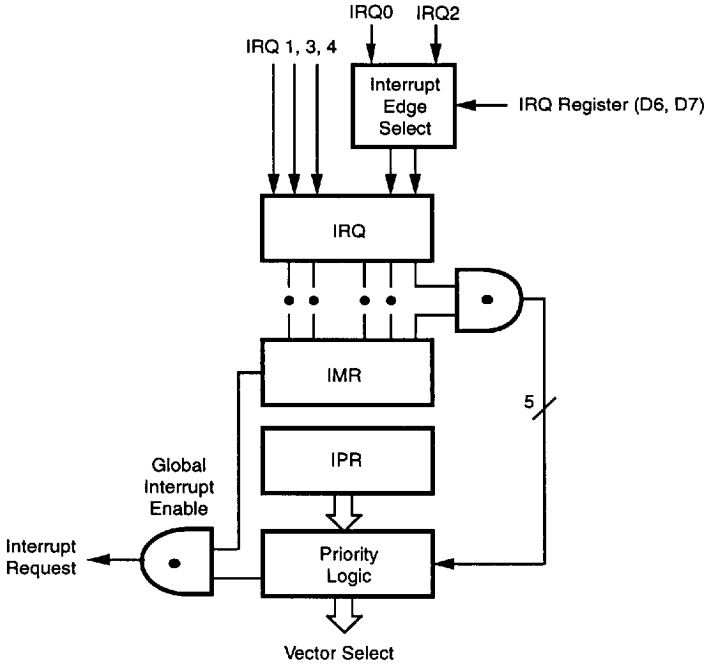


Figure 33. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Table 5. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising Falling Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rising Falling Edge Triggered
IRQ3	T16	6, 7	Internal
IRQ4	T8	8, 9	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86L7X interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6 . The configuration is shown in Table 6.

Table 6. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z86L7X on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The Z86L7X on-chip oscillator may be driven with a low cost RC network or other suitable external clock source.

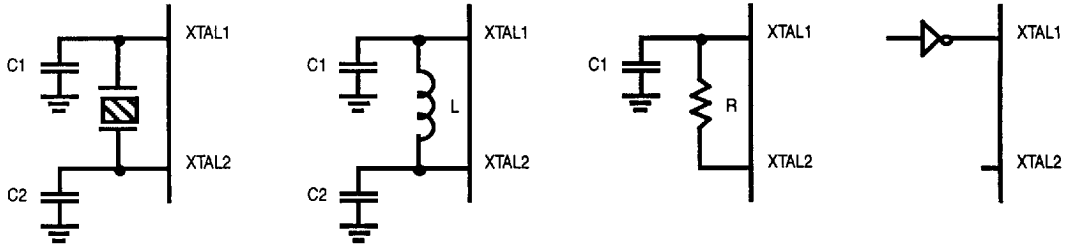
The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 34).

Power-On Reset *(POR).* A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power Fail to Power OK status.
2. Stop-Mode Recovery (if D5 of SMR = 1).
3. WDT Time-Out.

The POR time is a nominal 5 ms. Bit 7 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC, LC oscillators).



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
f = 8 MHz

LC
C1, C2 = 22 pF

L = 130 µH *
f = 3 MHz *

RC
@ 3V VCC (TYP)

C1 = 33 pF *
R = 1K *

External Clock

* Preliminary value including pin parasitics

Figure 34. Oscillator Configuration

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, and IRQ4 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA (typical) or less. STOP mode is terminated only by a reset, such as WDT time-out, POR, SMR, or external reset. This causes the processor to restart the application program at address 000CH. In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, i.e.,

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP mode
                or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT mode
```

Port Configuration Register *(PCON).* The PCON register configures the comparator output on Port 3. It is located in the expanded register file at Bank F, location 00 (Figure 35).

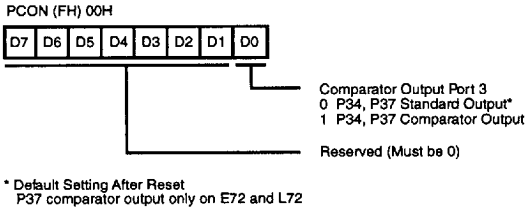


Figure 35. Port Configuration Register (PCON) (Write Only)

FUNCTIONAL DESCRIPTION (Continued)

Comparator Output Port 3 *(D0).* Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Stop-Mode Recovery Register *(SMR).* This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 36). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR register, specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

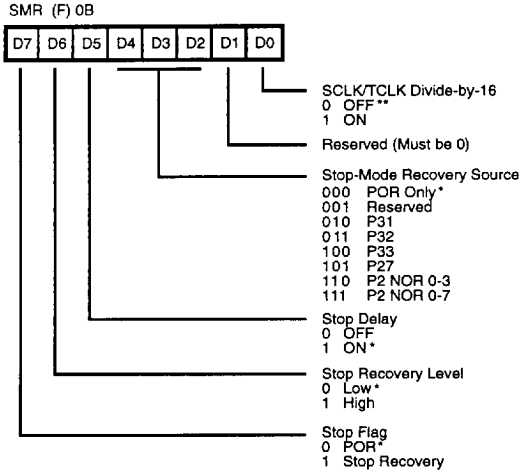


Figure 36. Stop-Mode Recovery Register

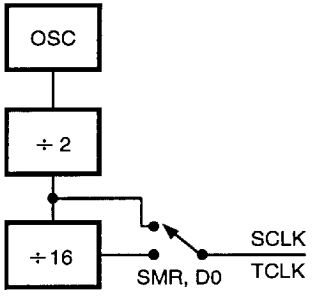


Figure 37. SCLK Circuit

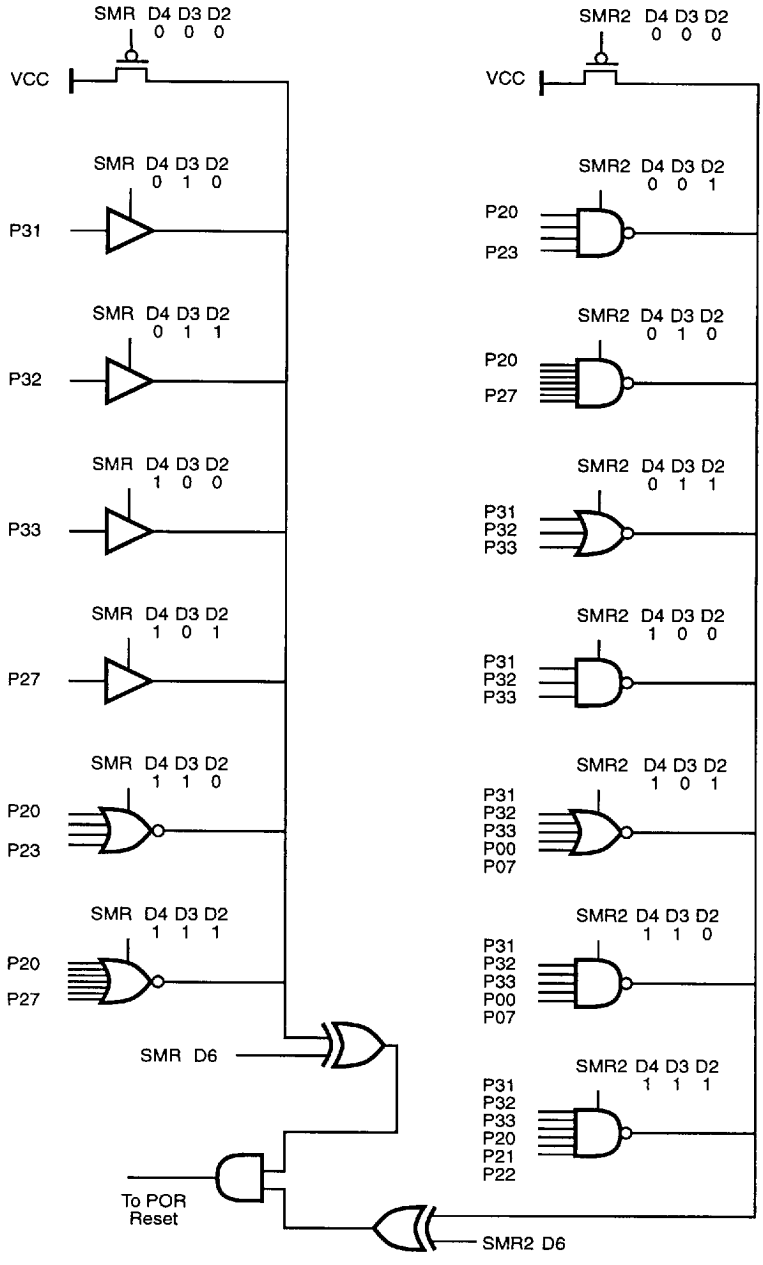


Figure 38. Stop-Mode Recovery Source

FUNCTIONAL DESCRIPTION (Continued)

SCLK/TCLK Divide-by-16 Select *(D0).* D0 of the SMR controls a Divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources interrupt logic). After Stop-Mode Recovery, this bit is set to a 0.

Stop-Mode Recovery Source *(D2, D3, and D4).* These three bits of the SMR specify the wake up source of the STOP recovery (Figure 38 and Table 7).

Table 7. Stop-Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	P30 transition
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Note:
Any Port 2 bit defined as an output will drive the corresponding input to the default state to allow the remaining inputs to control the AND/OR function. Refer to SMR2 register for other recover sources.

Stop-Mode Recovery Delay Select *(D5).* This bit, if High, disables the 5 ms /RESET delay after Stop-Mode Recovery. The default configuration of this bit is one. If the "fast" wake up is selected, the Stop-Mode Recovery source needs to be kept active for at least 5TpC.

Stop-Mode Recovery Edge Select *(D6).* A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Z86L7X from STOP mode. A 0 indicates Low level recovery. The default is 0 on POR (Figure 36).

Cold or Warm Start *(D7).* This bit is set by the device upon entering STOP mode. A 0 in this bit (cold) indicates that the device will be reset by POR/WDT Reset. A 1 in this bit (warm) indicates that the device awakens by a SMR source. This is a READ only bit.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bit 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved (Figure 39). This register is accessible only during the first 64 processor cycles (128 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 40). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH. It is organized as follows:

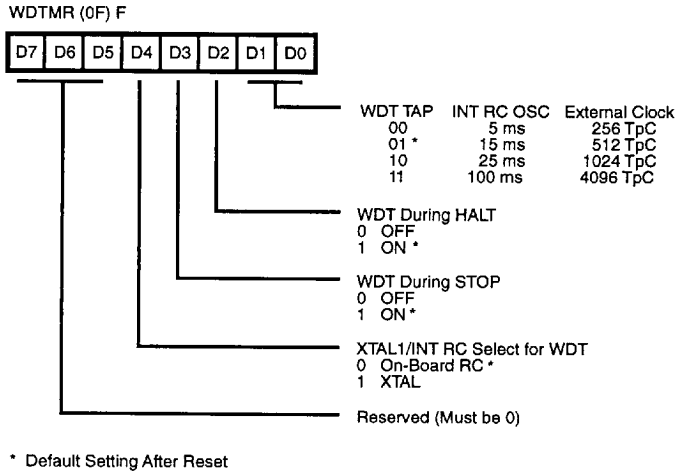


Figure 39. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select *(D0, D1)*. Selects the WDT time period. It is configured as shown in Table 8.

Table 8. WDT Time Select

D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	5 ms min	256 TpC
0	1	15 ms min	512 TpC
1	0	25 ms min	1024 TpC
1	1	100 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle.
The default on reset is 15 ms.
See Figures 28 to 29 for details.

WDTMR During HALT *(D2)*. This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP *(D3)*. This bit determines whether or not the WDT is active during STOP mode. Since the XTAL clock is stopped during STOP mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT *(D4)*. This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.

FUNCTIONAL DESCRIPTION (Continued)

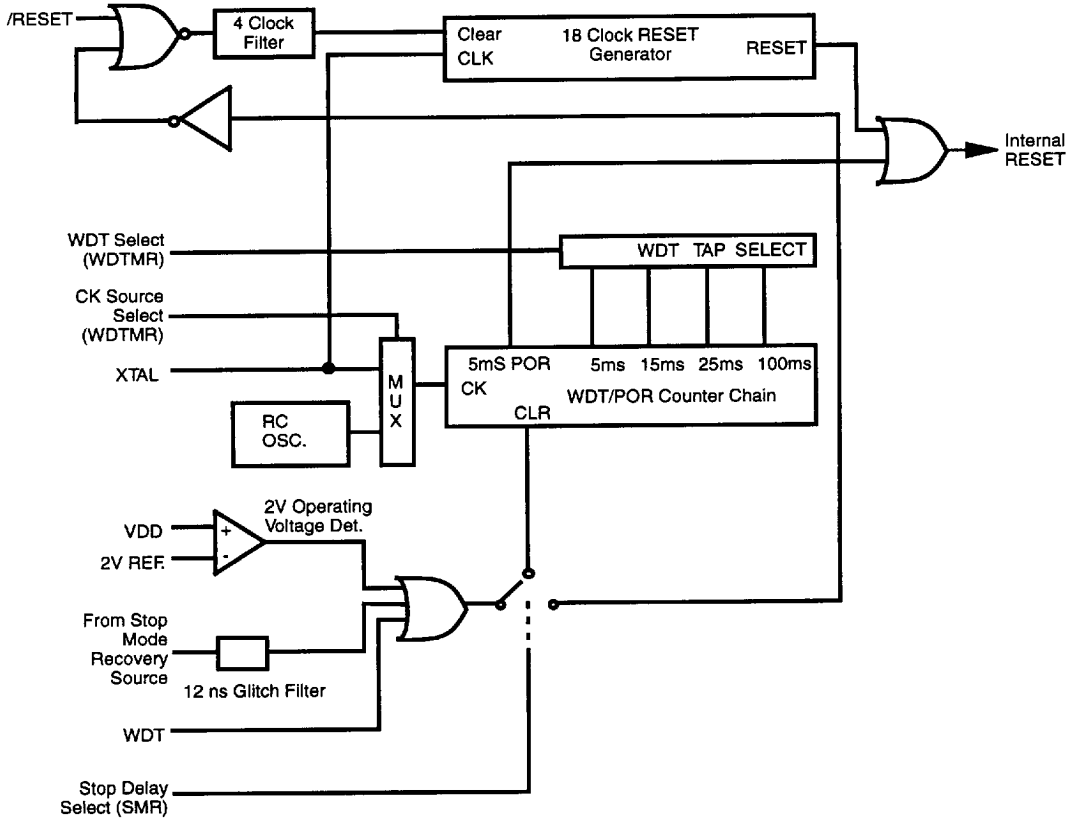


Figure 40. Resets and WDT

Low Voltage Protection. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{LV} (Low Voltage). The minimum operating voltage varies with the temperature and operating frequency, while V_{LV} varies with temperature only.

Mask Selectable Options. There are six Mask Selectable Options to choose from based on ROM code requirements. These are:

RC/Other	Clock Source
Port 0 Pull-ups (lower nibble)	On/Off
Port 0 Pull-ups (upper nibble)	On/Off
Port 2 Pull-ups	On/Off
Port 3 Pull-ups	On/Off
Mouse/Normal	M/N

The Low Voltage trip voltage (V_{LV}) is less than 2.1V under the following conditions:

Maximum (V_{LV}) Conditions:

T_A = 0°C, +55°C Internal clock frequency equal to or less than 4.0 MHz

Note: The internal clock frequency is one-half the external clock frequency.

The device functions normally at or above 2.0V under all conditions. Below 2.0V, the device is guaranteed to function normally until the Low Voltage Protection trip point V_{LV} is reached, below which reset is globally driven. The device is guaranteed to function normally at supply voltages above the V_{LV} trip point for the temperatures and operating frequencies in maximum V_{LV} conditions. The actual V_{LV} trip point is a function of temperature and process parameters (Figure 41).

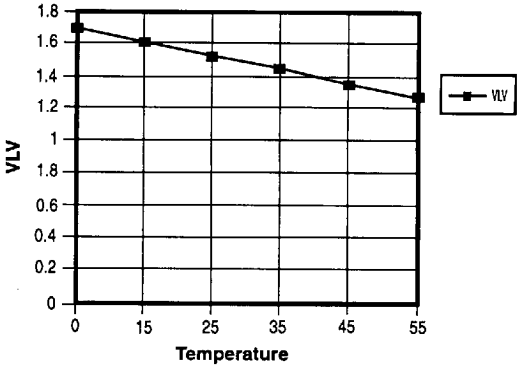


Figure 41. Typical Z86L7X Low Voltage vs Temperature at 8 MHz

3

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp.	–65°	+150°	C
T_A	Oper. Ambient Temp.		†	C

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 42).

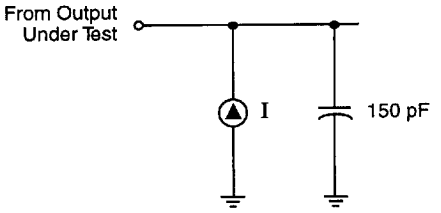


Figure 42. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

DC CHARACTERISTICS

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typ @ 25°C	Units	Conditions	Notes [3]
	Max Input Voltage	2.0V		7		V	I_{IN} 250 µA	
		3.9V		7		V	I_{IN} 250 µA	
V_{CH}	Clock Input High Voltage	2.0V	0.9 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator	
		3.9V	0.9 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
		3.9V	V_{SS} – 0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0V	0.7 V_{CC}	V_{CC} + 0.3	1.3	V		
		3.9V	0.7 V_{CC}	V_{CC} + 0.3	2.5	V		
V_{IL}	Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}	0.5	V		
		3.9V	V_{SS} – 0.3	0.2 V_{CC}	0.9	V		
V_{OH1}	Output High Voltage	2.0V	V_{CC} – 0.4		1.7	V	I_{OH} = –0.5 mA	
		3.9V	V_{CC} – 0.4		3.7	V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage (P36, P37)	2.0V	0.7 V_{CC}			V	I_{OH} = –7 mA	
		3.9V	0.7 V_{CC}			V	I_{OH} = –7 mA	[10]
V_{OL1}	Output Low Voltage	2.0V		0.4	0.2	V	I_{OL} = 1.0 mA	
		3.9V		0.4	0.1	V	I_{OL} = <4.0 mA	
V_{OL2}	Output Low Voltage	2.0V		0.8	0.3	V	I_{OL} = 2.0 mA 3 Pin Max	
		3.9V		0.8	0.5	V	I_{OL} = 8.0 mA 3 Pin Max	
V_{OL2}	Output Low Voltage (P20-P22, P36, P00, P01, P07)	2.0V		0.8	0.3	V	I_{OL} = 10 mA	[9]
		3.9V		0.8	0.5	V	I_{OL} = 10 mA 2 O/P only	
V_{RH}	Reset Input High Voltage	2.0V	0.8 V_{CC}	V_{CC}	1.5	V		
		3.9V	0.8 V_{CC}	V_{CC}	3.0	V		
V_{RI}	Reset Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}	0.5			
		3.9V	V_{SS} – 0.3	0.2 V_{CC}	0.9			
V_{OFFSET}	Comparator Input Offset Voltage	2.0V		25	10	mV		
		3.9V		25	10	mV		
I_{IL}	Input Leakage	2.0V	–1	1	< 1	µA	V_{IN} = 0V, V_{CC}	
		3.9V	–1	1	< 1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	2.0V	–1	1	< 1	µA	V_{IN} = 0V, V_{CC}	
		3.9V	–1	1	< 1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	2.0V		–45	–20	µA		
		3.9V		–55	–30	µA		
I_{CC}	Supply Current	2.0V		10	4	mA	@ 8.0 MHz	[4, 5]
		3.9V		15	10	mA	@ 8.0 MHz	[4, 5]
		2.0V		100	10	µA	@ 32 kHz	[4, 5,11]
		3.9V		300	10	µA	@ 32 kHz	[4, 5,11]

DC CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typ @ 25°C	Units	Conditions	Notes [3]
I_{CC1}	Standby Current	2.0V		3	1	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8.0 MHz	[4,5]
		3.9V		5	4	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8.0 MHz	[4,5]
		2.0V		2	0.8	mA	Clock Divide-by-16 @ 8.0 MHz	[4,5]
		3.9V		4	2.5	mA	Clock Divide-by-16 @ 8.0 MHz	[4,5]
I_{CC2}	Standby Current	2.0V		8	2	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6,8]
		3.9V		10	3	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6,8]
		2.0V		500	310	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6,8]
		3.9V		800	600	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6,8]
T_{POR}	Power-On Reset	2.0V	7.5	75	13	ms		
		3.9V	2.5	20	7	ms		
V_{LV}	V_{CC} Low Voltage Protection			2.15	1.7	V	8 MHz max Ext. CLK Freq.	[7]

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Frequency
Crystal/Resonator	3.0 mA	5	mA	8.0 MHz
External Clock Drive	0.3 mA	5	mA	8.0 MHz

[2] GND = 0V
[3] 2.0V to 3.9V
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] CL1 = CL2 = 100 pF
[6] Same as note [4] except inputs at V_{CC}.
[7] The V_{LV} increases as the temperature decreases.
[8] Oscillator stopped.
[9] Two outputs at a time, independent to other outputs.
[10] One at a time.
[11] 32 kHz clock driver input.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram

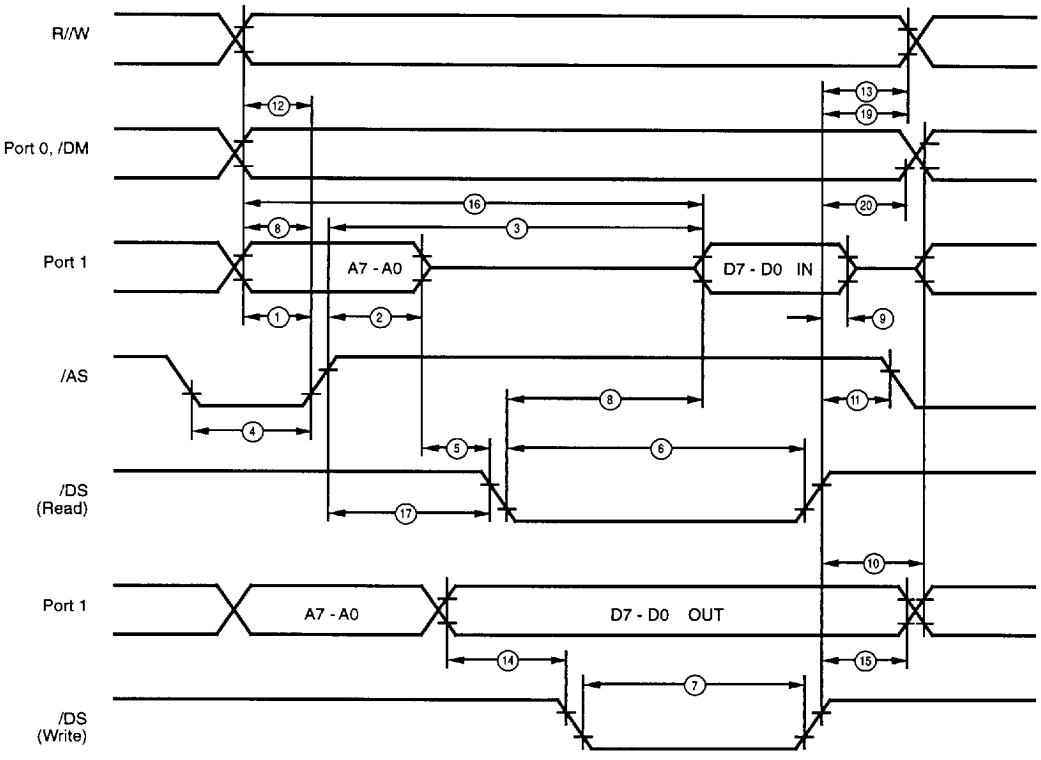


Figure 43. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Table

No.	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C 8.0 MHz Min	Max	Units	Notes
1	TdA(AS)	Address Valid to	2.0V	55		ns	[2]
		/AS Rising Delay	3.9V	55		ns	
2	TdAS(A)	/AS Rising to Address	2.0V	70		ns	[2]
		Float Delay	3.9V	70		ns	
3	TdAS(DR)	/AS Rising to Read	2.0V		400	ns	[1, 2]
		Data Required Valid	3.9V		400	ns	
4	TwAS	/AS Low Width	2.0V	80		ns	[2]
			3.9V	80		ns	
5	Td	Address Float to	2.0V	0		ns	
		/DS Falling	3.9V	0		ns	
6	TwDSR	/DS (Read) Low Width	2.0V	300		ns	[1, 2]
			3.9V	300		ns	
7	TwDSW	/DS (Write) Low Width	2.0V	165		ns	[1, 2]
			3.9V	165		ns	
8	TdDSR(DR)	/DS Falling to Read	2.0V		260	ns	[1, 2]
		Data Required Valid	3.9V		260	ns	
9	ThDR(DS)	Read Data to	2.0V	0		ns	[2]
		/DS Rising Hold Time	3.9V	0		ns	
10	TdDS(A)	/DS Rising to Address	2.0V	85		ns	[2]
		Active Delay	3.9V	95		ns	
11	TdDS(AS)	/DS Rising to /AS	2.0V	60		ns	[2]
		Falling Delay	3.9V	70		ns	
12	TdR/W(AS)	R/W Valid to /AS	2.0V	70		ns	[2]
		Rising Delay	3.9V	70		ns	
13	TdDS(R/W)	/DS Rising to	2.0V	70		ns	[2]
		R/W Not Valid	3.9V	70		ns	
14	TdDW(DSW)	Write Data Valid to /DS	2.0V	80		ns	[2]
		Falling (Write) Delay	3.9V	80		ns	
15	TdDS(DW)	/DS Rising to Write	2.0V	70		ns	[2]
		Data Not Valid Delay	3.9V	80		ns	
16	TdA(DR)	Address Valid to Read	2.0V		475	ns	[1, 2]
		Data Required Valid	3.9V		475	ns	
17	TdAS(DS)	/AS Rising to	2.0V	100		ns	[2]
		/DS Falling Delay	3.9V	100		ns	
18	TdDM(AS)	/DM Valid to /AS	2.0V	55		ns	[2]
		Falling Delay	3.9V	55		ns	
19	TdDS(DM)	/DS Rise to	2.0V			ns	
		/DM Valid Delay	3.9V			ns	
20	ThDS(A)	/DS Rise to Address	2.0V			ns	
		Valid Hold Time	3.9V			ns	

Notes:
[1] When using extended memory timing add 2 TpC.
[2] Timing numbers given are for minimum TpC.
[3] 2.0V to 3.9V
Standard Test Load
All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC CHARACTERISTICS
Additional Timing Diagram

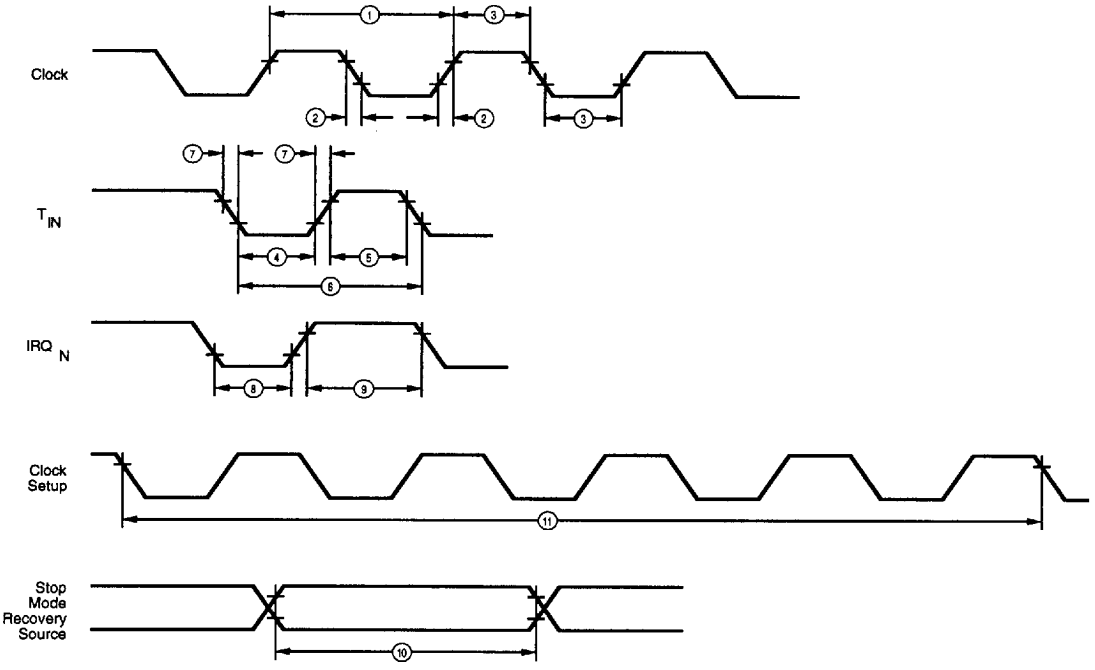


Figure 44. Additional Timing

AC CHARACTERISTICS
Additional Timing Table

No	Symbol	Parameter		V_{CC} Note [3]	T_A = 0°C to +70°C 8.0 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period		2.0V	121	DC	ns	[1]
				3.9V	121	DC	ns	[1]
2	TrC,TfC	Clock Input Rise		2.0V		25	ns	[1]
		and Fall Times		3.9V		25	ns	[1]
3	TwC	Input Clock Width		2.0V	37		ns	[1]
				3.9V	37		ns	[1]
4	TwTinL	Timer Input		2.0V	100		ns	[1]
		Low Width		3.9V	70		ns	[1]
5	TwTinH	Timer Input		2.0V	3TpC			[1]
		High Width		3.9V	3TpC			[1]
6	TpTin	Timer Input Period		2.0V	8TpC			[1]
				3.9V	8TpC			[1]
7	TrTin,TfTin	Timer Input Rise		2.0V		100	ns	[1]
		and Fall Timers		3.9V		100	ns	[1]
8A	TwIL	Interrupt Request		2.0V	100		ns	[1, 2]
		Low Time		3.9V	70		ns	[1, 2]
8B	TwIL	Int. Request		2.0V	3TpC			[1, 3]
		Low Time		3.9V	3TpC			[1, 3]
9	TwIH	Interrupt Request		2.0V	3TpC			[1, 2]
		Input High Time		3.9V	3TpC			[1, 2]
10	Twsm	Stop-Mode Recovery		2.0V	12		ns	
		Width Spec		3.9V	12		ns	
				2.0V	5TpC			[7]
				3.9V	5TpC			[8]
11	Tost	Oscillator		2.0V		5TpC		[4]
		Start-up Time		3.9V		5TpC		[4]
12	Twdt	Watch-Dog Timer	(5 ms)	2.0V	12	75	ms	D0 = 0 [5]
		Delay Time		3.9V	5	20	ms	D1 = 0 [5]
			(15 ms)	2.0V	25	150	ms	D0 = 1 [5]
				3.9V	10	40	ms	D1 = 0 [5]
			(25 ms)	2.0V	50	300	ms	D0 = 0 [5]
				3.9V	25	80	ms	D1 = 1 [5]
			(100 ms)	2.0V	225	1200	ms	D0 = 1 [5]
				3.9V	100	320	ms	D1 = 1 [5]

Notes:
[1] Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).
[3] Interrupt request through Port 3 (P30).
[4] SMR – D5 = 0
[5] Reg. WDTMR
[6] 2.0V to 3.9V
[7] Reg. SMR – D5 = 0
[8] Reg. SMR – D5 = 1

AC CHARACTERISTICS
Handshake Timing Diagrams

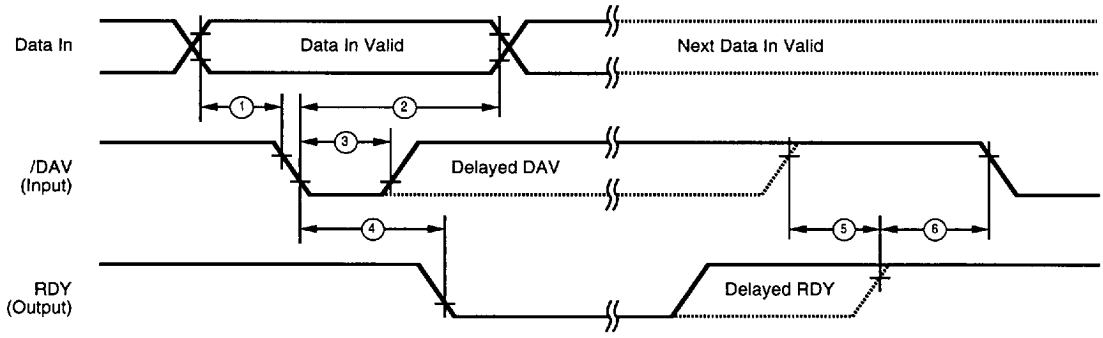


Figure 45. Input Handshake Timing

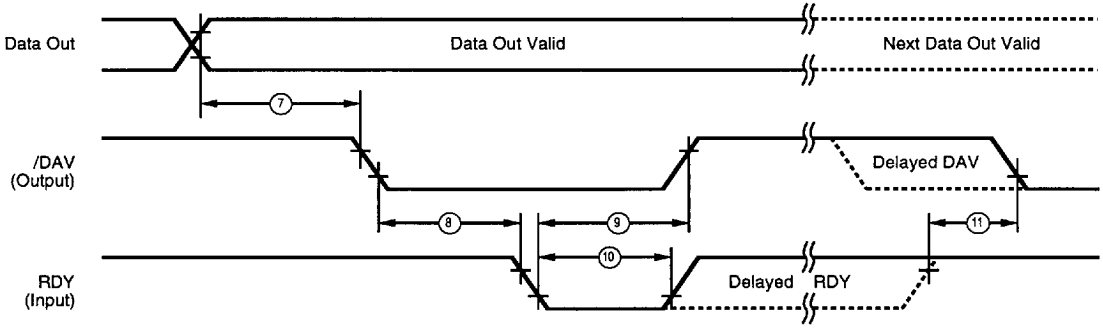


Figure 46. Output Handshake Timing

AC CHARACTERISTICS
Handshake Timing Table

No	Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to +70°C 8.0 MHz Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	2.0V	0		IN
			3.9V	0		IN
2	ThDI(DAV)	Data In Hold Time	2.0V	160		IN
			3.9V	115		IN
3	TwDAV	Data Available Width	2.0V	155		IN
			3.9V	110		IN
4	TdDAVI(RDY)	DAV Falling to RDY	2.0V		160	IN
		Falling Delay	3.9V		115	IN
5	TdDAVId(RDY)	DAV Rising to RDY	2.0V		120	IN
		Falling Delay	3.9V		80	IN
6	TdRDYO(DAV)	RDY Rising to DAV	2.0V	0		IN
		Falling Delay	3.9V	0		IN
7	TdDO(DAV)	Data Out to DAV	2.0V	63		OUT
		Falling Delay	3.9V	63		OUT
8	TdDAV0(RDY)	DAV Falling to RDY	2.0V	0		OUT
		Falling Delay	3.9V	0		OUT
9	TdRDY0(DAV)	RDY Falling to DAV	2.0V		160	OUT
		Rising Delay	3.9V		115	OUT
10	TwRDY	RDY Width	2.0V	110		OUT
			3.9V	80		OUT
11	TdRDY0d(DAV)	RDY Rising to DAV	2.0V		110	OUT
		Falling Delay	3.9V		80	OUT

Note:
[3] 2.0V to 3.9V

EXPANDED REGISTER FILE CONTROL REGISTERS (0D)

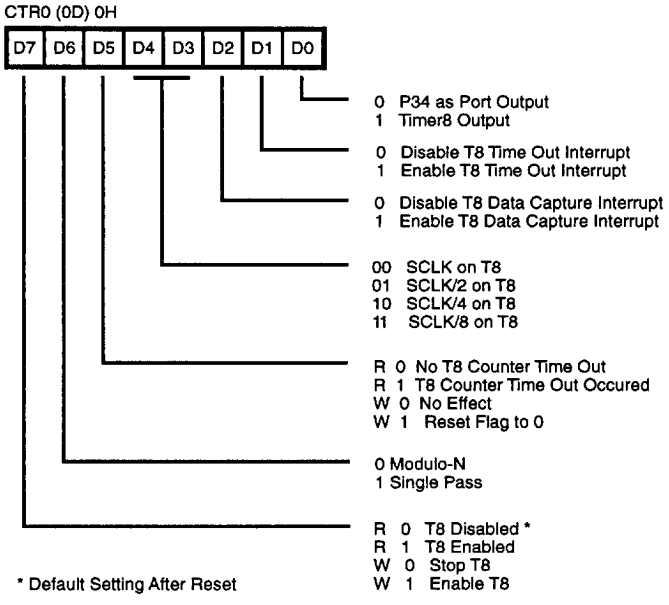


Figure 47. TC8 Control Register ((0D) 0H: Read/Write Accept Where Noted)

3

EXPANDED REGISTER FILE CONTROL REGISTERS (0D) (Continued)

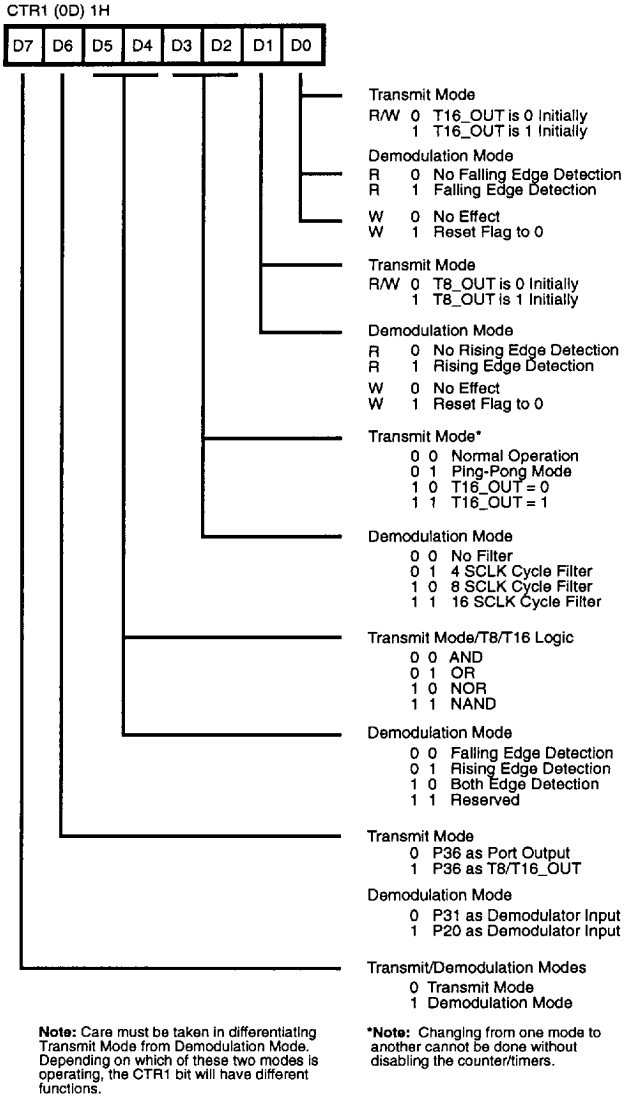


Figure 48. T8 and T16 Common Control Functions ((0D) 1H: Read/Write)

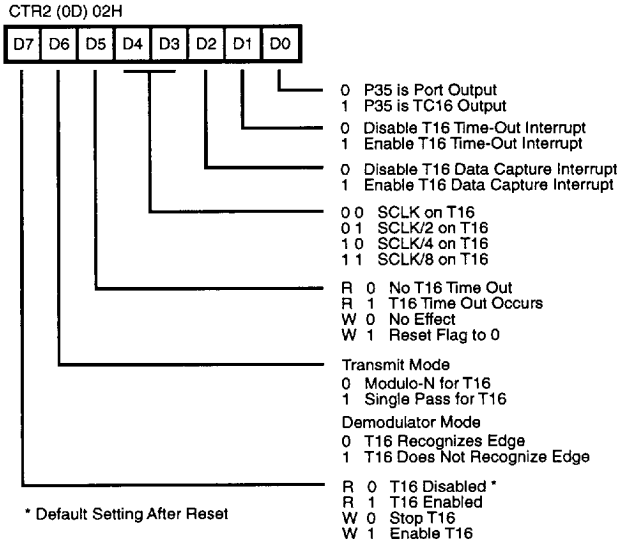
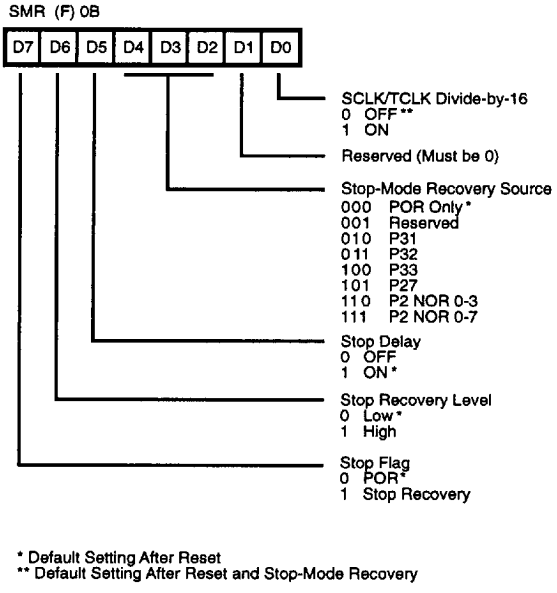


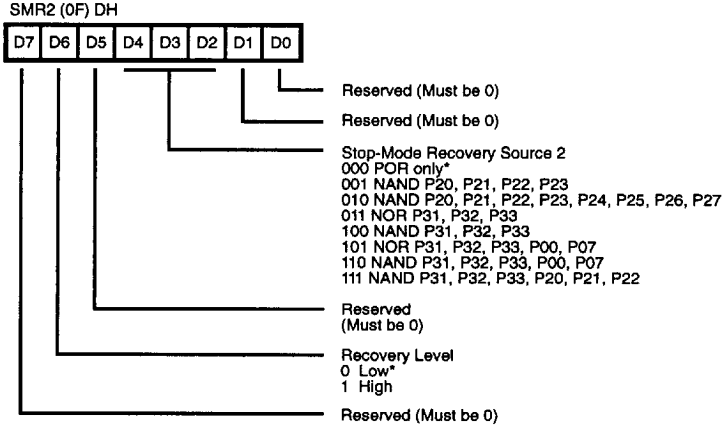
Figure 49. T16 Control Register
((0D) 2H: Read/Write Except Where Noted)

EXPANDED REGISTER FILE CONTROL REGISTERS (0F)



* Default Setting After Reset
** Default Setting After Reset and Stop-Mode Recovery

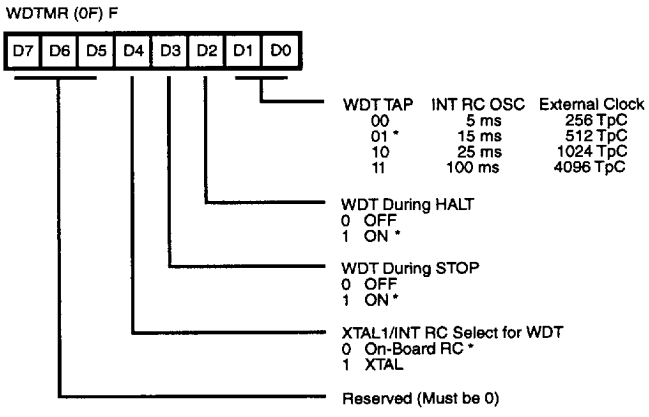
Figure 50. Stop-Mode Recovery Register ((F)0BH: D6-D0 = Write Only, D7 = Read Only)



Note: If used in conjunction with SMR, either of the two specified events will cause a Stop-Mode Recovery.

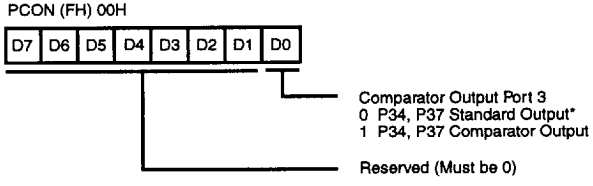
*Default Setting After Reset

Figure 51. Stop-Mode Recovery Register 2 ((0F) DH: D2-DH, D6 Write Only)



* Default Setting After Reset

Figure 52. Watch-Dog Timer Mode Register ((F) 0FH: Write Only)



* Default Setting After Reset
P37 comparator output only on E72 and L72

Figure 53. Port Configuration Register (PCON) ((0F) 0H: Write Only)

Z8 STANDARD CONTROL REGISTER DIAGRAMS

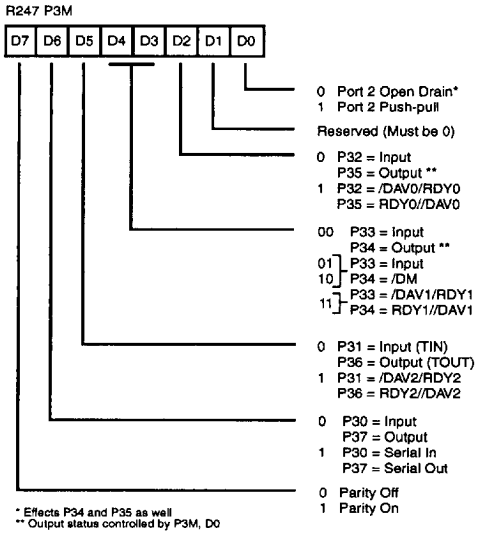


Figure 54. Port 3 Mode Register (F7H:Write Only)

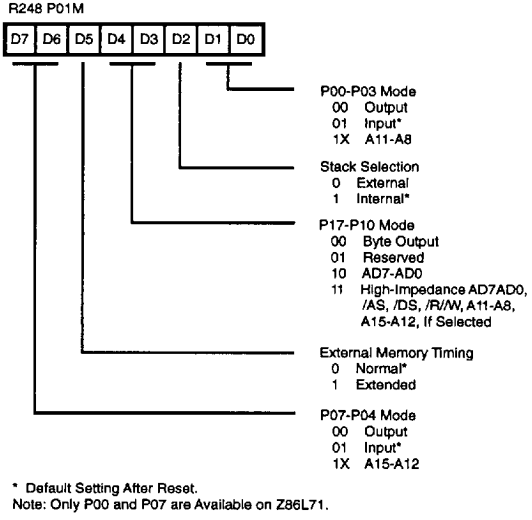


Figure 55. Port 0 and 1 Mode Register (F8H: Write Only)

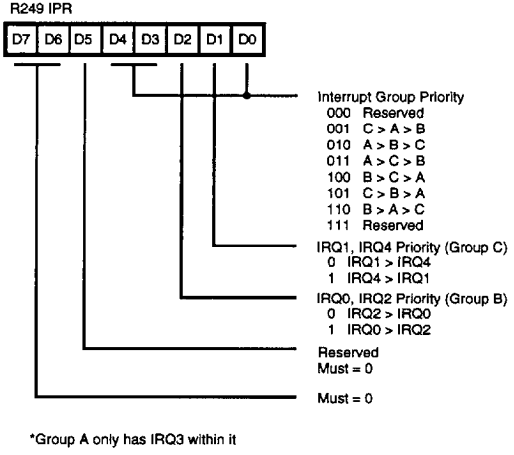


Figure 56. Interrupt Priority Registers ((0)F9H:Write Only)

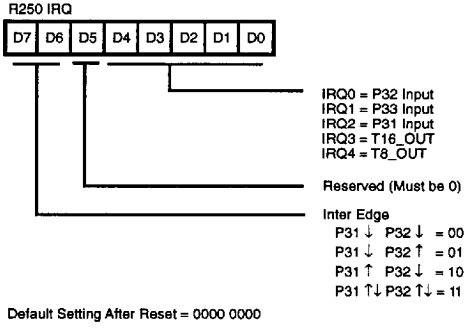


Figure 57. Interrupt Request Register ((0)FAH:Read/Write)

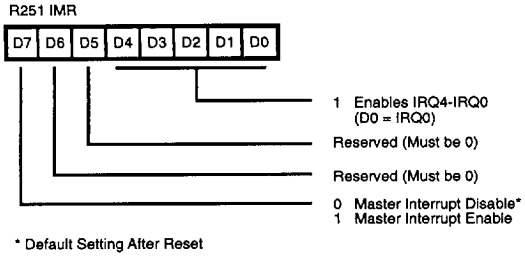


Figure 58. Interrupt Mask Register ((0)FBH:Read/Write)

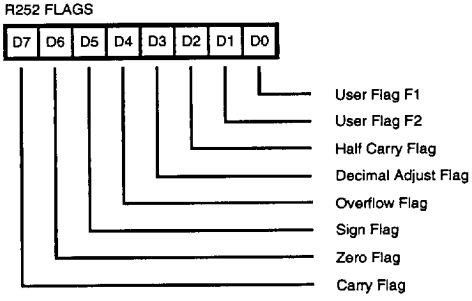


Figure 59. Flag Register ((0)FCH:Read/Write)

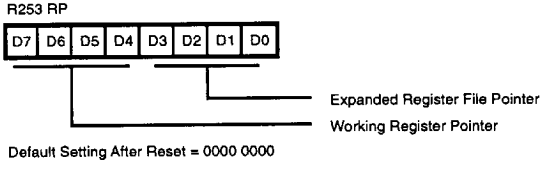


Figure 60. Register Pointer ((0)FDH:Read/Write)

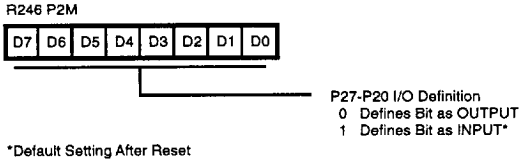


Figure 61. Port 2 Mode Register (F6H:Write Only)

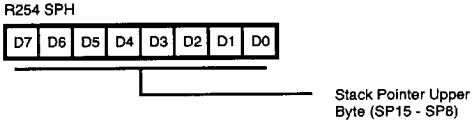


Figure 62. Stack Pointer High ((0)FEH:Read/Write)

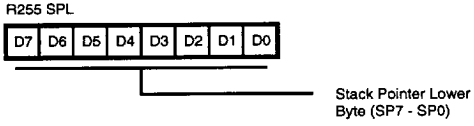


Figure 63. Stack Pointer Low ((0)FFH:Read/Write)

3

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

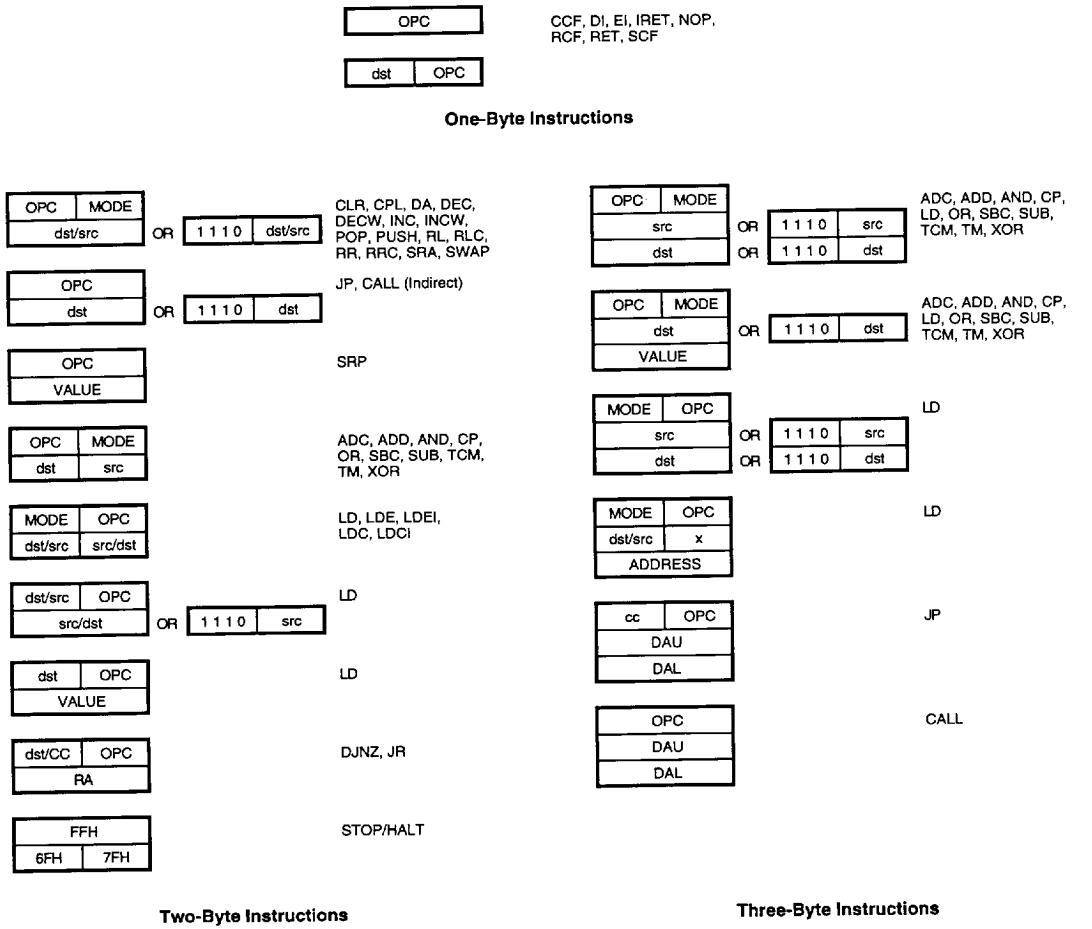
Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

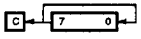
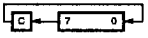
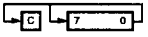
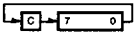
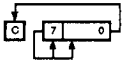
INSTRUCTION SUMMARY (Continued)

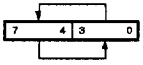
Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src + C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R IR R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst←src	r Irr	Irr r	C2 D2	-	-	-	-	-	-
LDCI dst, src dst←src r←r + 1;rr←rr + 1	Ir Irr	Irr Ir	C3 D3	-	-	-	-	-	-
LDE dst, src dst←src	r Irr	Irr Ir	82 92	-	-	-	-	-	-
LDEI dst, src dst←src r←r + 1;rr←rr + 1	Ir Irr	Irr Ir	83 93	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-

3

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP – 1; @SP←src	R IR		70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP dst RP←src	Im		31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
WDT			5F	-	X	X	X	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

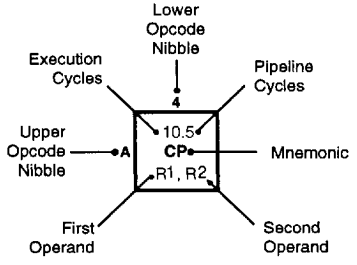
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1	12.0 **LDE** r1, Irr2	18.0 **LDEI** Ir1, Irr2												6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1	12.0 **LDE** r2, Irr1	18.0 **LDEI** Ir2, Irr1												6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2					3	1	



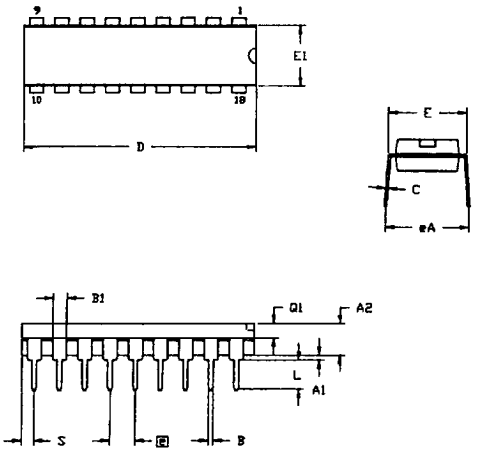
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

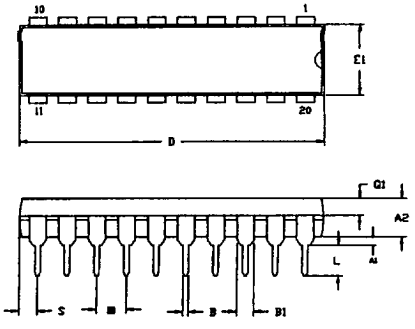
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
■	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

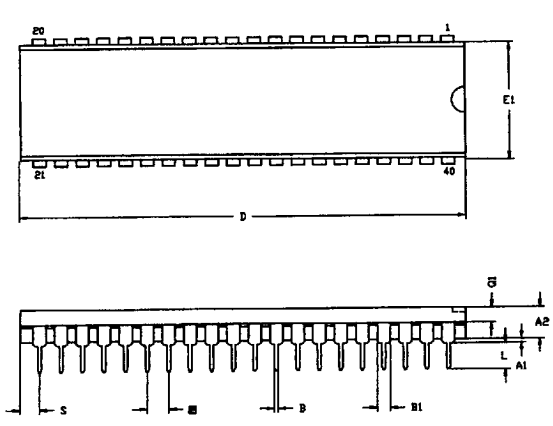
18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	-	.015	-
A2	3.25	3.68	.128	.145
B	0.41	0.51	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
■	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

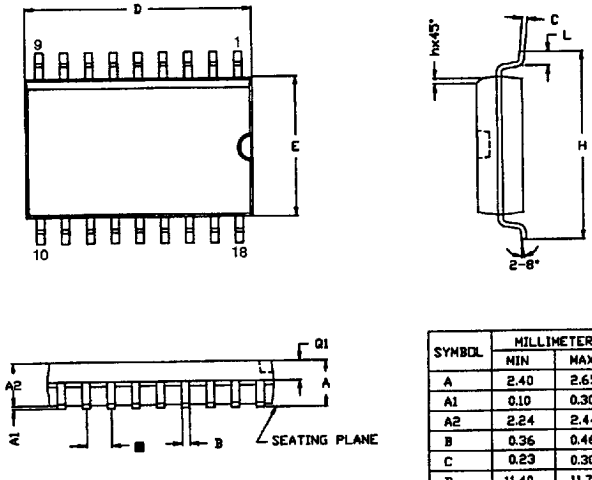
20-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

40-Pin DIP Package Diagram

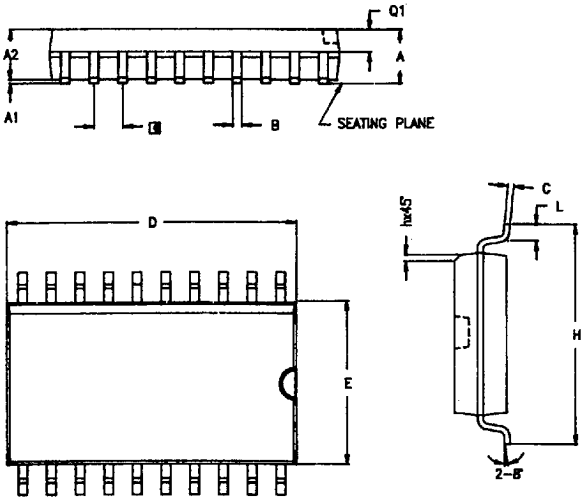


CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	11.40	11.75	.449	.463
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

18-Pin SOIC Package Diagram

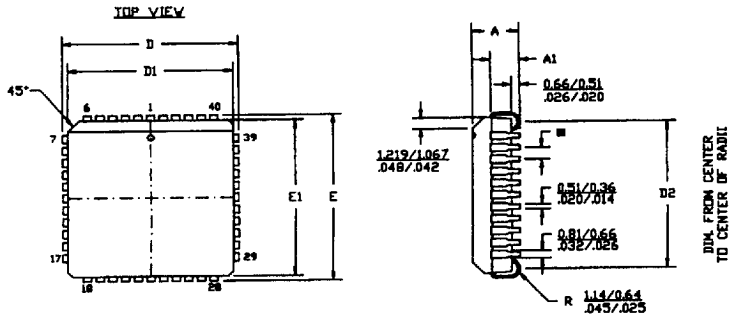
PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	.496	.510
E	7.40	7.60	.291	.299
e	1.27 TYP		.050 TYP	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

20-Pin SOIC Package Diagram



NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.67	2.92	.105	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
■	1.27 TYP		.050 TYP	

44-Pin PLCC Package Diagram

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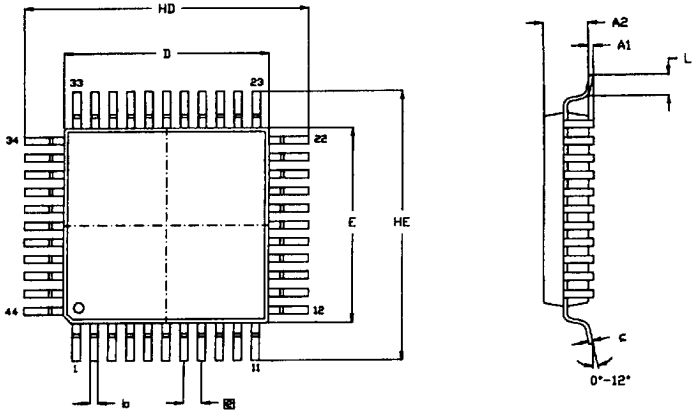
PACKAGE INFORMATION (Continued)



NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 mm .004"

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
e	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

44-Pin QFP Package Diagram

ORDERING INFORMATION

Z86L70/71/72/75/76

8.0 MHz

18-pin DIP	20-pin DIP	40-pin DIP	
Z86L7008PSC	Z86L7108PSC	Z86L7208PSC	
Z86L7508PSC		Z86L7608PSC	
18-pin SOIC	**20-pin SOIC**	**44-pin PLCC**	**44-pin QFP**
Z86L7008SSC	Z86L7108SSC	Z86L7208VSC	Z86L7208FSC
Z86L7608SSC		Z86L7608VSC	Z86L7608FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Codes

Package
P = Plastic DIP
F = Plastic Quad Flat Pack
V = Plastic Chip Carrier

Temperature
S = 0°C to +70°C

Speed
08 = 8.0 MHz

Environmental
C = Plastic Standard

Example:

Z 86L71 08 P S C is a Z86L70, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 08 — Speed
- 86L71 — Product Number
- Z — Zilog Prefix

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