Z86L79/L80

IR/LOW-VOLTAGE MICROCONTROLLER

FEATURES

Part	ROM (KB)	RAM* (Bytes)	I/O	Voltage Range
Z86L79	4	237	24	2.0V to 3.9V
Z86L80	8	237	24	2.0V to 3.9V

Note: *General-Purpose

- Three Standby Modes (Typical)
  - STOP - 2 µA
  - HALT - 0.8 mA
  - Low-Voltage Standby ($<V_{LV}$)
- Expanded Register File Control Registers
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Registers
  - One Programmable 16-Bit Counter/Timer with One Capture Register
  - Programmable Input Glitch Filter for Pulse Reception
- Five Priority Interrupts
- Low-Voltage Detection and Standby Mode
- Watch-Dog/Power-On Reset Circuits
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive
- Mask-Selectable 200-KOhm Pull-Ups on Ports 0, 2, 3
  - Port 2 Pull-Ups are Bit Selectable
  - Pull-Ups Automatically Disabled as Outputs
- Maskable Single-Trip-Point Inputs on P00 Through P03.
- Permanently Enabled WDT Option (Maskable)
- 28-Pin DIP and SOIC Packages

GENERAL DESCRIPTION

The Z86L79/L80 family of IR (Infrared) Remote Controllers are ROM-based members of the Z8® MCU single-chip family with 237 bytes of general-purpose RAM. The only differentiating factor between these two versions is the availability of ROM. Zilog's CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion along with cost-effective and low power consumption.

The Z86L79/80 architecture is based on Zilog's 8-bit Microcontroller core with an Expanded Register File to allow access to register-mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z8® MCU offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery operated hand-held applications.

Z8 applications demand powerful I/O capabilities. The Z86L79/80 fulfills this with two package options with 24 pins of dedicated input and output. These lines are grouped into three ports. Each port consists of eight lines and is configurable under software control to provide timing, status signals, and parallel I/O.

GENERAL DESCRIPTION (Continued)

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File, and Expanded Register File. The Register File is composed of 256 bytes of RAM. It includes four I/O port registers, ten control and status registers, and the rest are general purpose registers. The Expanded Register File consists of three register groups.

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86L79/80 family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

Notes: All Signals with a preceding front slash, "/", are active Low, for example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

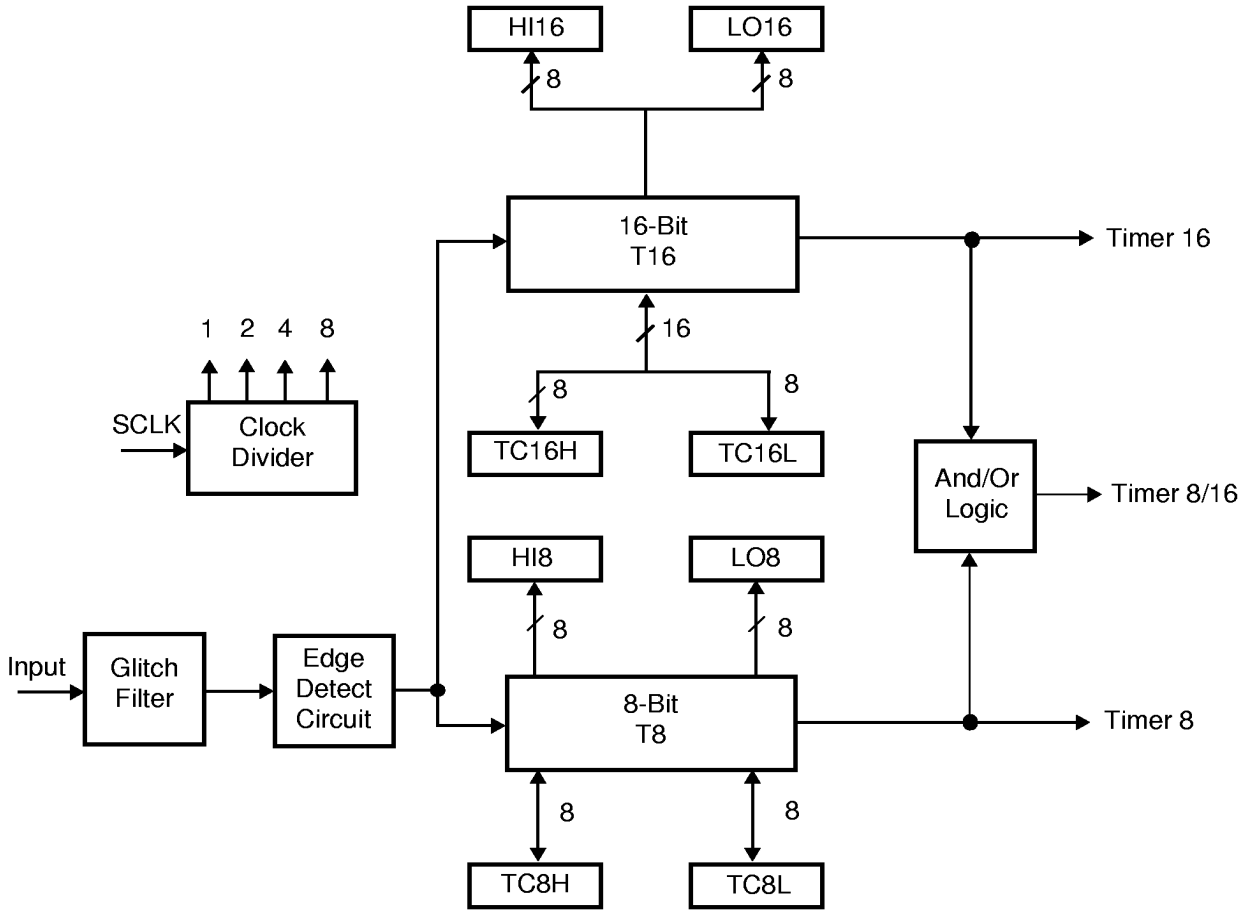


Figure 1. Counter/Timer Block Diagram

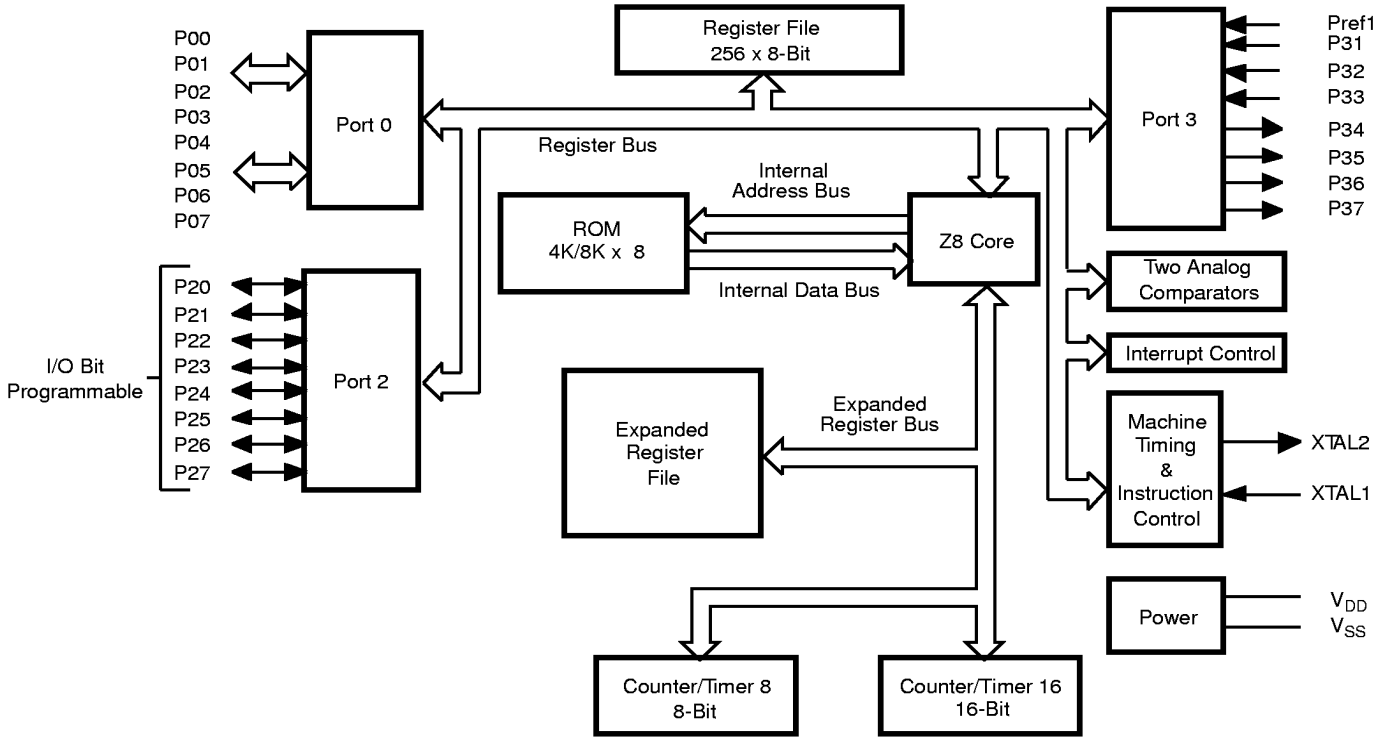


Figure 2. Functional Block Diagram

PIN DESCRIPTION

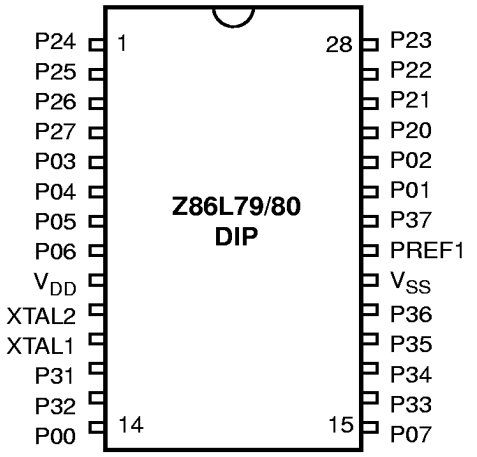


Figure 3. 28-Pin DIP/SOIC Pin Assignments

Table 1. Pin Identification

28-Pin DIP & SOIC	Symbol	Direction	Description
14	P00	Input/Output	Port 0 is Nibble Programmable.
23	P01	Input/Output	
24	P02	Input/Output	
5	P03	Input/Output	
6	P04	Input/Output	Port 0 can be configured as a 0.4 V_{DD} single-trip point.
7	P05	Input/Output	
8	P06	Input/Output	
15	P07	Input/Output	
25	P20	Input/Output	Port 2 pins are individually configurable as input or output.
26	P21	Input/Output	

Table 1. Pin Identification

28-Pin DIP & SOIC	Symbol	Direction	Description
27	P22	Input/Output	
28	P23	Input/Output	
1-4	P24-P27	Input/Output	
21	Pref1	Input	Analog Ref Input
12	P31	Input	IRQ2/Modulator Input
13	P32	Input	IRQ0
16	P33	Input	IRQ1
17	P34	Output	T8 Output
18	P35	Output	T16 Output
19	P36	Output	T8/T16 Output
22	P37	Output	
11	XTAL1	Input	Crystal, Oscillator Clock
10	XTAL2	Output	Crystal, Oscillator Clock
9	V_{DD}		Power Supply
20	V_{SS}		Ground

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp.	–65°	+150°	C
T_A	Oper. Ambient Temperature		†	C

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 4).

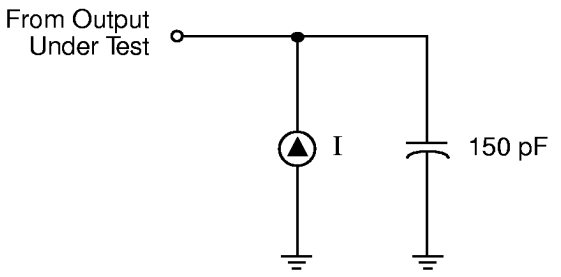


Figure 4. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

Precaution: SMR Reg 0B hex BANK F Bit D1 must be 0.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
	Max Input Voltage	2.0V		7		V	I_{IN} <250 µA	
		3.9V		7		V	I_{IN} <250 µA	
V_{CH}	Clock Input High Voltage	2.0V	0.9 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator	
		3.9V	0.9 V_{CC}	V_{CC} + 0.3		V		
V_{CL}	Clock Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
		3.9V	V_{SS}– 0.3	0.2 V_{CC}		V		
V_{IH}	Input High Voltage	2.0V	0.7 V_{CC}	V_{CC} + 0.3	1.0	V		
		3.9V	0.7 V_{CC}	V_{CC} + 0.3	2.0	V		
V_{IL}	Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}	0.5	V		
		3.9V	V_{SS} – 0.3	0.2 V_{CC}	0.9	V		
V_{OH1}	Output High Voltage	2.0V	V_{CC} – 0.4		1.7	V	I_{OH} = –0.5 mA	
		3.9V	V_{CC} – 0.4		3.7	V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage (P36)	2.0V	V_{CC} - .8			V	I_{OH} = –7 mA	
		3.9V	V_{CC} - .8			V	I_{OH} = –7 mA	
V_{OL1}	Output Low Voltage	2.0V		0.4	0.2	V	I_{OL} = 1.0 mA	
		3.9V		0.4	0.1	V	I_{OL} = 1.0 mA	
V_{OL2}	Output Low Voltage	2.0V		0.8	0.3	V	I_{OL} = 2.0 mA	
		3.9V		0.8	0.3	V	I_{OL} = 2.0 mA	
	Output Low Voltage (P20-P22, P36)	2.0V		0.8	0.3	V	I_{OL} = 10 mA	8
		3.9V		0.8	0.5	V	I_{OL} = 10 mA 2 Pin max.	
V_{OFFSET}	Comparator Input Offset Voltage	2.0V		25	10	mV		11
		3.9V		25	10	mV		
I_{IL}	Input Leakage	2.0V	–1	1	<1	µA	V_{IN} = 0V, V_{CC}	
		3.9V	–1	1	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	2.0V	–1	1	<1	µA	V_{IN} = 0V, V_{CC}	
		3.9V	–1	1	<1	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	2.0V		10	4	mA	@ 8.0 MHz	3, 4
		3.9V		15	10	mA	@ 8.0 MHz	
		2.0V		100	10	µA	@ 32 kHz	3, 10
		3.9V		300	10	µA	@ 32 kHz	
I_{CC1}	Standby Current - HALT Mode	2.0V		3	1	mA	V_{IN} = 0V, V_{CC}	4, 5
		3.9V		5	4	mA	@ 8.0 MHz	
		2.0V		2	0.8	mA	Clock Divide-by-	
		3.9V		4	2.5	mA	16 @ 8.0 MHz	
I_{CC2}	Standby Current- STOP Mode	2.0V		8	1	µA	V_{IN} = 0V, V_{CC}	5, 7
		3.9V		10	2	µA	WDT is not Running	
		2.0V		500	310	µA	V_{IN} = 0V, V_{CC}	5, 7
		3.9V		800	600	µA	WDT is Running	
V_{ICR}	Input Common Mode Voltage Range	2.0V	0	V_{CC}-1.0V		V		11
		3.9V	0	V_{CC}-1.0V		V		

Symbol	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
T_{POR}	Power-On Reset	2.0V	7.5	75	13	ms		
		3.9V	2.5	20	7	ms		
V_{LV}	V_{CC} Low Voltage Protection			2.15	1.7	V	4 MHz max Int. CLK Freq	6

Notes:

1. V_{SS} = 0V = GND
2. V_{CC} Range: 2.0V to 3.9V, typical values measured at 3.3V.
3. All outputs unloaded, I/O pins floating, inputs at rail.
4. $C_{L1} = C_{L2}$ = 22 pF
5. Same as note [3] except P3 inputs at V_{CC}.
6. The V_{LV} increases as the temperature decreases.
7. Oscillator stopped
8. Two outputs at a time, independent of other outputs.
9. 32-kHz clock driver input
10. WDT not running
11. For analog comparator, inputs when analog comparators are enabled.

AC CHARACTERISTICS

Timing Diagram

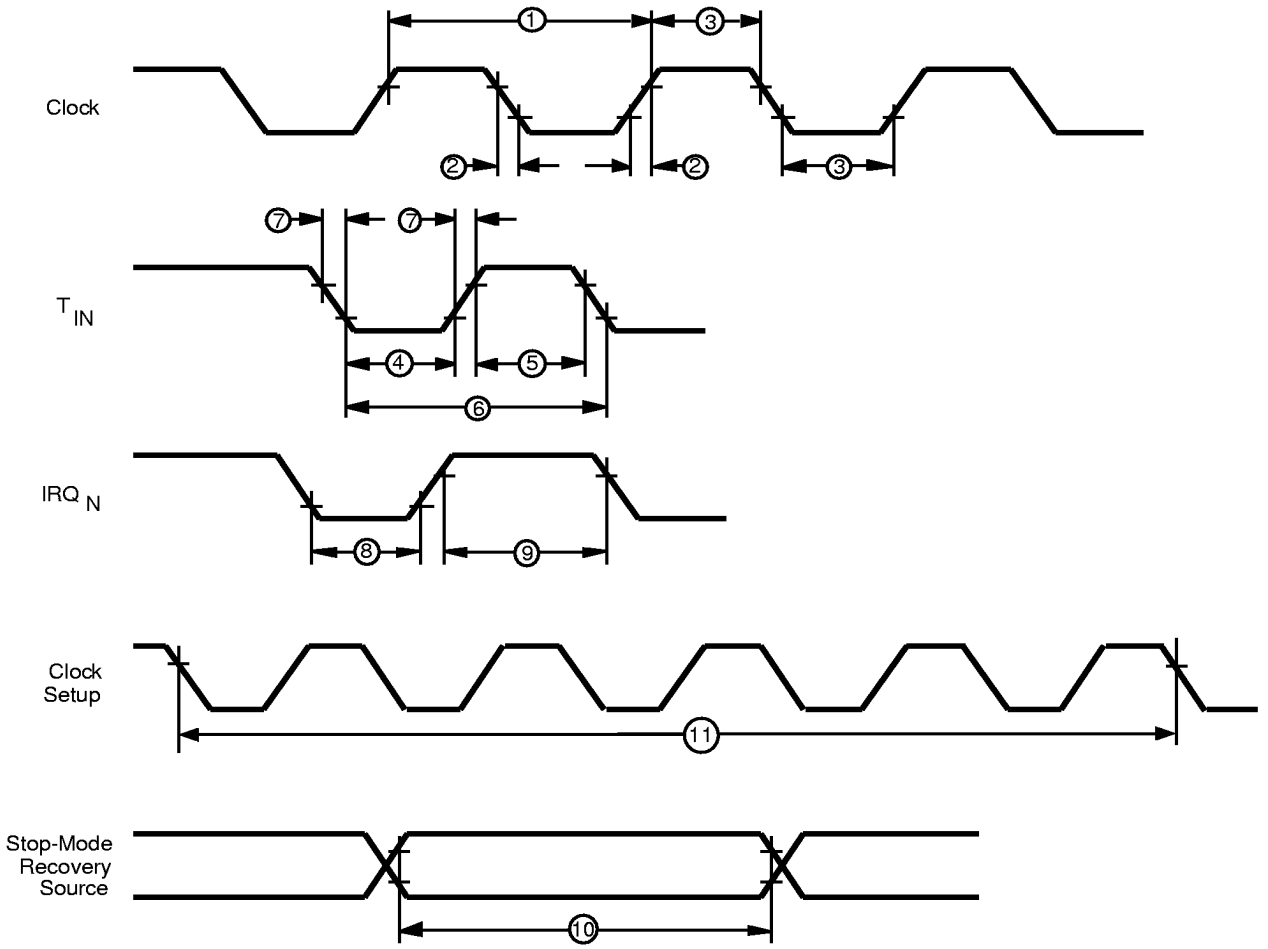


Figure 5. Timing

AC CHARACTERISTICS

Timing Table

No	Symbol	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Units		Notes	
1	TpC	Input Clock Period	2.0V	121	DC	ns		1	
			3.9V	121	DC	ns		1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0V		25	ns		1	
			3.9V		25	ns		1	
3	TwC	Input Clock Width	2.0V	37		ns		1	
			3.9V	37		ns		1	
4	TwTinL	Timer Input Low Width	2.0V	100		ns			
			3.9V	70		ns			
5	TwTinH	Timer Input High Width	2.0V	3TpC				1	
			3.9V	3TpC				1	
6	TpTin	Timer Input Period	2.0V	8TpC				1	
			3.9V	8TpC				1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0V		100	ns		1	
			3.9V		100	ns		1	
8A	TwIL	Interrupt Request Low Time	2.0V	100		ns		1, 2	
			3.9V	70		ns		1, 2	
8B	TwIL	Interrupt Request Low Time	2.0V	3TpC				1, 3	
			3.9V	3TpC				1, 3	
9	TwIH	Interrupt Request Input High Time	2.0V	3TpC				1, 2	
			3.9V	3TpC				1, 2	
10	Twsm	Stop-Mode Recovery Width	2.0V	12		ns		8	
			3.9V	12		ns		8	
			2.0V	5TpC		ns		7	
			3.9V	5TpC		ns		7	
11	Tost	Oscillator Start-up Time	2.0V		5TpC			4	
			3.9V		5TpC			4	
12	Twdt	Watch-Dog Timer Delay Time						WDTMR D1	D0
			2.0V	12	75	ms	5	0	0
			3.9V	5	20	ms	5		
			2.0V	25	150	ms	5	0	1
			3.9V	10	40	ms	5		
			2.0V	50	300	ms	5	1	0
			3.9V	20	80	ms	5		
			2.0V	225	1200	ms	5	1	1
			3.9V	80	320	ms	5		

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Interrupt request through Port 3 (P30).
4. SMR – D5 = 0
5. Reg. WDTMR
6. V_{CC} Range: 2.0V to 3.9V
7. Reg. SMR – D5 = 0
8. Reg. SMR – D5 = 1

AC CHARACTERISTICS

Handshake Timing Diagram

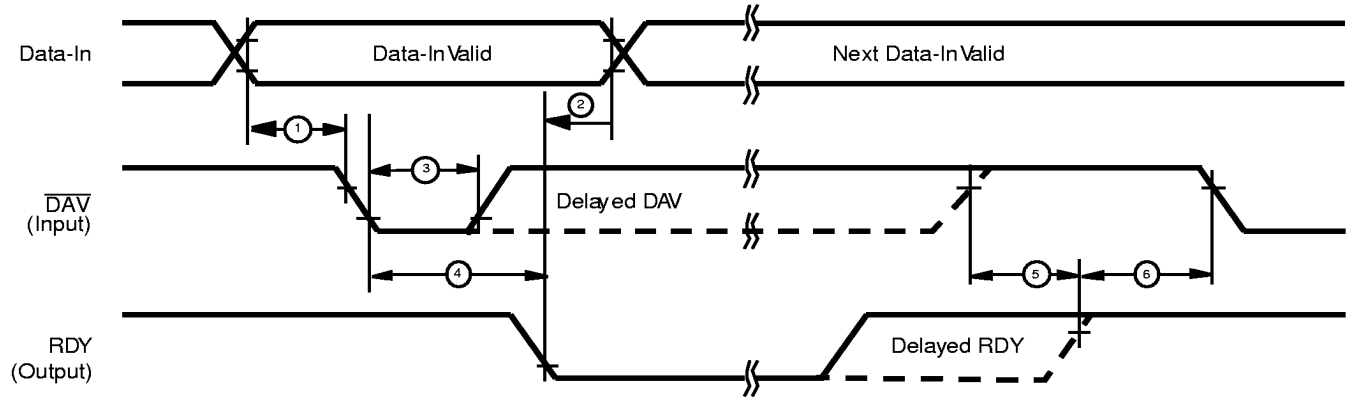


Figure 6. Port I/O with Input Handshake Timing

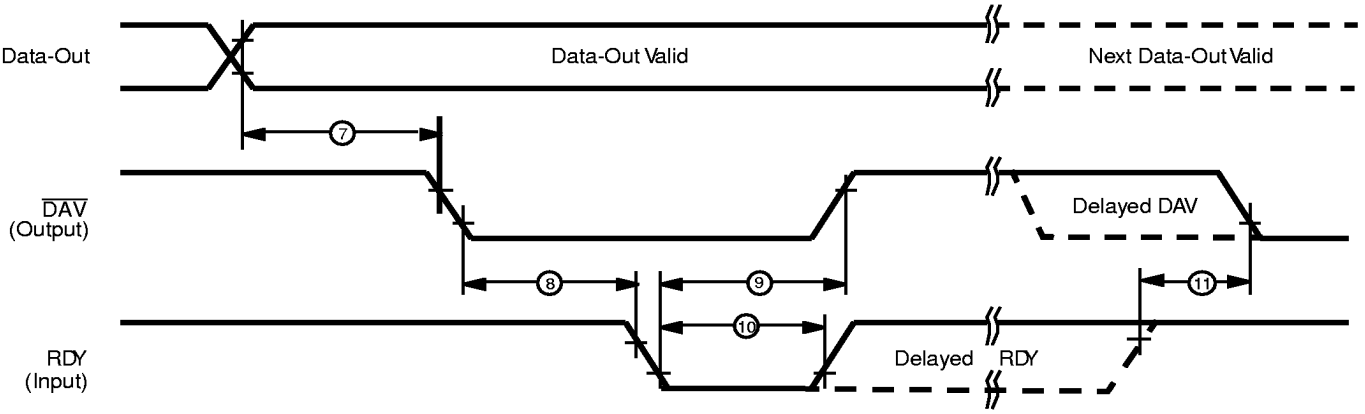


Figure 7. Port I/O with Output Handshake Timing

AC CHARACTERISTICS

Handshake Timing Table

No	Symbol	Parameter	V_{CC}	T_A = 0°C to +70°C 8 MHz Min	Max	Data Direction
1	TsDI(DAV)	Data-In Setup Time	2.0V	0		IN
			3.9V	0		IN
2	ThDI(DAV)	Data-In Hold Time	2.0V	160		IN
			3.9V	115		IN
3	TwDAV	Data Available Width	2.0V	155		IN
			3.9V	110		IN
4	TdDAVI (RDY)	DAV Falling to RDY	2.0V		160	IN
		Falling Delay	3.9V		115	IN
5	TdDAVId (RDY)	DAV Rising to RDY	2.0V		120	IN
		Falling Delay	3.9V		80	IN
6	TdRDYO (DAV)	RDY Rising to DAV	2.0V	0		IN
		Falling Delay	3.9V	0		IN
7	TdDO (DAV)	Data Out to DAV	2.0V	63		OUT
		Falling Delay	3.9V	63		OUT
8	TdDAV0 (RDY)	DAV Falling to RDY	2.0V	0		OUT
		Falling Delay	3.9V	0		OUT
9	TdRDY0 (DAV)	RDY Falling to DAV	2.0V		160	OUT
		Rising Delay	3.9V		115	OUT
10	TwRDY	RDY Width	2.0V	110		OUT
			3.9V	80		OUT
11	TdRDY0d (DAV)	RDY Rising to DAV	2.0V		110	OUT
		Falling Delay	3.9V		80	OUT

PIN FUNCTIONS

XTAL1

Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2

Crystal 2 (time-based output). This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

Port 0 (P07-P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull in this configuration.

Using single trip point ROM mask option, Port 00-03 can be programmed to allow direct interface to applications that require single point comparison like mouse/trackball IR sensors. ROM mask option will enable the 0.4 V_{DD} Trip Point Buffers on these inputs.

An optional 200 KOhms (port wide) pull-up is available as a mask option on all bits for the L79/L80 versions.

These pull-ups are disabled when configured (bit by bit) as an output.

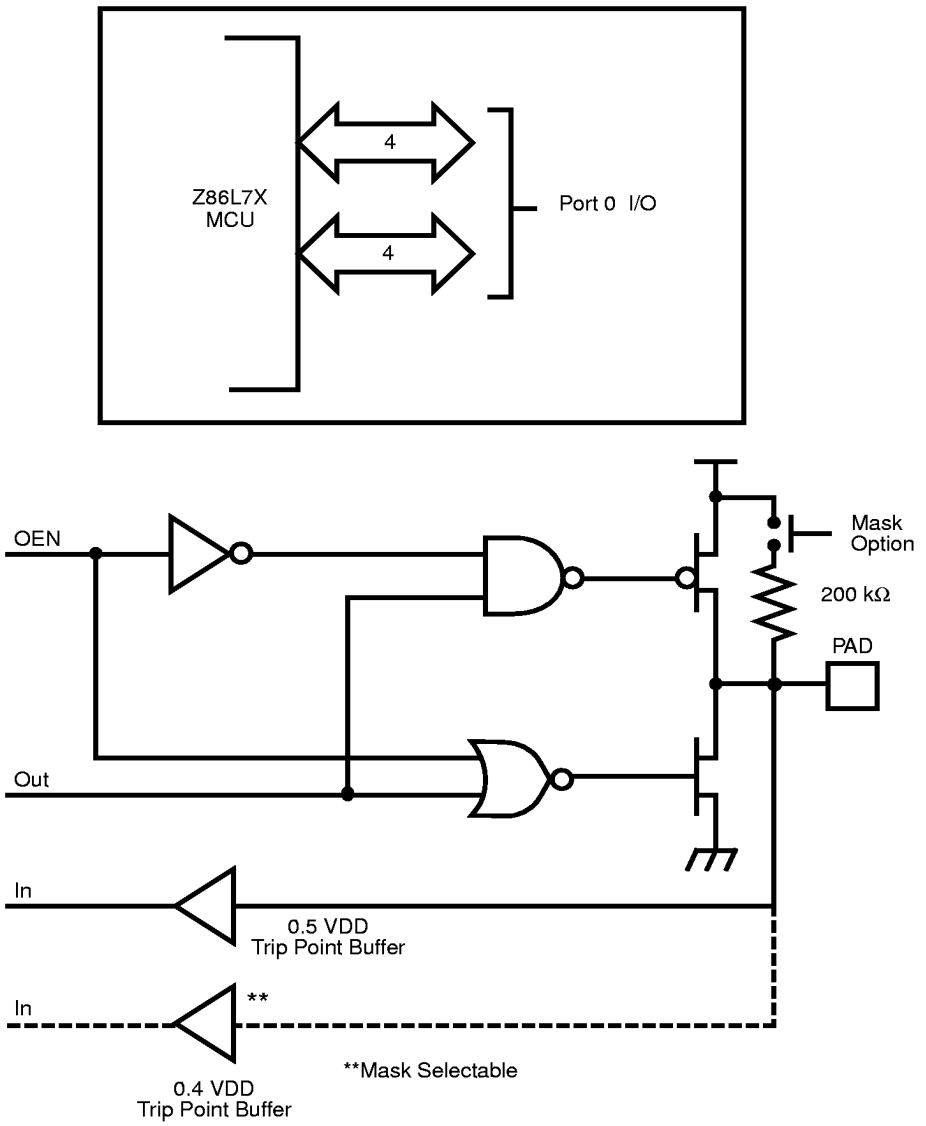


Figure 8. Port 0 Configuration

Port 2 (P27-P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight 200 KOhms (±50%) pull-up resistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. Port 2 may be placed under handshake control. In this configuration, Port 3 lines, P31 and P36 are used as the handshake controls lines $\overline{DAV2}$ and RDY2. The handshake signal assignment for Port 3, lines P31 and P36 is dictated by the direction (input or output) assigned to Bit 7, Port 2 (Figure 9). The Z8 wakes up with the eight bits of Port 2 configured as inputs with open-drain outputs.

Port 2 also has an 8-bit input NOR and a NAND gate which can be used to wake up the part from STOP Mode. P20 can be programmed to access the edge selection circuitry .

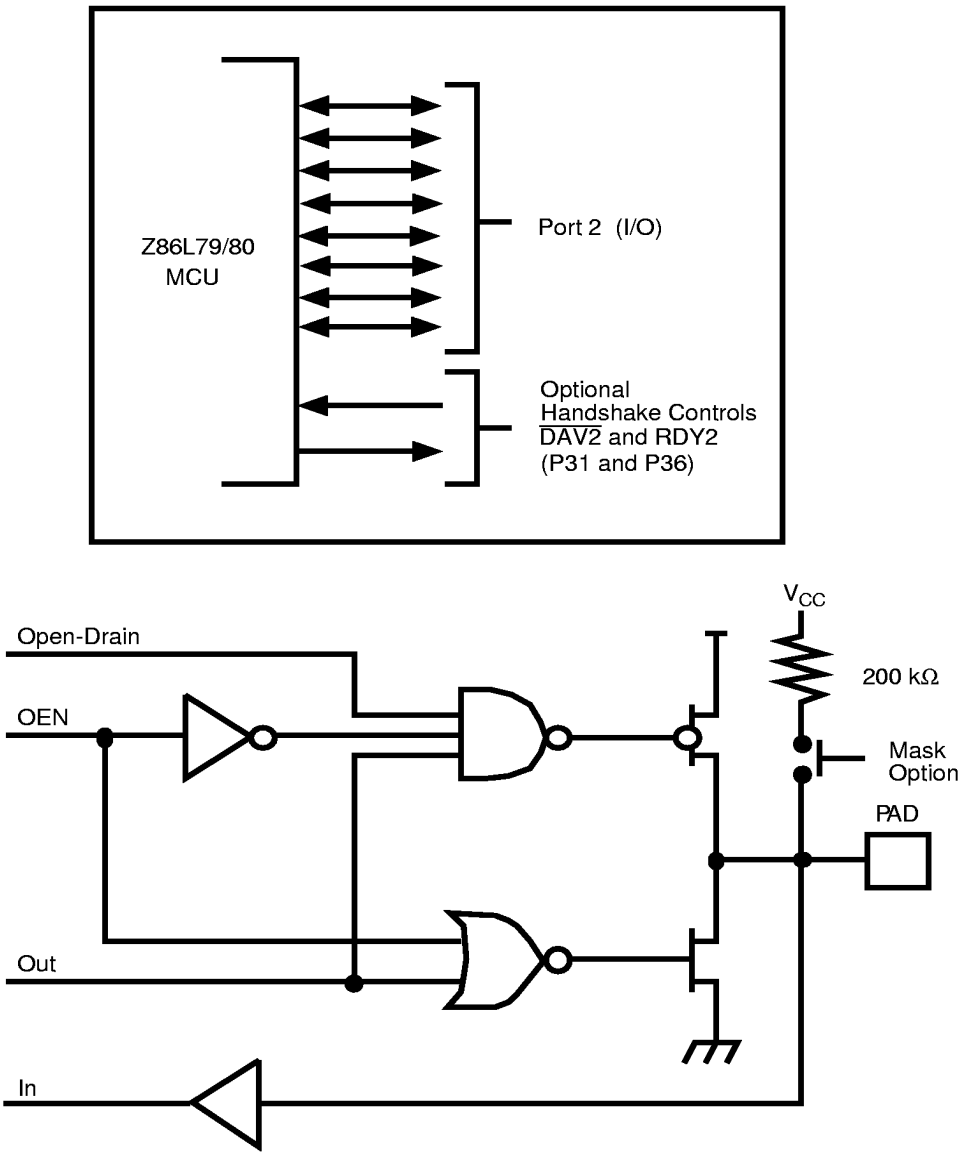


Figure 9. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P31)

Port 3 is a 7-bit, CMOS-compatible three fixed input and four fixed output port. Port 3 consists of three fixed input (P33-P31) and four fixed output (P37-P34), and can be configured under software control for Input/Output, Interrupt, Port handshake, Data Memory functions and output from the counter/timers. P31, P32, and P33 are standard CMOS inputs; outputs are push-pull, except for P34, 35 which are controlled by P3M, D0.

Two on-board comparators process analog signals on P31 and P32 with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the edge detection circuit is through P31 or P20. Handshake lines Ports 0, 1, and 2 are available on P31 through P36.

Port 3 provides the following control functions: handshake for Ports 0 and 2 ($\overline{DAV}$ and RDY); three external interrupt request signals (IRQ2-IRQ0). (See Table 2).

Port 3 also provides output for each of the counter/timers and the AND/OR Logic. Control is performed by programming bits D5-D4 of CTR1, bit 0 of CTR0 and bit 0 of CTR2.

Table 2. Pin Assignments

Pin	I/O	C/T	Comp.	Int.	P0 HS	P2 HS
Pref1	IN		RF1			
P31	IN	ISP	AN1	IRQ2		D/R
P32	IN		AN2	IRQ0	D/R	
P33	IN		RF2	IRQ1		
P34	OUT	T8	A01			
P35	OUT	T16			R/D	
P36	OUT	T8/16				R/D
P37	OUT		A02			

Notes:
1. HS = Handshake Signals
2. D = $\overline{DAV}$
3. R = RDY

Comparator Inputs

Port 3, P31 and P32 all have a comparator front end. The comparator reference voltages are on P33 and Pref1. The internal P33 register and its corresponding IRQ1 is connected to the Stop-Mode Recovery source selected by the SMR. In this mode, any of the Stop-Mode Recovery sources can be used to toggle the P33 bit or generate IRQ1. In digital mode, P33 can be used as a Port 3 register input or IRQ1 for P33 (Figure 11).

Note: The comparators are disabled in STOP Mode.

Comparator Outputs

These may be programmed to be outputted on P34 and P37 through the PCON register (Figure 10).

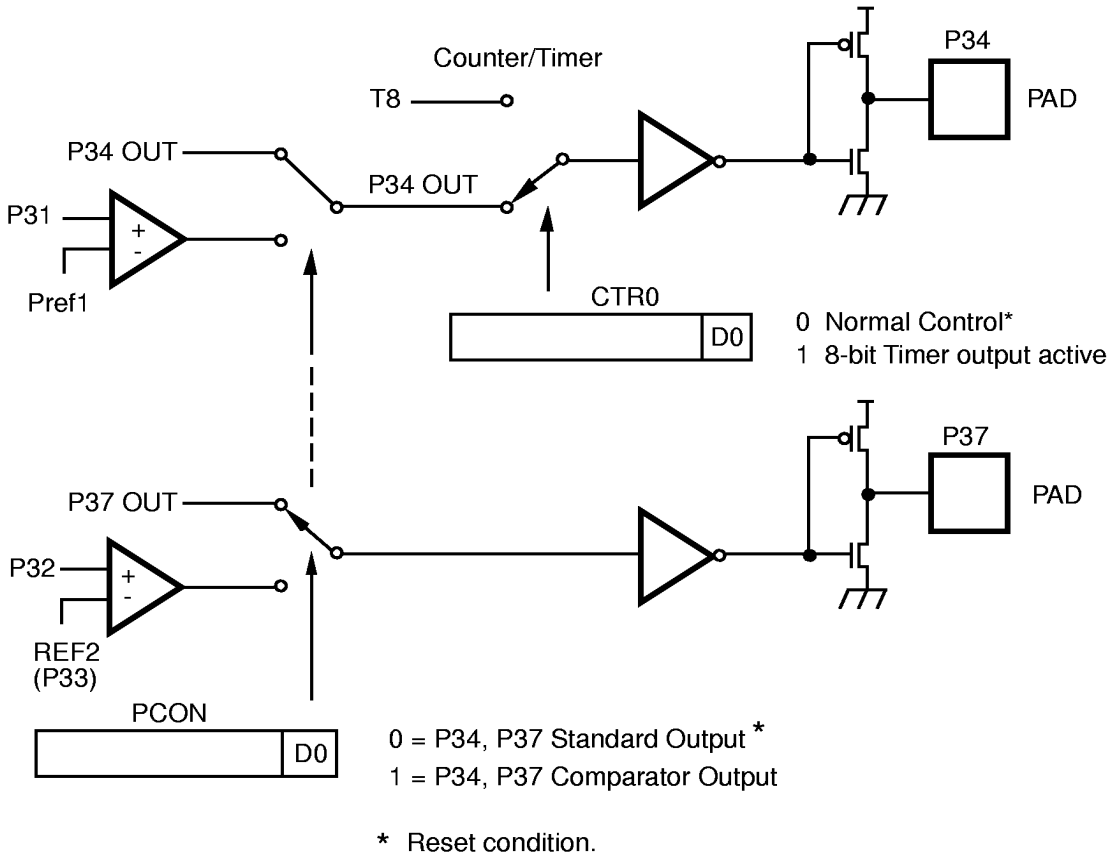


Figure 10. Port 3 Comparator Configuration

Reset

Program execution begins at location 000CH, 5-10 TpC cycles after the RST is released. For Power-On Reset, the typical reset output time is 5 ms. The Z86L79/80 does not reset WDTMR, SMR, P2M, or P3M registers on a Stop-Mode Recovery operation either from WDT or the programmed STOP Mode recovery source.

PIN FUNCTIONS (Continued)

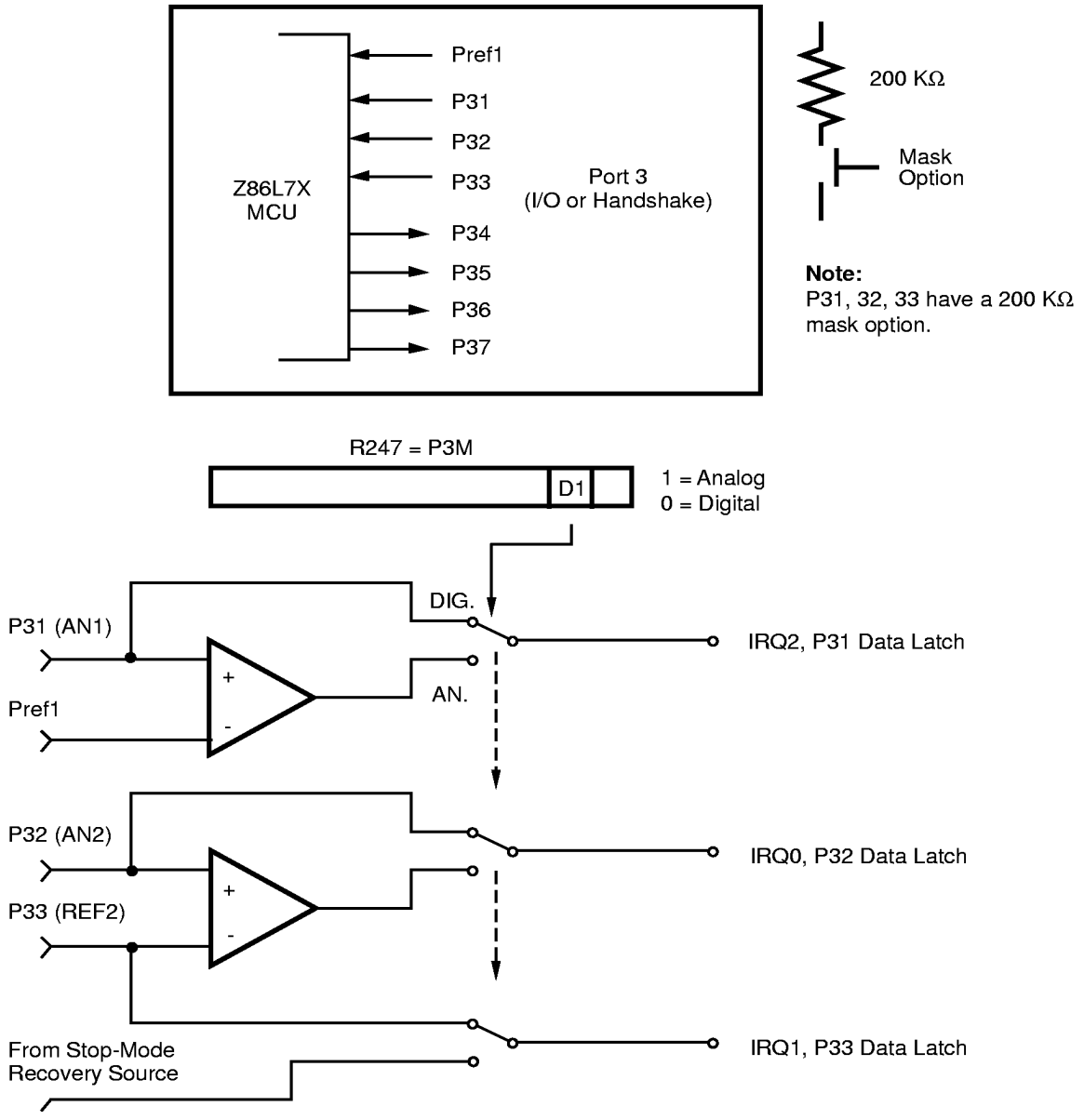
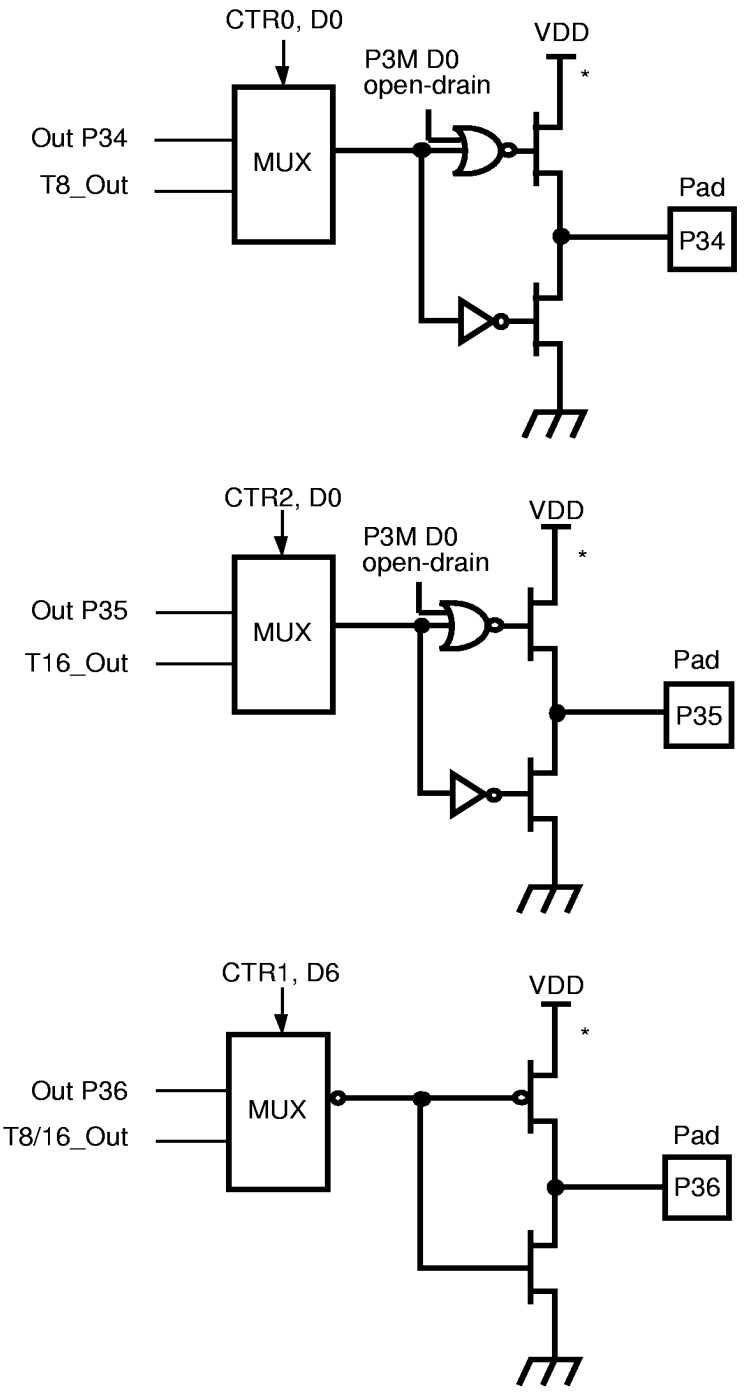


Figure 11. Port 3 Configuration



* Default after reset output is push-pull.

Figure 12. Port 3 Counter Timer Output Configuration

FUNCTIONAL DESCRIPTION

The Z8 incorporates special functions to enhance the Z8's functionality in consumer and battery operated applications.

Reset

The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- Low Voltage Detection

Program Memory

The Z86L79/80 addresses up to 4K and 8 K of internal program memory. (Figure 13). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain five 16-bit vectors that correspond to the five available interrupts. Addresses 12 to 4K, and 8K (dependent on version) consist of on-chip mask-programmed ROM.

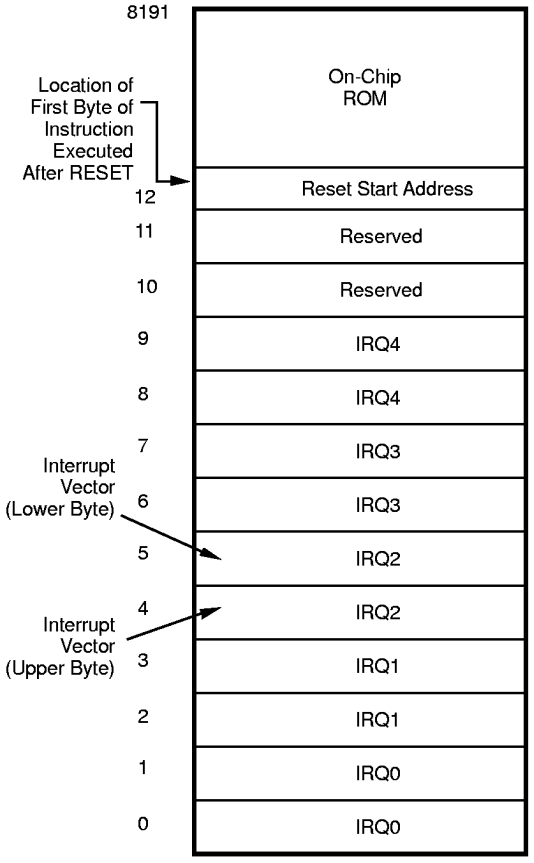


Figure 13. Program Memory Map

External Data Memory

Not accessible using the 28-pin Z86L79/80.

Expanded Register File

The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register group (Figure 14).

The upper nibble of the register pointer (Figure 16) selects a group of 16 bytes in the register file, out of the full 256, to be accessed. The lower nibble selects the expanded register file bank and, in the case of the Z86L79/80 Banks F and D are implemented. A 0H in the lower nibble will allow the normal register file to be addressed, but any other value from 1H to FH will exchange the lower 16 registers in favor of an expanded register group of 16 registers. (See Figure 15.) For example:

R253 RP = 00H
R0 = Port 0
R1 = Port 1
R2 = Port 2
R3 = Port 3

But if:

R253 RP = 0DH
R0 = CTRL0
R1 = CTRL1
R2 = CTRL2
R3 = Reserved

The counter/timers are mapped into ERF group D. Access is easily done using the following example:

LD	RP, #0DH	Select ERF D for access and register Bank 0 as the working register group
LD	R0,#xx	access CTRL0
LD	1, #xx	access CTRL1
LD	RP, #7DH	Select expanded register group (ERF) Bank D for access and register Group 7 as the working register Group.
LD	R1, 2	CTRL2 → register 71H

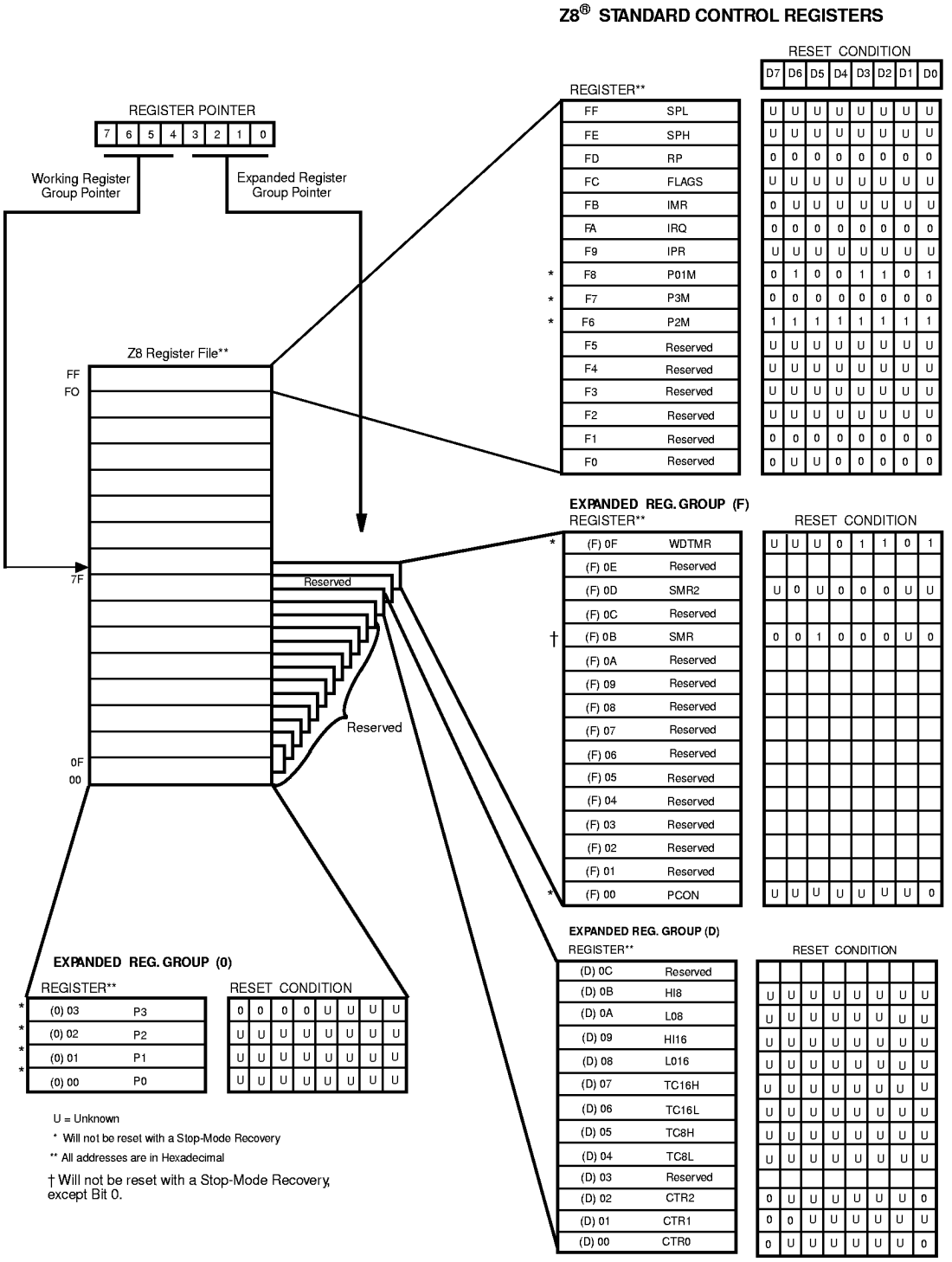


Figure 14. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

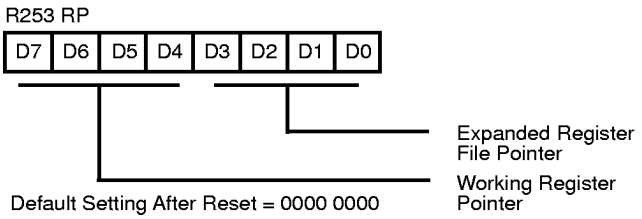


Figure 15. Register Pointer Register

Register File

The register file consists of four I/O port registers, 236 general-purpose registers with 10 control and status registers (R3-R0, R239-R4, and R255-R246, respectively), plus two Expanded Register Groups (D and F) which reside in the expanded register group. Instructions can access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 14). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Register Bank E0-EF is only accessed through working registers and indirect addressing modes. R240-R245 registers are reserved.

Stack

The Z86L79/80 external data memory or the internal register file is used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the general-purpose registers (R4-R239). SPH is used as a general-purpose register only when using internal stacks. When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH will be loaded into Port 0 whenever the internal stack is accessed

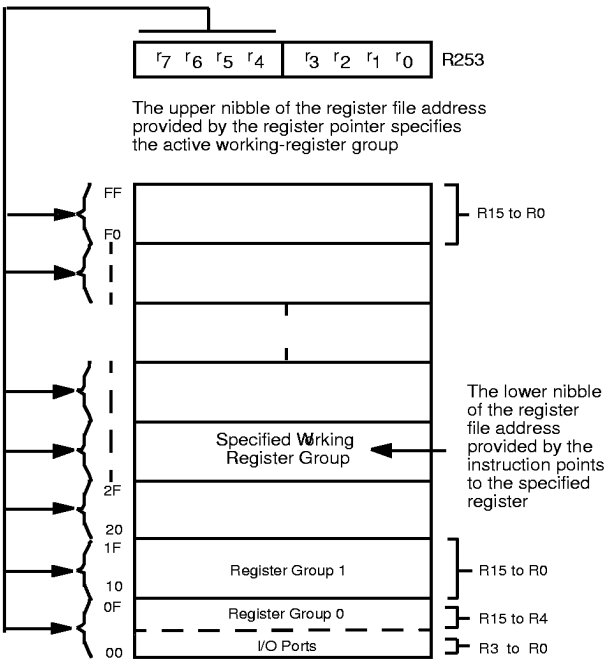


Figure 16. Register Pointer

Counter/Timer Register Description

Expanded Register Group D	
(D)%0C	Reserved
(D)%0B	HI8
(D)%0A	LO8
(D)%09	HI16
(D)%08	LO16
(D)%07	TC16H
(D)%06	TC16L
(D)%05	TC8H
(D)%04	TC8L
(D)%03	Reserved
(D)%02	CTR2
(D)%01	CTR1
(D)%00	CTR0

HI8(D)%0B
Holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	76543210	R W	Captured Data No Effect

L08(D)%0A
Holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	76543210	R W	Captured Data No Effect

HI16(D)%09
Holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	76543210	R W	Captured Data No Effect

L016(D)%08
Holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	76543210	R W	Captured Data No Effect

TC16H(D)%07
Counter/Timer2 MS-Byte Hold Register.

Field	Bit Position		Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)%06
Counter/Timer2 LS-Byte Hold Register.

Field	Bit Position		Description
T16_Data_LO	76543210	R/W	Data

TC8H(D)%05
Counter/Timer8 High Hold Register.

Field	Bit Position		Description
T8_Level_HI	76543210	R/W	Data

TC8L(D)%04
Counter/Timer8 Low Hold Register.

Field	Bit Position		Description
T8_Level_LO	76543210	R/W	Data

FUNCTIONAL DESCRIPTION (Continued)

Table 3. CTR0 (D)%00: Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R	0*	**Table 4. Counter Disabled**
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-------	R/W	0*	Modulo-N
			1	Single Pass
Time_OUT	--5------	R	0	No Counter Time_OUT
			1	Counter Time_OUT Occurred
			0	No Effect
			1	Reset Flag to 0
T8 _Clock	---43---	R/W	0 0*	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_MASK	-----2--	R/W	0	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt
Counter_INT_Mask	------1-	R/W	0	Disable Time_OUT Interrupt
			1	Enable Time_OUT Interrupt
P34_O	-------0	R/W	0	P34 as Port Output
			1	T8 Output on P34

Notes:
* Indicates the value after Power-On Reset.

CTR0: Counter/Timer8 Control Register Description

T8 Enable
This field enables T8 when set (written) to 1.

Single/Modulo-N
When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single pass), the counter stops when the terminal count is reached.

Time_OUT
This bit is set when T8 times out (terminal count reached). To reset this bit, a 1 should be written to this location.

Note: This is the only way to reset this status condition, therefore, care should be taken to reset this bit prior to using/enabling the counter/timers.

Care must be taken when utilizing the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers will be evaluated using the OR or AND logical operators and the specified value, then written back into the registers. Example: When the status of bit 5 is 1, a reset condition will occur.

T8 Clock
Defines the frequency of the input signal to T8.

Capture_INT_Mask
Set this bit to allow interrupt when data is captured into either LO8 or HI8 when a positive or negative edge detection occurs in demodulation mode.

Counter_INT_Mask
Set this bit to allow interrupt when T8 has a timeout.

P34_OUT
This bit defines whether P34 is used as a normal output pin or the T8 output.

Table 5. CTR1(D)%01: Controls the Functions in Common with the T8 and T16

Field	Bit Position		Value	Description
Mode	7-------	R/W	0	Transmit Mode
			1	Demodulation Mode
P36_OUT/	-6------	R/W		Transmit Mode
Demodulator_Input			0	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/	--54----	R/W		Transmit Mode
Edge _Detect			00	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved
Transmit_Submode/	----32--	R/W		Transmit Mode
Glitch_Filter			00	Normal Operation
			01	Ping-Pong Mode
			10	T16_OUT =0
			11	T16_OUT = 1
				Demodulation Mode
			00	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	16 SCLK Cycle
Initial_T8_OUT/	------1-			Transmit Mode
Rising_Edge		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_OUT/	-------0			Transmit Mode
Falling _Edge		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		R	0	No Effect
			1	Reset Flag to 0

CTR1 Register Description

Mode
If it is 0, the Counter/Timers are in the transmit mode, otherwise they are in the demodulation mode.

P36_OUT/Demodulator_Input
In Transmit Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In Demodulation Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

T8/T16_Logic/Edge _Detect
In Transmit Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In Demodulation Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter
In Transmit Mode, this field defines whether T8 and T16 are in the Ping-Pong mode or in independent normal operation mode. Setting this field to Normal Operation Mode terminates the Ping-Pong Mode operation. When set to 10, T16_OUT is immediately set to A0. When set to 11, T16 is immediately forced to a 1.

In Demodulation Mode, this field defines the width of the glitch that should be filtered out.

Initial_T8_OUT/Rising_Edge
In Transmit Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. Note: When (CTR1, D1, D0) Bits are loaded, T8_OUT and T16_OUT will switch to the opposite state. This ensures a transition to the initial value when the counters are enabled. Therefore, it is not advisable to change (CTR1, D1, D0) Bits while the counters are running.

In Demodulation Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Initial_T16 OUT/Falling _Edge
In Transmit Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or Ping-Pong Mode (CTR1, D3, D2).

In Demodulation Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Table 6. CTR2 (D)%02: Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7----- --	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6------	R/W		Transmit Mode
			0	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_OUT	--5-----	R	0	No Counter Timeout
				Counter Timeout Occurred
				No Effect
				Reset Flag to 0
T16 _Clock	---43---	R/W	00	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	-----2--	R/W	0	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt
Counter_INT_Mask	------1-	R/W	0	Disable Time_OUT Interrupt
			1	Enable Time_OUT Interrupt
P35_OUT	-------0	R/W	0	P35 as Port Output
			1	T16 Output on P35

Note: *Indicates the value after Power-On Reset.

CTR2 Description

T16_Enable
This field enables T16 when set to 1.

Single/Modulo-N
In Transmit Mode, when set to 0, the counter reloads the initial value when terminal count is reached. When set to 1, the counter stops when the terminal count is reached.

In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges; when set to 1, T16 captures and detects on the first edge, but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode.

Time_OUT
This bit is set when T16 times out (terminal count reached). In order to reset it, a 1 should be written to this location.

T16_Clock
Defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask
Set this bit to allow interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask
Set this bit to allow interrupt when T16 times out.

P35_OUT
This bit defines whether P35 is used as a normal output pin or T16 output.

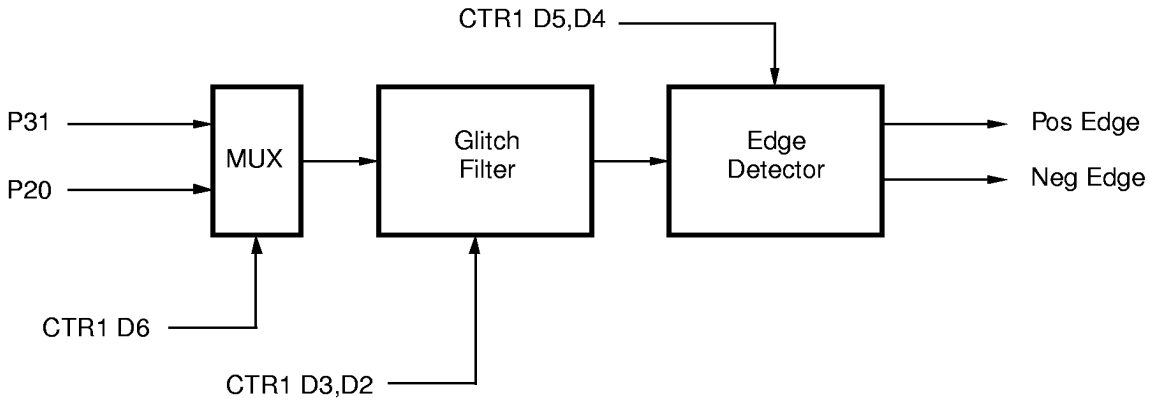


Figure 17. Glitch Filter Circuitry

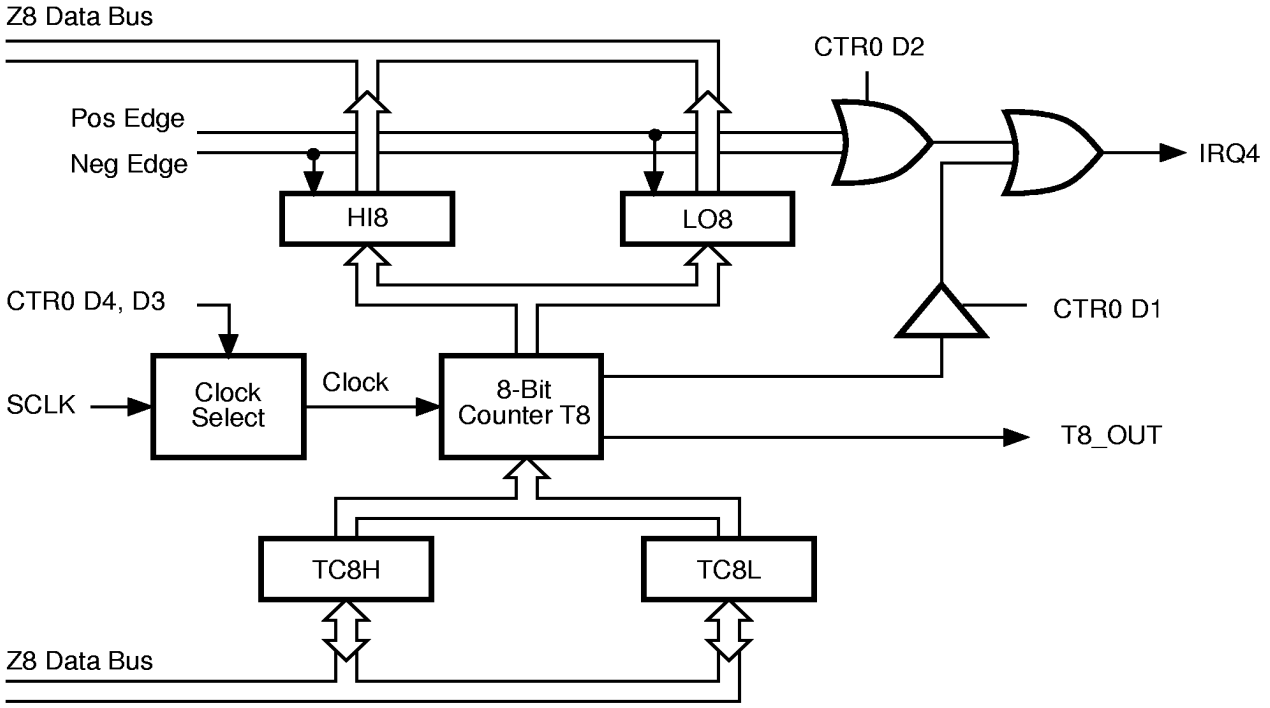


Figure 18. 8-Bit Counter/Timer Circuits

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5-D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal which have a width less than specified (CTR1 D3, D2) are filtered out.

T8 Transmit Mode

When T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1. If it is 1, T8_OUT is 0.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1 D1). If the initial value (CTR1 D1) is 0, TC8L is loaded, otherwise TC8H is loaded into the counter. In Single-Pass Mode (CTR0 D6), T8 counts down

to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0 D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0 D1). In Modulo-N Mode, after reaching terminal count, T8_OUT is toggled, but no interrupt is generated. Then T8 loads a new count. If the T8_OUT level now is 0, TC8L is loaded; if the T8_OUT level is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, sets the time-out status bit (CTR0 D5) and generates an interrupt if enabled (CTR0 D1). This completes one cycle. T8 then loads from TC8H or TC8L according to the T8_OUT level, and repeats the cycle. (Refer to Figures 19-21).

The user can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded. Care must be taken not to write these registers at the time the values are to be loaded into the counter/timer, to ensure known operation. An initial count of 1 is not allowed (a non-function will occur). An initial count of 0 will cause TC8 to count from 0 to %FF to %FE (Note, % is used for hexadecimal values). Transition from 0 to %FF is not a time-out condition.

Note: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands, first stopping the counter/timers, then resetting the status bits is necessary. This is required because it takes one counter/timer clock interval for the initiated event to actually occur.

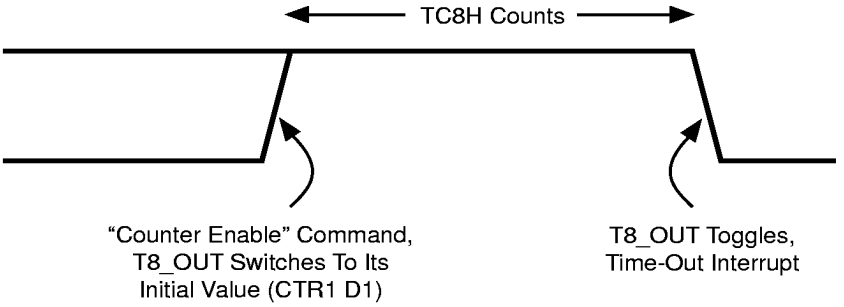


Figure 19. T8_OUT in Single-Pass Mode

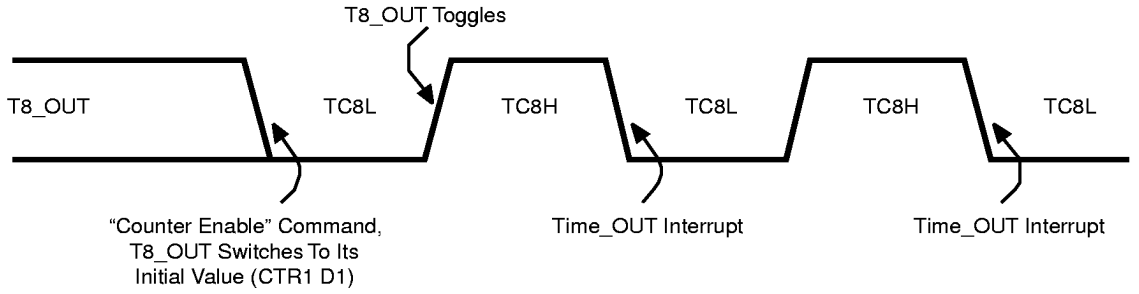


Figure 20. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user should program TC8L and TC8H to %FF. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8, if negative edge, HI8. One of the edge detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with %FF and starts counting again. Should T8 reach 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from %FF (Figures 22 and 23).

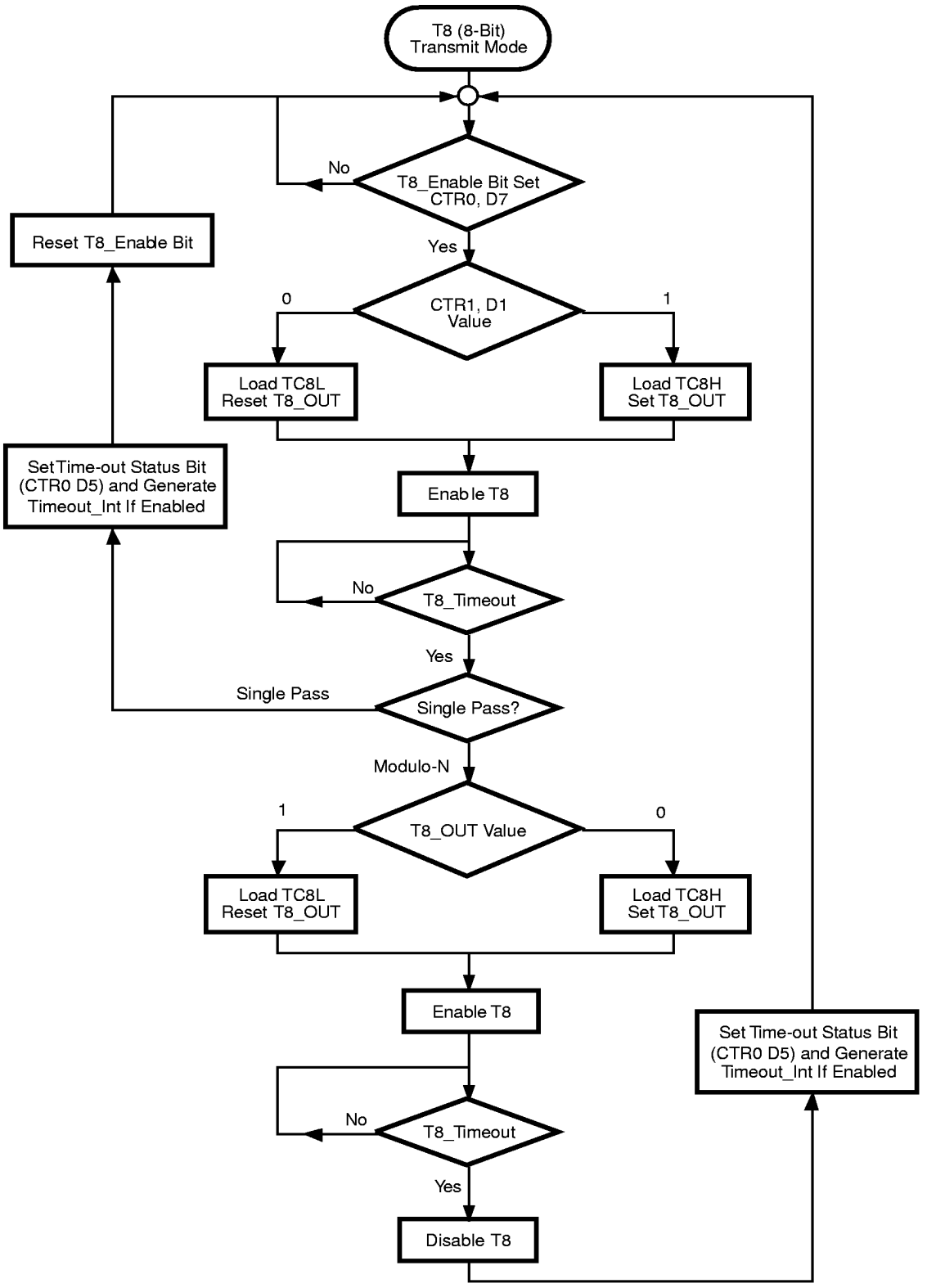


Figure 21. Transmit Mode Flowchart

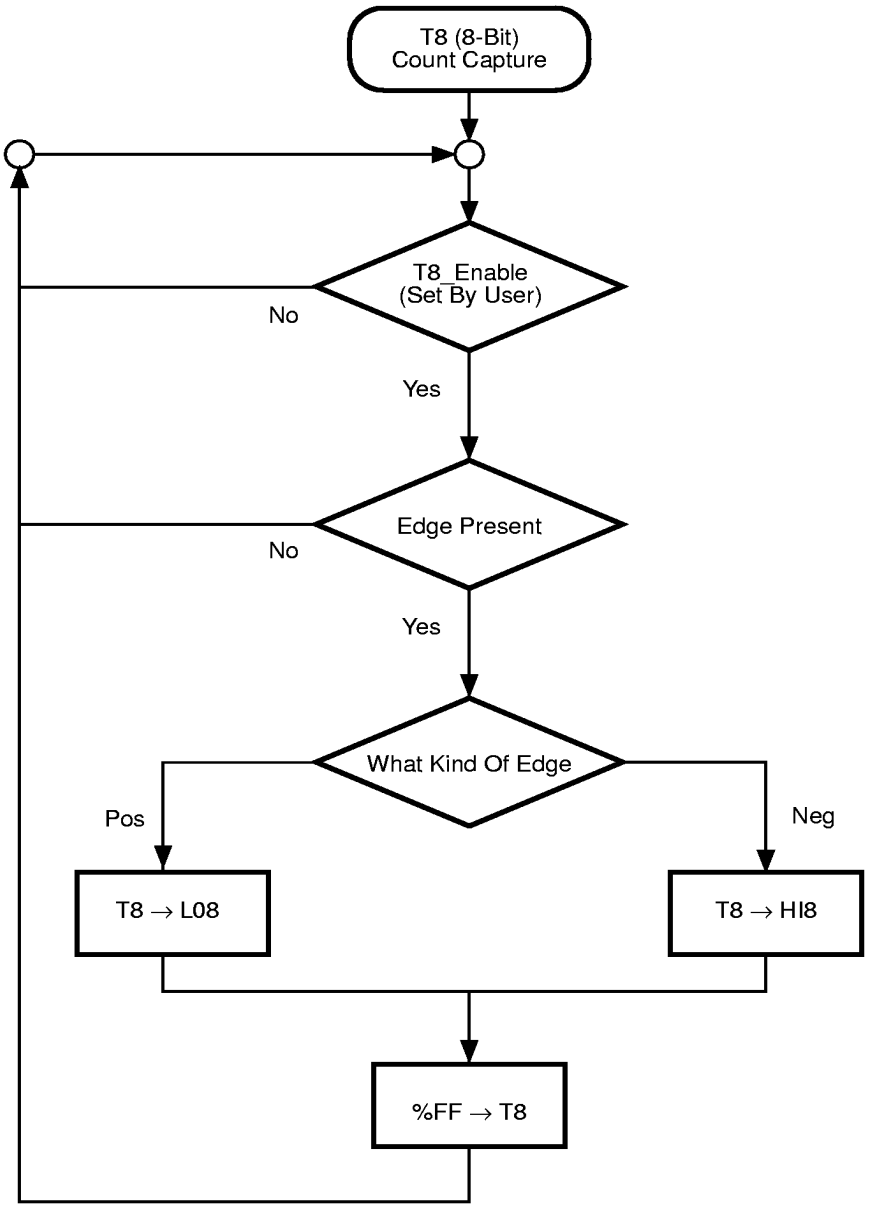


Figure 22. Demodulation Mode Count Capture Flowchart

FUNCTIONAL DESCRIPTION (Continued)

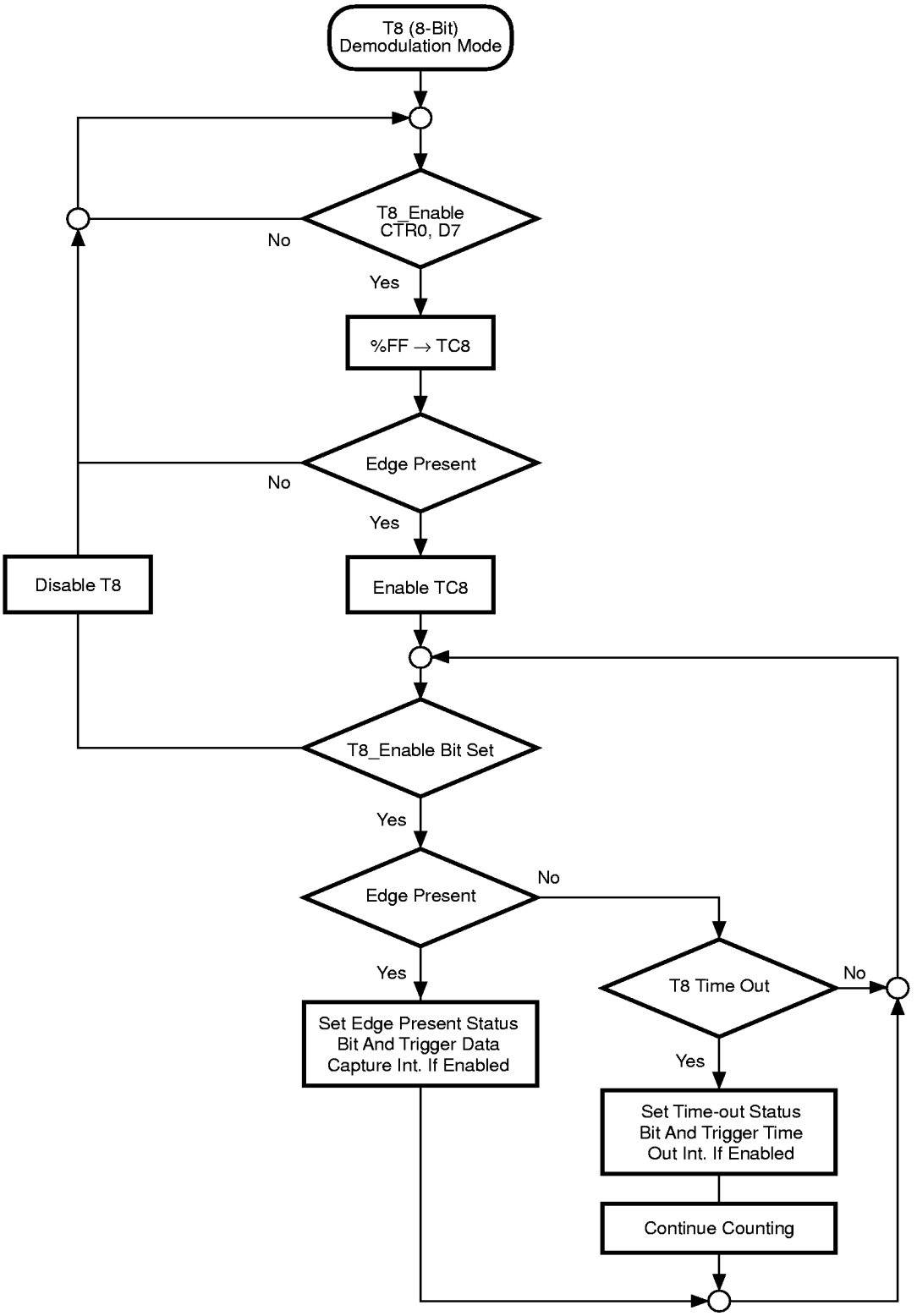


Figure 23. Demodulation Mode Flowchart

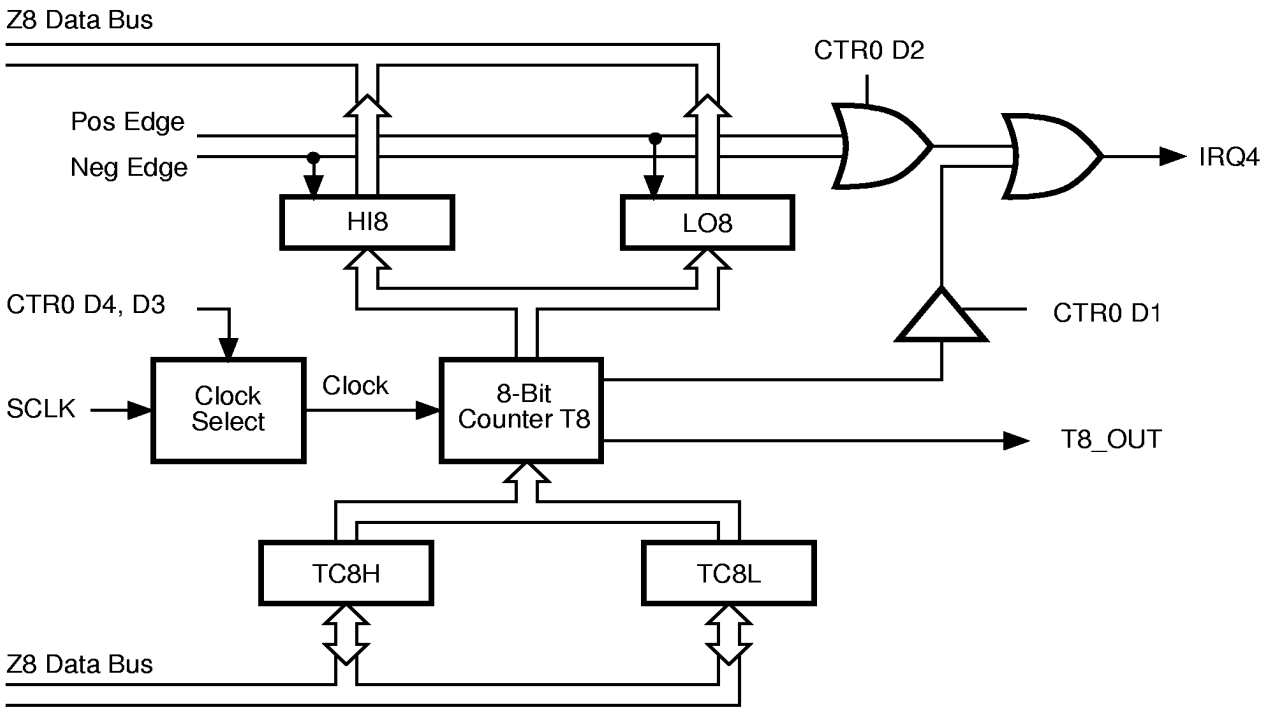


Figure 24. 16-Bit Counter/Timer Circuits

T16 Transmit Mode

In Normal or Ping-Pong Mode, the output of T16 when not enabled is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. The user can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3, D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1 D0). When T16 counts down to 0, T16_OUT is toggled (in Normal or Ping-Pong Mode), an interrupt is generated if enabled (CTR2 D1), and a status bit (CTR2 D5) is set.

Note: that global interrupts will override this function as described in the interrupts section. If T16 is in Single-Pass Mode, it is stopped at this point. If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L and the counting continues.

The user can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded. Care must be taken not to load these registers at the time the counter/timer value is set, to ensure known operation. The initial value of the counter should not be 1, but should instead be 0. As T16 counts down, its value changes from 0 to %FFFF, then continues to decrement to %FFFE, and so forth, down to an ending value of 1. Transition from 0 to %FFFF is not a time-out condition.

FUNCTIONAL DESCRIPTION (Continued)

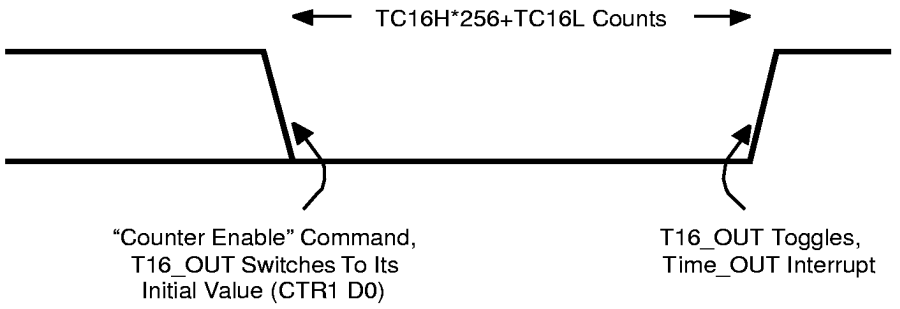


Figure 25. T16_OUT in Single-Pass Mode

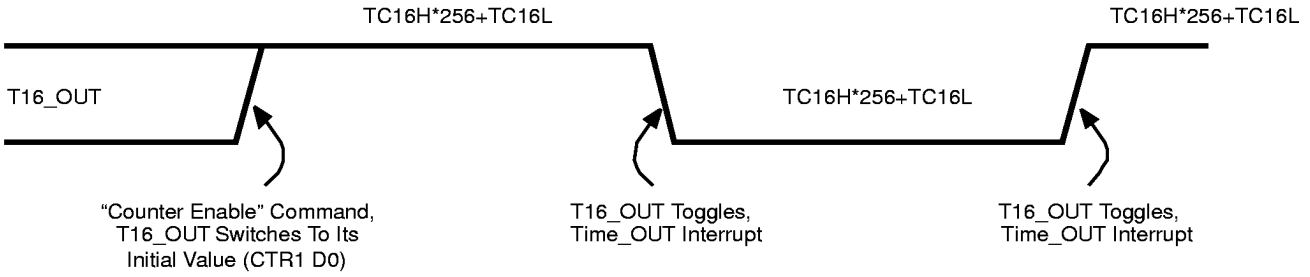


Figure 26. T16_OUT in Modulo-N Mode

T16 Demodulation Mode

The user should program TC16L and TC16H to %FF. After T16 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, begins to count down.

If D6 of CTR2 is 0
When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current count in T16 is one's complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1 D1, D0) is set and an interrupt is generated if enabled (CTR2 D2). T16 is loaded with %FFFF and starts again.

If D6 of CTR2 is 1
T16 ignores the subsequent edges in the input signal and continues counting down. A time out of T8 will cause T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 will capture and reload on the next edge (rising, falling, or both depending on CTR1 D5, D4) but continue to ignore subsequent edges.

Should T16 reach 0, it continues counting from %FFFF; meanwhile, a status bit (CTR2 D5) is set and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in Transmit Mode. T8 and T16 must be programmed in Single-Pass Mode (CTR0 D6, CTR2 D6) and Ping-Pong Mode must be programmed in CTR1 D3, D2. The user can begin the operation by enabling either T8 or T16 (CTR0 D7 or CTR2 D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1 D1). Then, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled and T16 is enabled. T16_OUT switches to its initial value (CTR1 D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count it stops, T8 is enabled again, and the whole cycle repeats. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0 D1, CTR2 D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1.

Note: Enabling Ping-Pong operation while the counter/timers are running may cause intermittent counter/timer function.

Disable the counter/timers, then reset the status flags prior to instituting this operation.

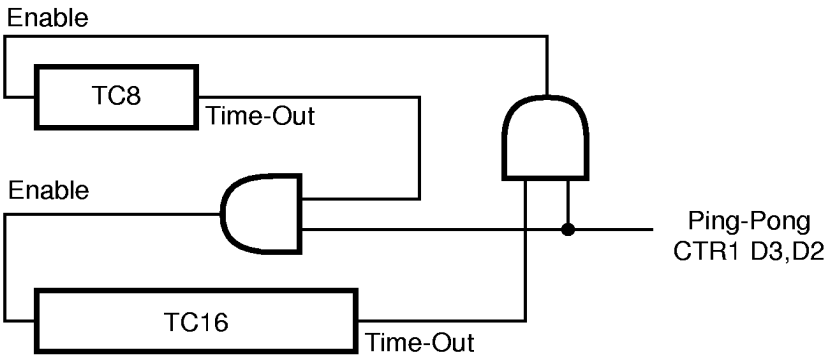


Figure 27. Ping-Pong Mode

To Initiate Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) will be cleared by hardware. The time-out bits (CTR0 D5, CTR2 D5) will be set every time the counter/timers reach the terminal count.

FUNCTIONAL DESCRIPTION (Continued)

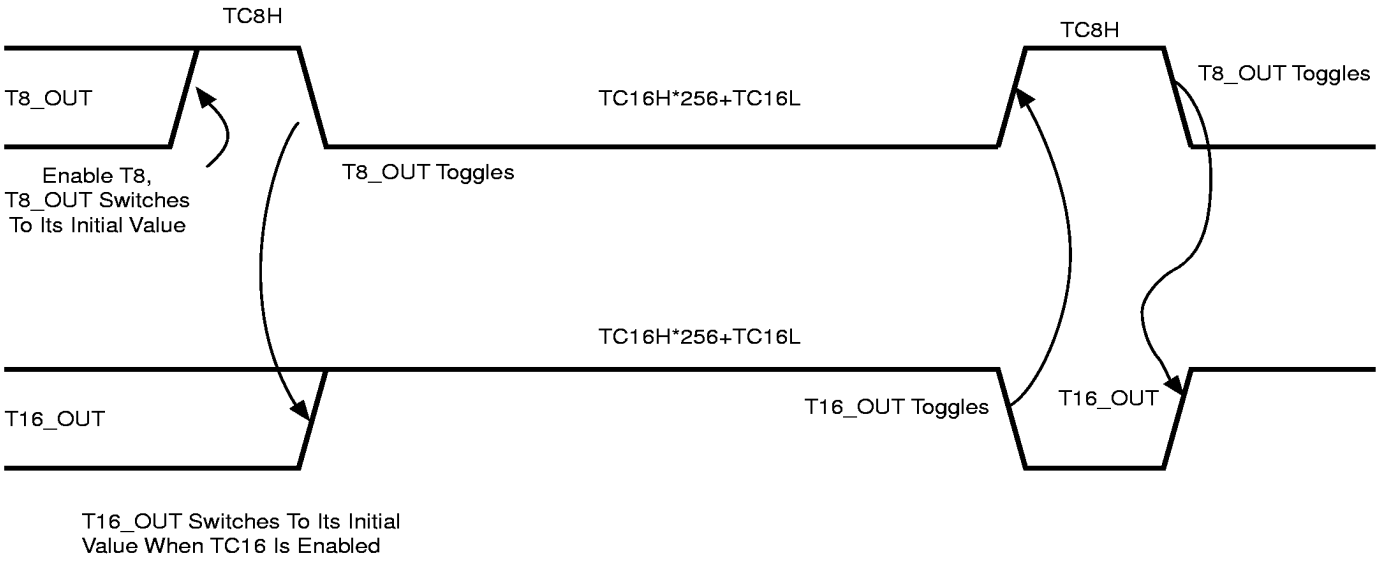


Figure 28. T8_OUT and T16_OUT in Ping-Pong Mode

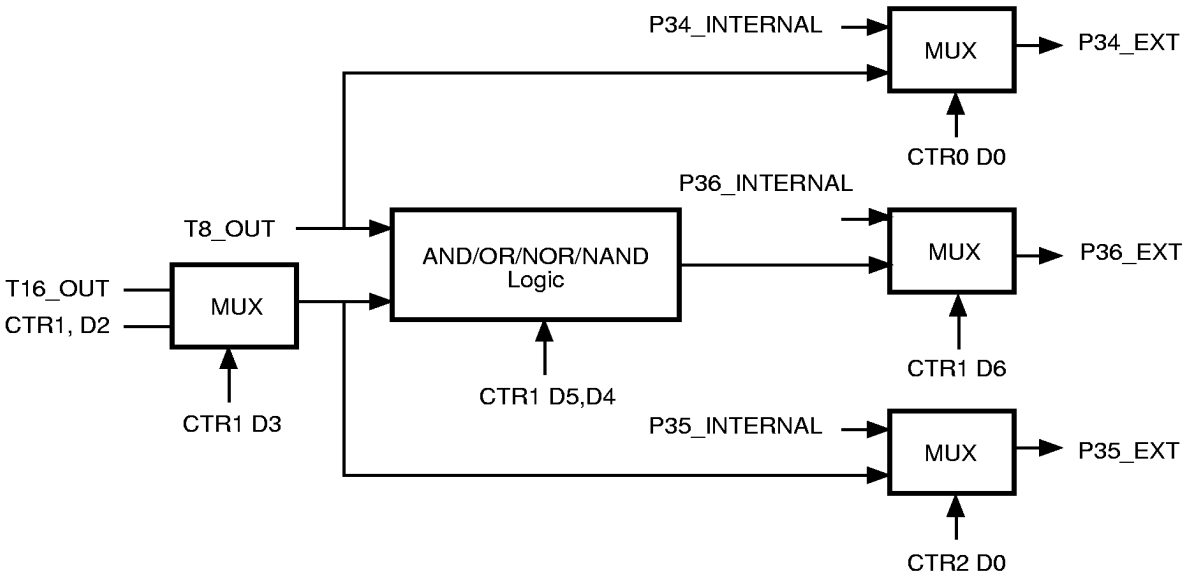


Figure 29. Output Circuit

Interrupts

The Z86L79/80 has five different interrupts. The interrupts can be masked and prioritized (Figure 30). The five sources are divided as follows: three sources are claimed by Port 3 lines P33-P31, the remaining two by the counter/timers (Table 8). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.

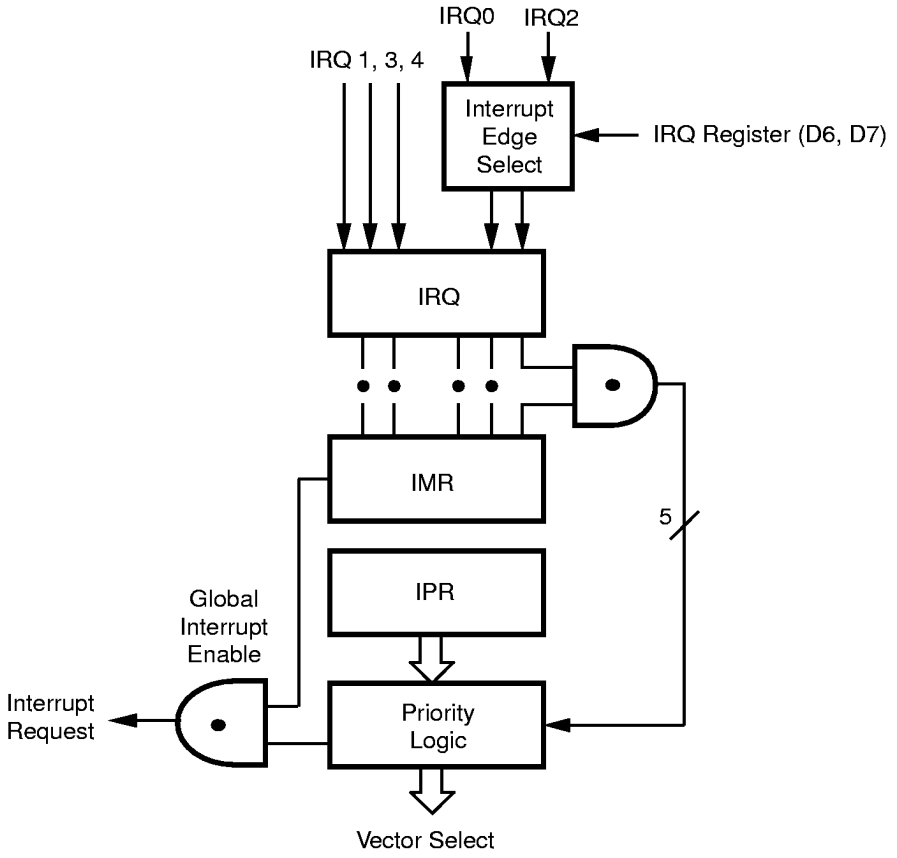


Figure 30. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Table 7. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rising Falling Edge Triggered
IRQ3	T16	6, 7	Internal
IRQ4	T8	8, 9	Internal
IRQ5		10,11	Reserved

Table 8. IRQ Register

IRQ		Interrupt Edge	
D7	D6	IRQ2	IRQ0
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge
In analog mode, the Stop-Mode Recovery sources selected by the SMR register are connected to IRQ1 input. Any of the Stop-Mode Recovery sources for SMR (except P31, P32, and P33) can be used to generate IRQ1 (falling edge triggered).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86L79/80 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 9.

Clock

The Z86L79/80 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The Z86L79/80 on-chip oscillator may be driven with a cost-effective RC network or other suitable external clock source.

The crystal should be connected across XTAL1 and XTAL2 using the suppliers recommended capacitors from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 31).

Power-On Reset

A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power Fail to Power OK status including waking up from Low Voltage standby mode.
2. Stop-Mode Recovery (if D5 of SMR = 1).
3. WDT Timeout.

The POR time is a nominal 5 ms. Bit 7 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery, as is typical for external clock, RC, and LC oscillators.

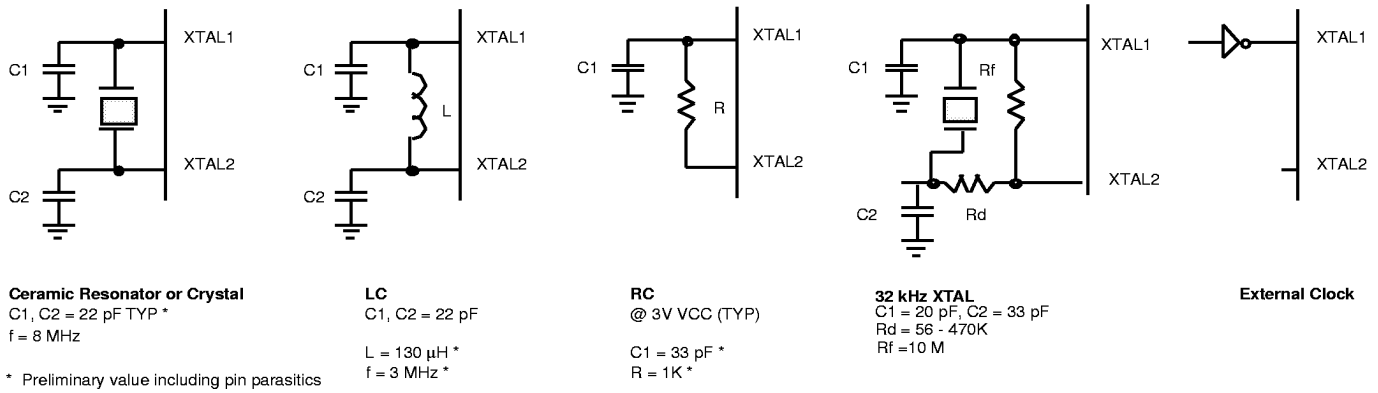


Figure 31. Oscillator Configuration

HALT

HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, and IRQ4 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA (typical) or less. STOP Mode is terminated only by a reset, such as WDT time-out, POR, SMR, or external reset. This causes the processor to restart the application program at address 000CH. In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, as in the following example:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
        or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

Notes:

1. A WDT timeout during STOP Mode will have the same effect like a recovery from any programmed STOP Mode recovery source except the reset delay of TPOR will occur.
2. The comparators are disabled in STOP Mode.

PORT CONFIGURATION REGISTER

The Port Configuration Register (PCON) register configures the comparator output on Port 3. It is located in the expanded register file at Bank F, location 00 (Figure 32).

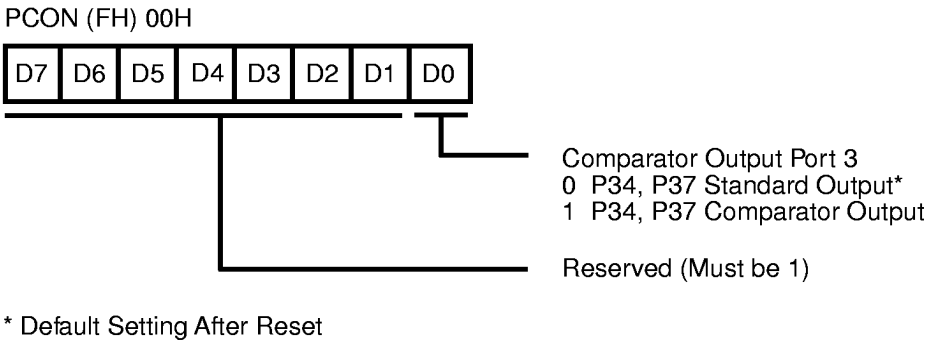


Figure 32. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0)
Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

STOP-MODE RECOVERY REGISTER (SMR)

This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the output of the recovery-source logic. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, the SMR register, specify the source of the Stop-Mode Recovery signal. Bit 0 determines the frequency of SCLK/TCLK in relation to the OSC. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

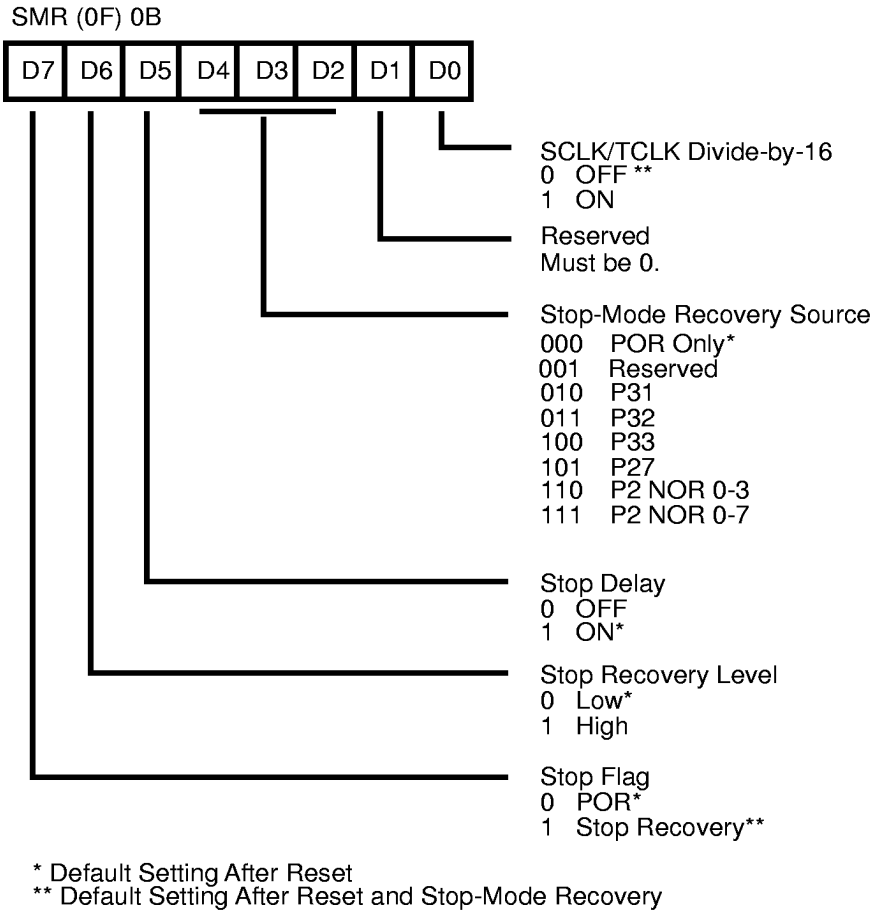


Figure 33. Stop-Mode Recovery Register

Table 9. SMR2(F)%0D: Stop-Mode Recovery Register 2

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0*	Low
			1	High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000*	A. POR Only
			001	B. NAND of P23-P20
			010	C. NAND or P27-P20
			011	D. NOR of P33-P31
			100	E. NAND of P33-P31
			101	F. NOR of P33-P31, P00,P07
			110	G. NAND of P33-P31,P00,P07
			111	H. NAND of P33-P31,P22-P20
Reserved	------10		00	Reserved (Must be 0)

Note: *Indicates the value after Power-On Reset.

Port pins configured as outputs are ignored as an SMR2 recover source for NAND only. For example, if NAND of P23-P20 is selected as the recover source and P20 is configured as output, then P20 is ignored as a recover source. The effective recover source in this case is NAND of P23-P21.

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a Divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution SCLK control) and/or HALT Mode (where TCLK sources interrupt logic). After Stop-Mode Recovery, this bit is set to a 0.

Note: When changing the system clock to or from divide-by-16, you must follow the instruction with two NOPs in order to avoid clock conflicts during the internal system clock frequency change.

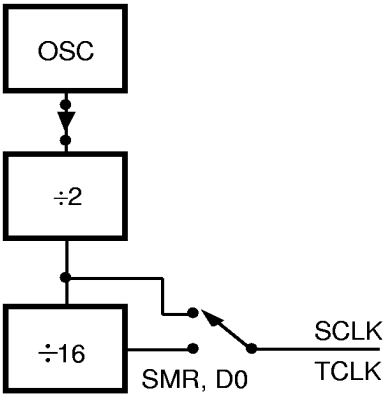


Figure 34. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake up source of the STOP recovery (Figure 35 and Table 10).

Table 10. Stop-Mode Recovery Source

SMR: 432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Stop-Mode Recovery Delay Select (D5)

This bit, if High, disables the 5 ms $\overline{\text{RESET}}$ delay after Stop-Mode Recovery. The default configuration of this bit is one. If the fast wake up is selected, the Stop-Mode Recovery source needs to be kept active for at least 5TpC.

Stop-Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery source logic outputs wakes the Z86L79/80 from STOP Mode. A 0 indicates Low level recovery. The default is 0 on POR (Figure 33).

Cold or Warm Start (D7)

This bit is set by the device when entering STOP Mode. A 0 in this bit (cold) indicates that the device will be reset by POR/WDT Reset. A 1 in this bit (warm) indicates that the device awakens by a SMR source. This is a READ only bit.

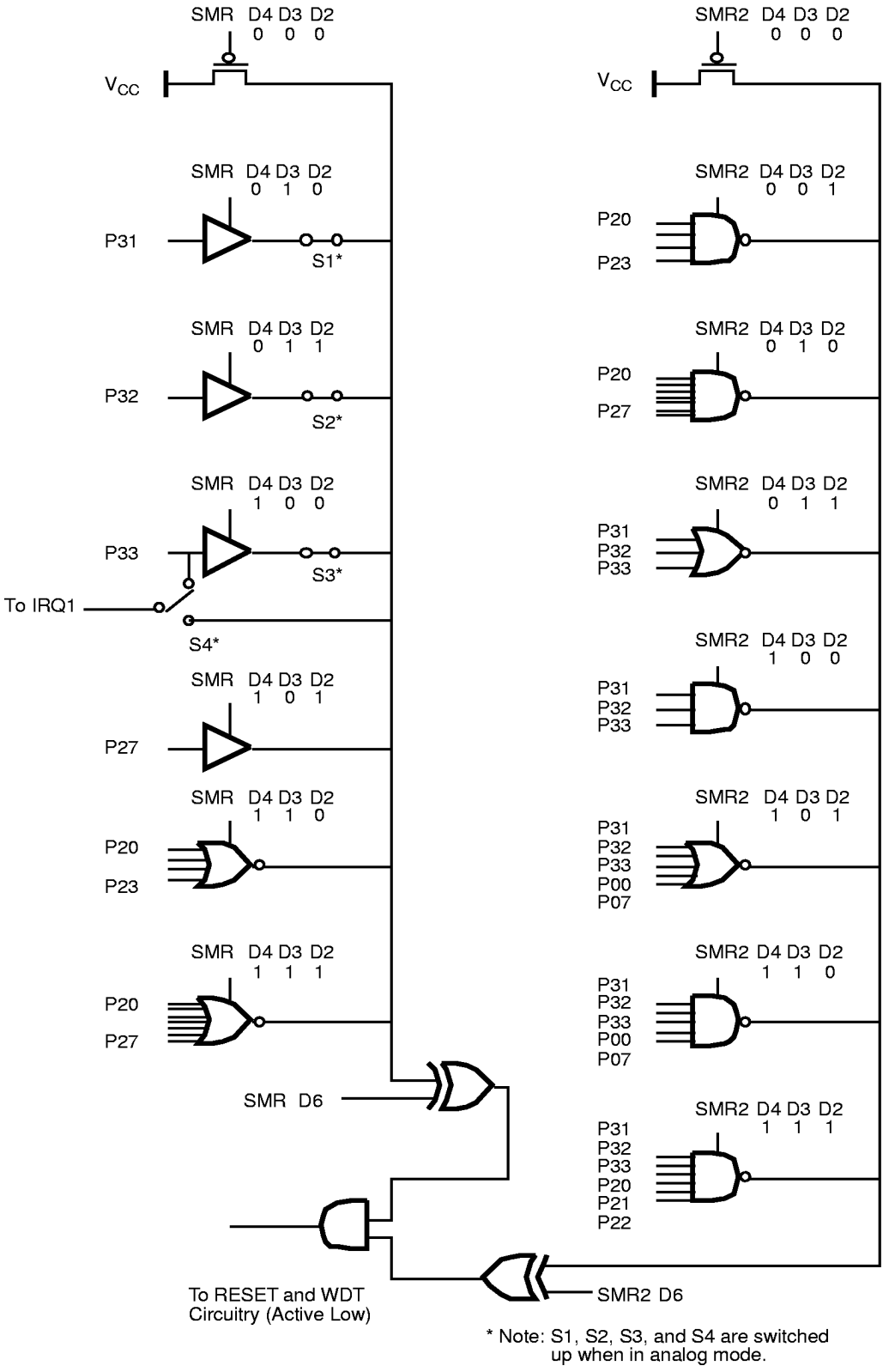


Figure 35. Stop-Mode Recovery Source

WATCH-DOG TIMER MODE REGISTER

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bit 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved (Figure 36). This register is accessible only within the first 60 processor cycles (60 internal system clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 37). After this point, the register cannot be modified by any means, intentional or otherwise. The Watch-Dog Timer Mode Register (WDTMR) cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH. It is organized as follows:

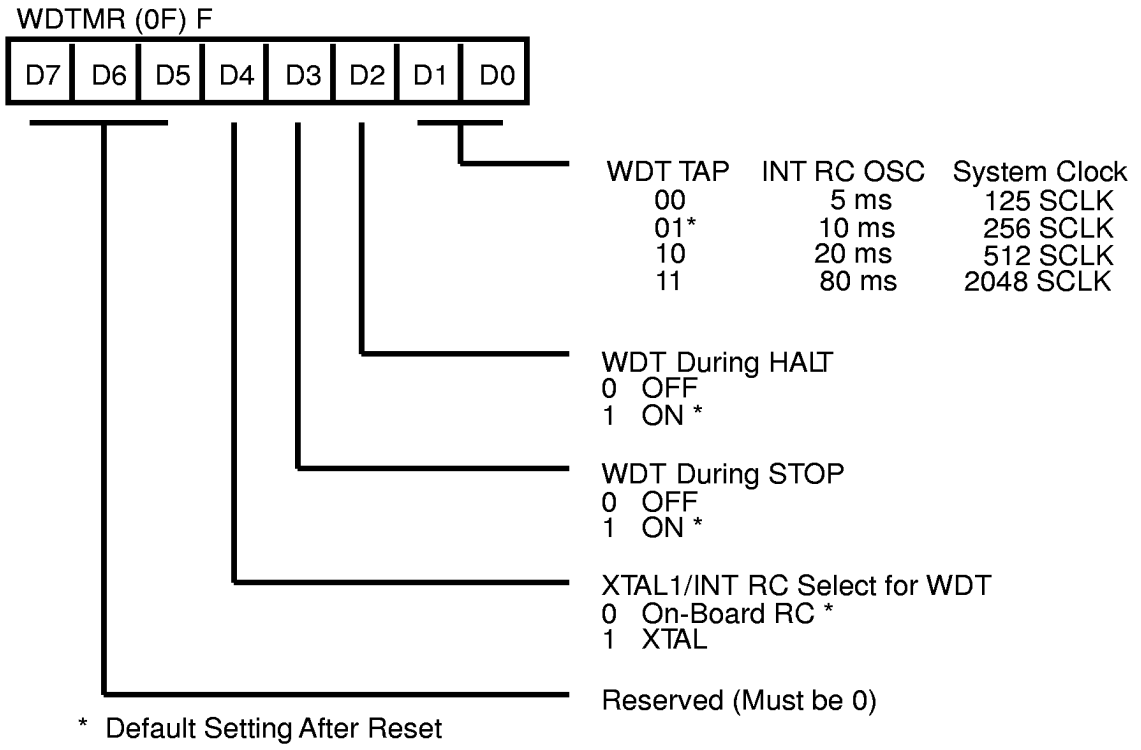


Figure 36. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

Selects the WDT time period. It is configured as shown in Table 11.

Table 11. WDT Time Select

D1	D0	Timeout of Internal RC OSC	Timeout of System Clock
0	0	5 ms min	125 SCLK
0	1	10 ms min	256 SCLK
1	0	20 ms min	512 SCLK
1	1	80 ms min	2048 SCLK

Notes:
TpC = XTAL clock cycle.
The default on reset is 10 ms.

Note: The WDT can be permanently enabled through a mask programming option. The option is selected by the customer at the time of ROM code submittal. In this mode, WDT is always activated when the device comes out of reset. Execution of the WDT instruction serves to refresh the WDT time-out period. WDT operation in the HALT and STOP Modes is controlled by WDTMR programming. If this mask option is not selected at the time of ROM code submission, the WDT must be activated by the user through the WDT instruction and is always disabled by any reset to the device.

WDTMR During HALT (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Since the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

Note: A WDT timeout during STOP Mode will have the same effect as a recovery from any programmed Stop-Mode Recovery source, except the reset delay will occur.

Clock Source for WDT (D4)

This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator. The WDT is stopped in STOP Mode if the external pin XTAL1 drives the WDT.

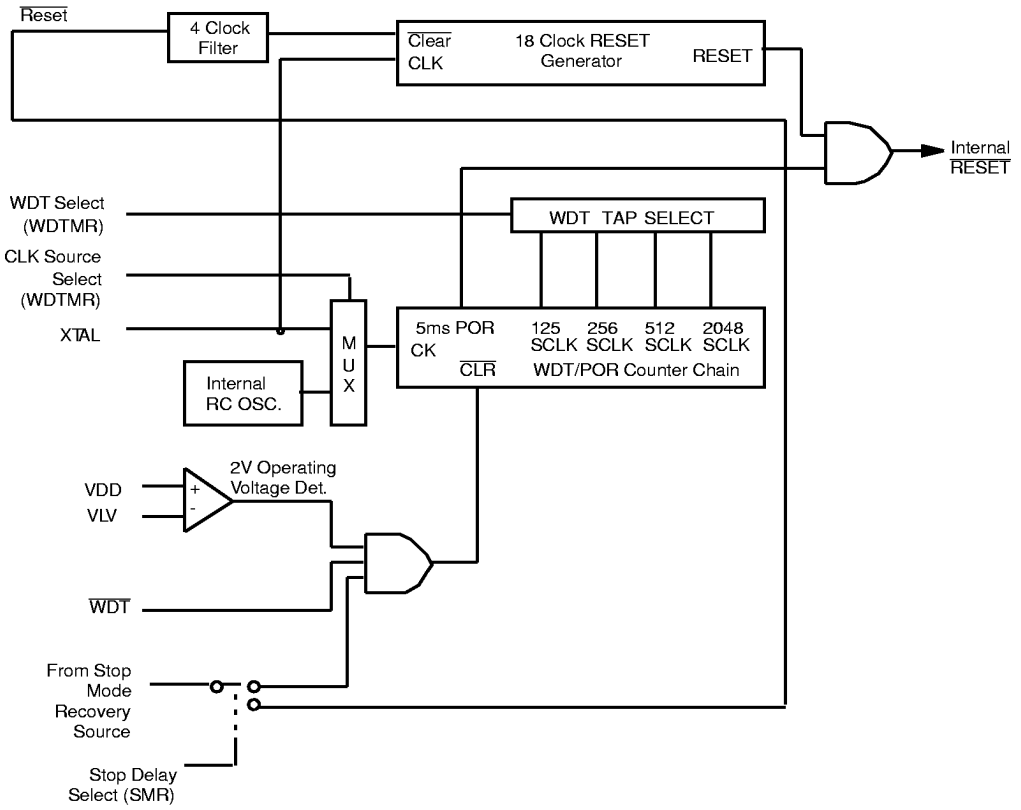


Figure 37. Resets and WDT

Mask Selectable Options

There are five Mask Selectable Options to choose from based on ROM code requirements. These are:

Clock Source	RC/XTAL
Port 0 Pull-ups	On/Off
Port 2 Pull-ups	On/Off
Port 3 Pull-ups	On/Off
Mouse/Normal	M/N

Low Voltage Detection/Standby

An on-chip Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{LV} (Low Voltage). The minimum operating voltage varies with the temperature and operating frequency, while V_{LV} varies with temperature only.

The Low Voltage trip voltage (V_{LV}) is less than 2.1V under the following conditions:

Maximum (V_{LV}) Conditions:

T_A = 0°C, +55°C Internal clock frequency equal to or less than 4.0 MHz

Note: The internal clock frequency is one-half the external clock frequency.

The device functions normally at or above 2.0V under all conditions. Below 2.0V, the device is guaranteed to function normally until the Low Voltage Protection trip point V_{LV} is reached, below which reset is globally driven and then the device is put in a low current stand by mode with the oscillator stopped. The device is guaranteed to function normally at supply voltages above the V_{LV} trip point for the temperatures and operating frequencies in maximum V_{LV} conditions. The actual V_{LV} trip point is a function of temperature and process parameters (Figure 38).

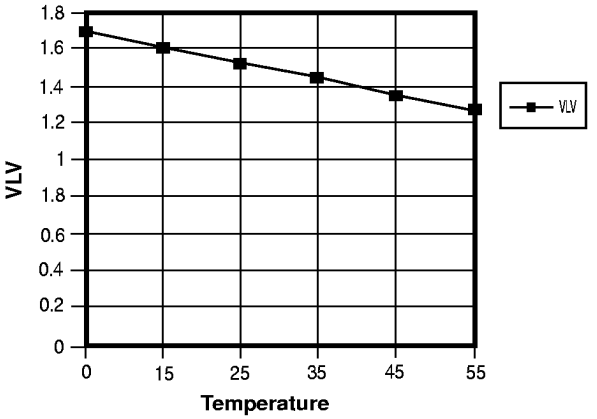


Figure 38. Typical Z86L79/80 Low Voltage vs. Temperature at 8 MHz

EXPANDED REGISTER FILE CONTROL REGISTERS (0D)

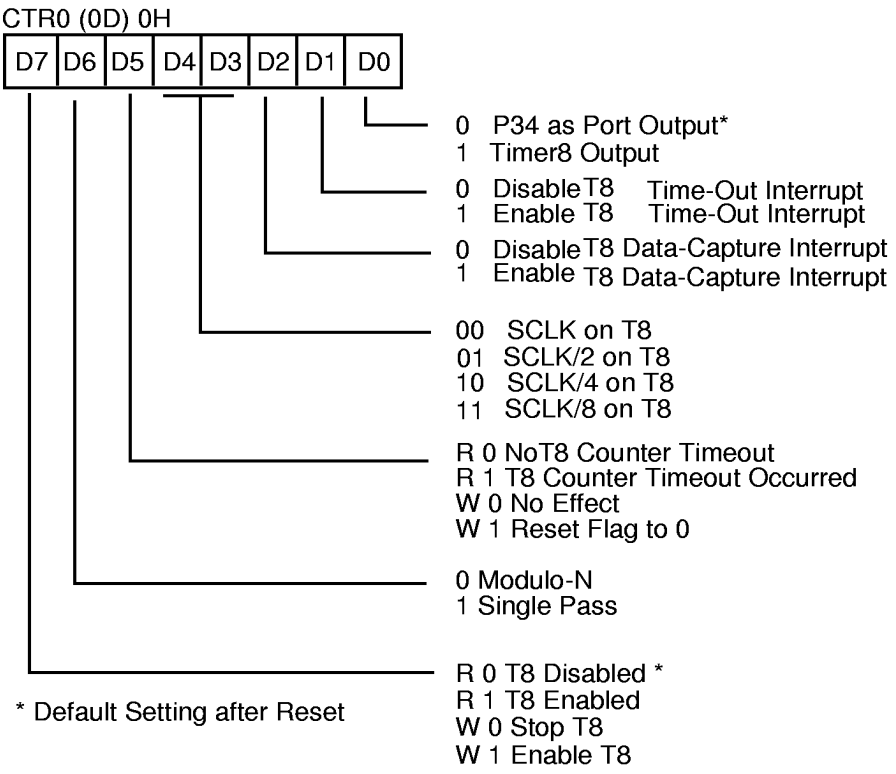


Figure 39. TC8 Control Register
((0D) 0H: Read/Write Accept Where Noted)

EXPANDED REGISTER FILE CONTROL REGISTERS (0D) (Continued)

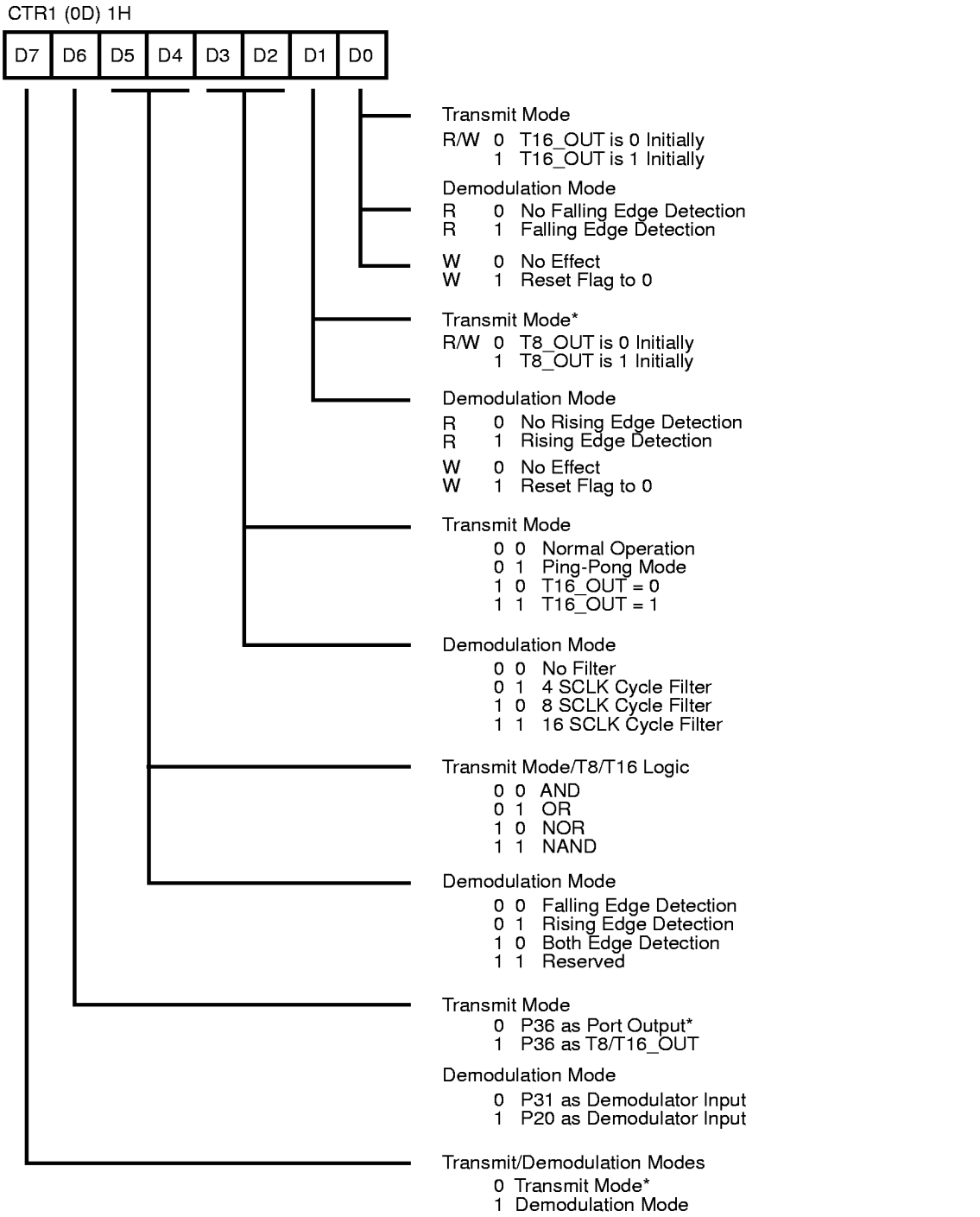


Figure 40. T8 and T16 Common Control Functions ((0D) 1H: Read/Write)

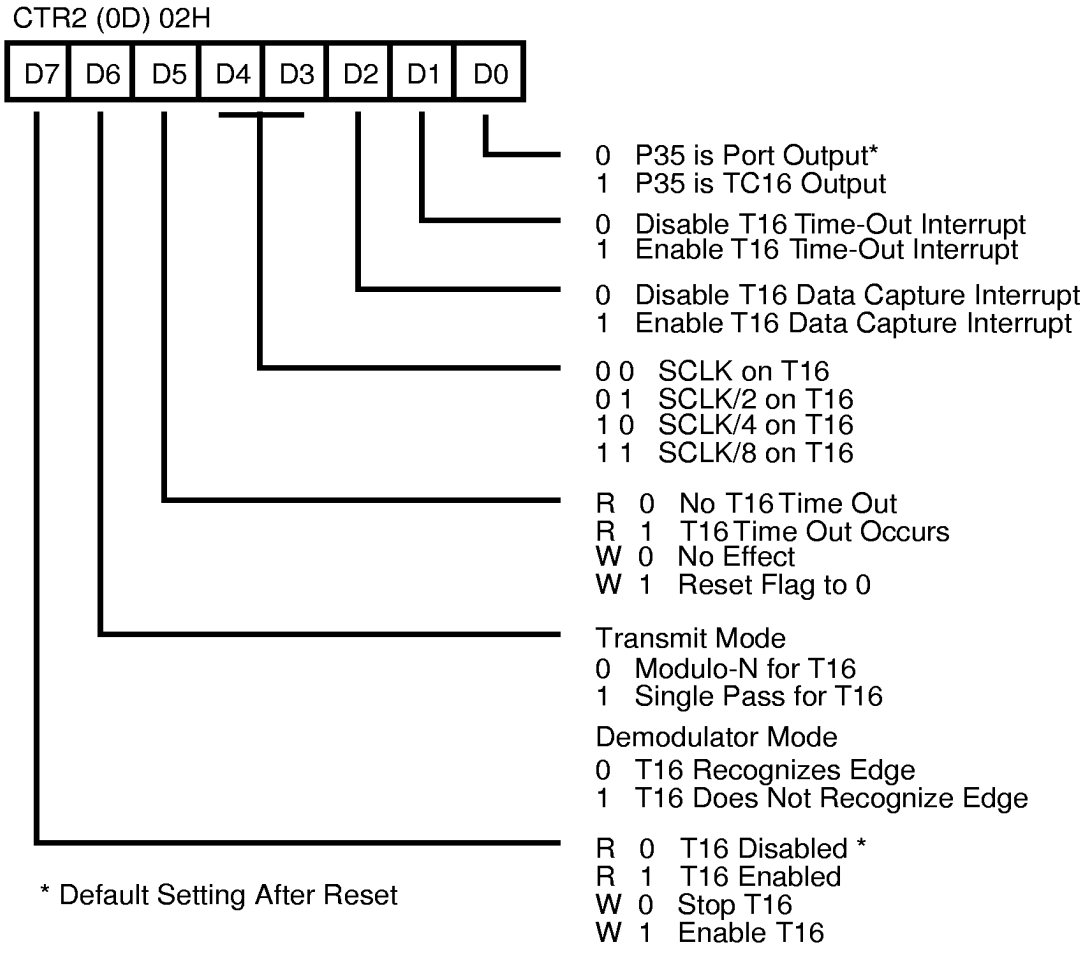


Figure 41. T16 Control Register
((0D) 2H: Read/Write Except Where Noted)

EXPANDED REGISTER FILE CONTROL REGISTERS (0D) (Continued)

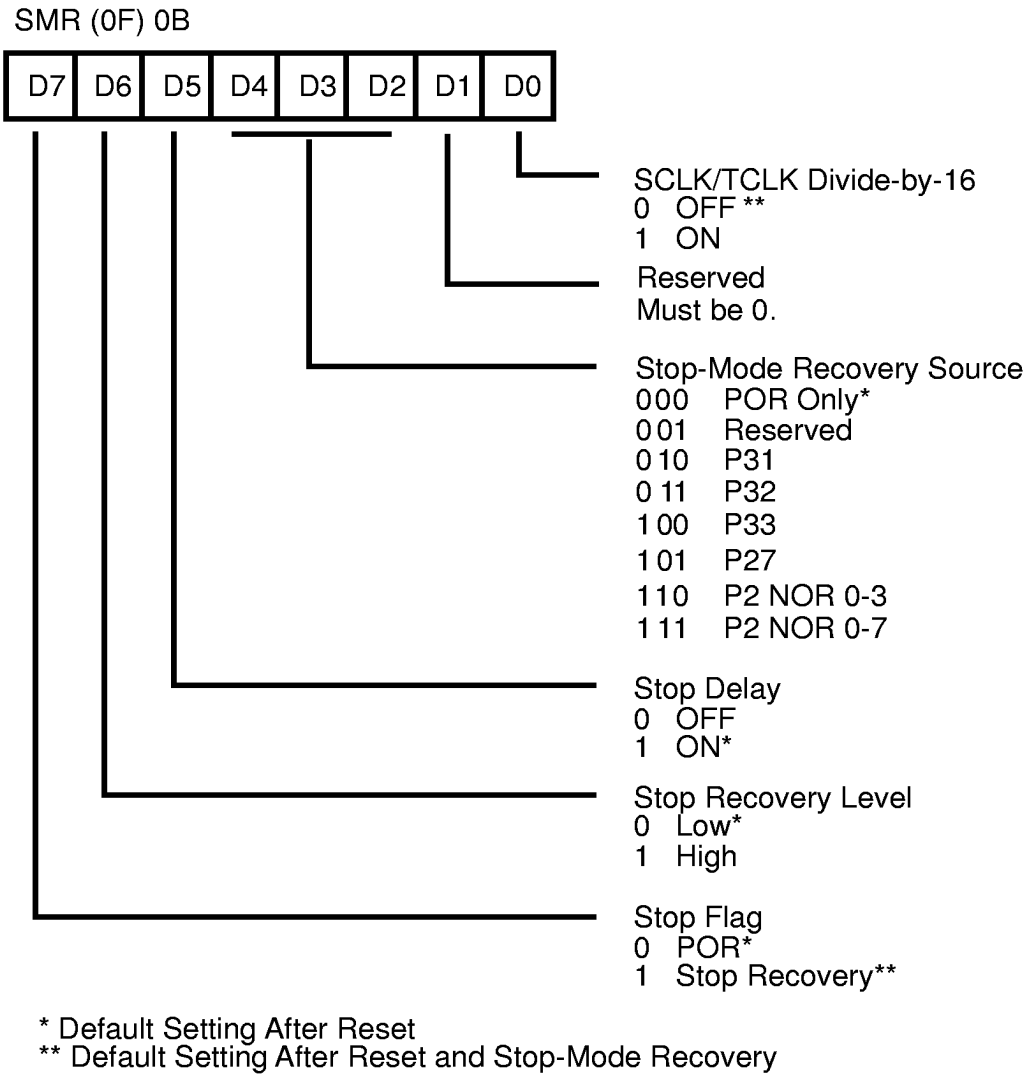


Figure 42. Stop-Mode Recovery Register ((F) 0BH: D6-D0 = Write Only)

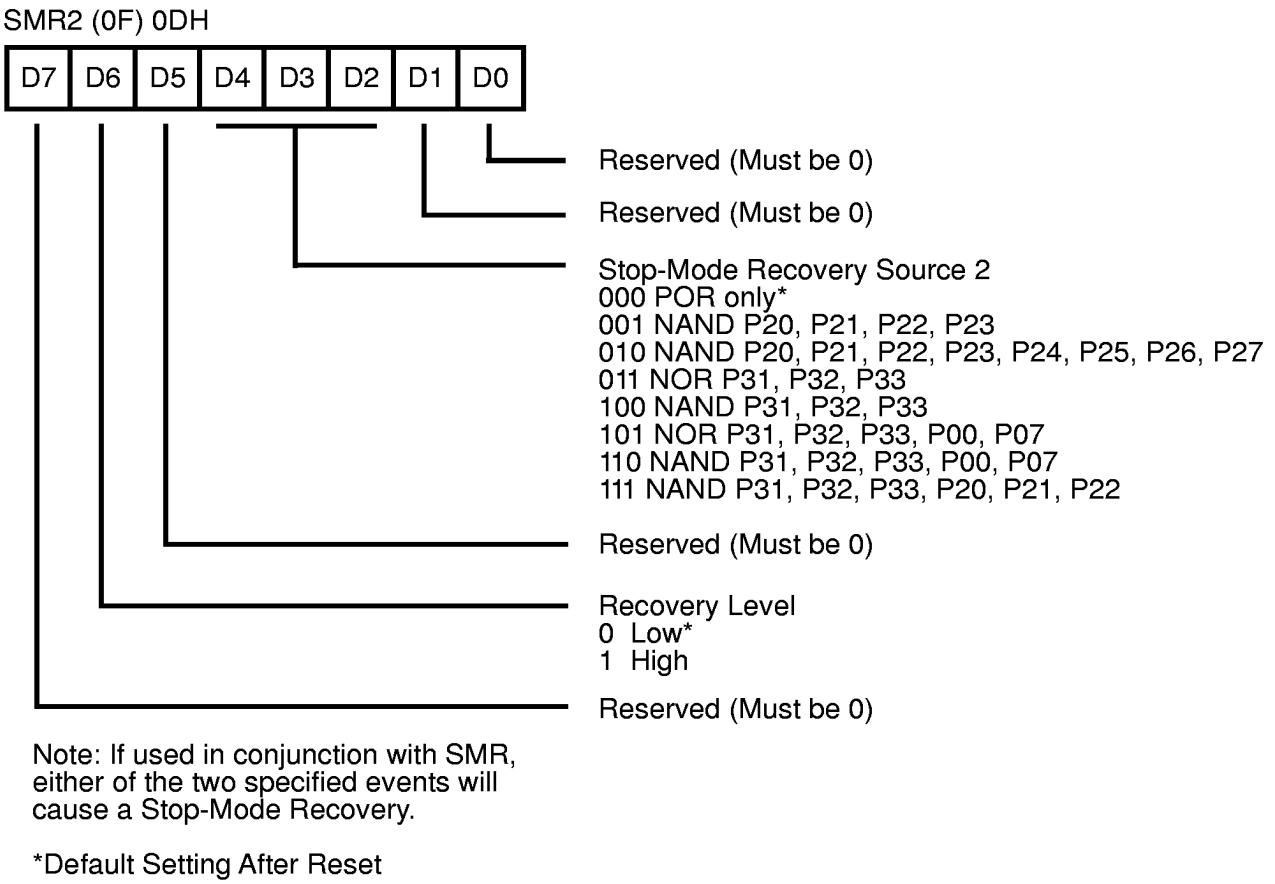


Figure 43. Stop-Mode Recovery Register 2 ((0F) DH: D2-DH, D6 Write Only)

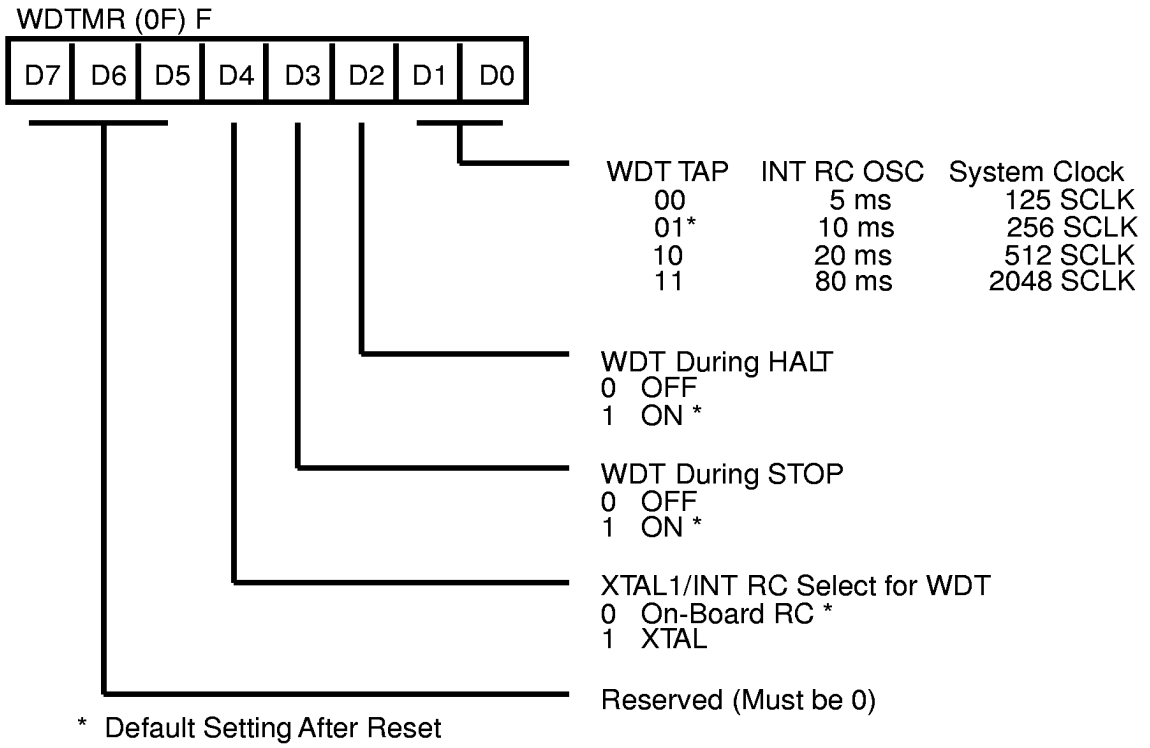


Figure 44. Watch-Dog Timer Mode Register ((F) OFH: Write Only)

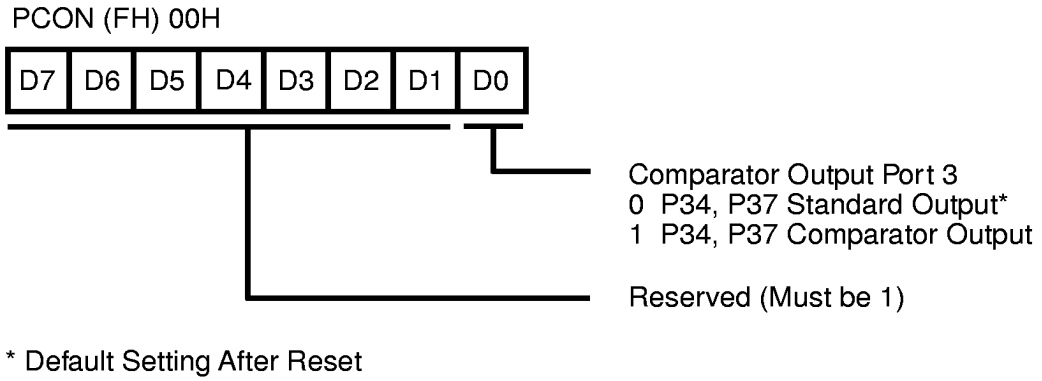


Figure 45. Port Configuration Register (PCON) ((0F) OH: Write Only)

Z8 STANDARD CONTROL REGISTER DIAGRAMS

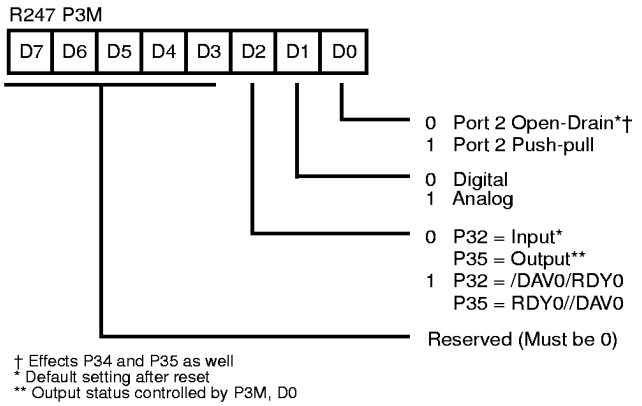


Figure 46. Port 3 Mode Register (F7H: Write Only)

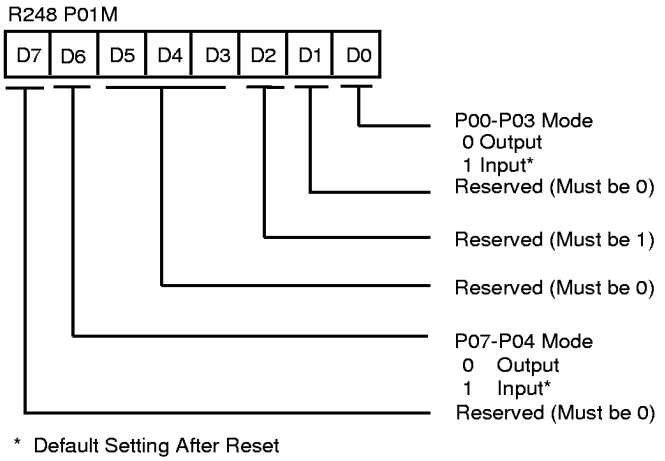


Figure 47. Port 0 and 1 Mode Register (F8H: Write Only)

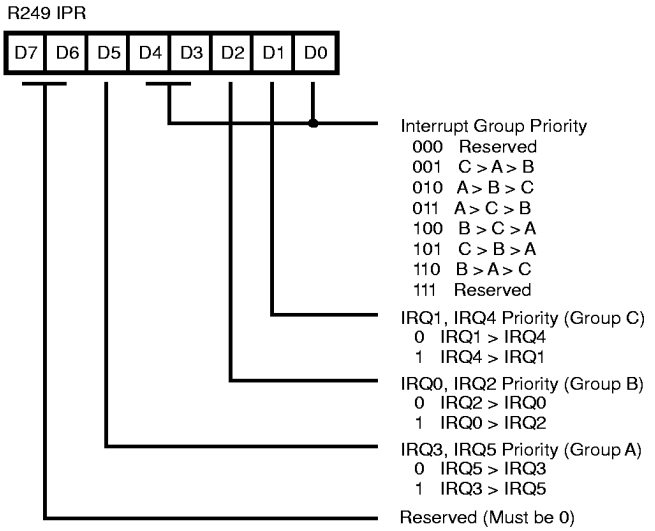


Figure 48. Interrupt Priority Registers ((0) F9H: Write Only)

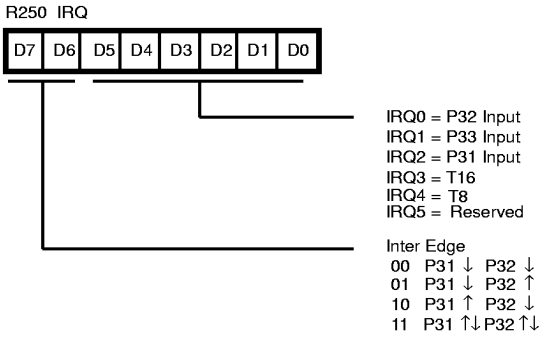


Figure 49. Interrupt Request Register ((0) FAH: Read/Write)

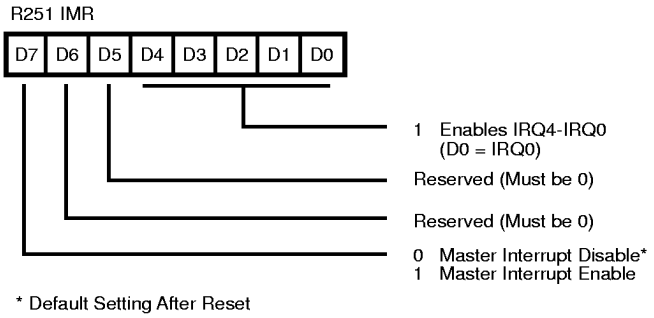


Figure 50. Interrupt Mask Register ((0) FBH: Read/Write)

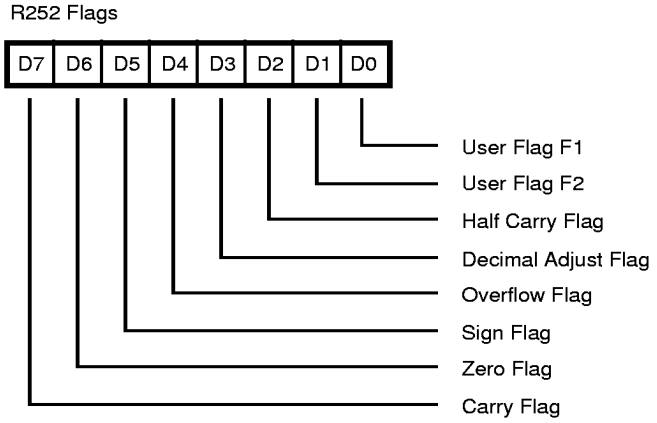


Figure 51. Flag Register ((0) FCH: Read/Write)

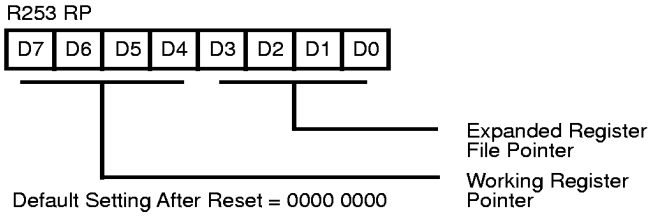


Figure 52. Register Pointer ((0) FDH: Read/Write)

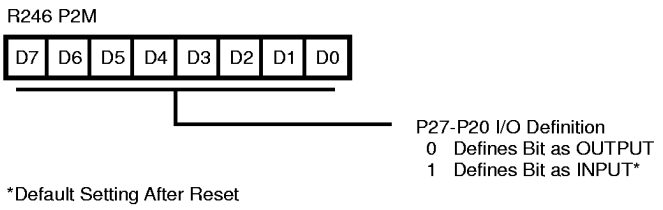


Figure 53. Port 2 Mode Register (F6H: Write Only)

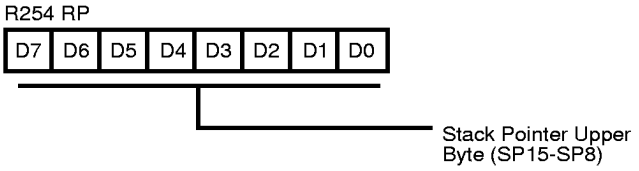


Figure 54. Stack Pointer High ((0) FEH: Read/Write)

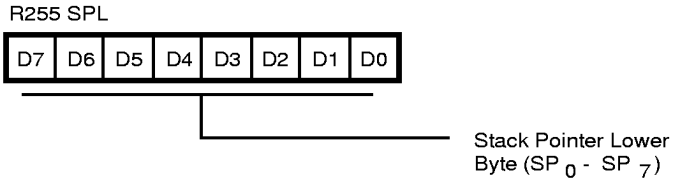
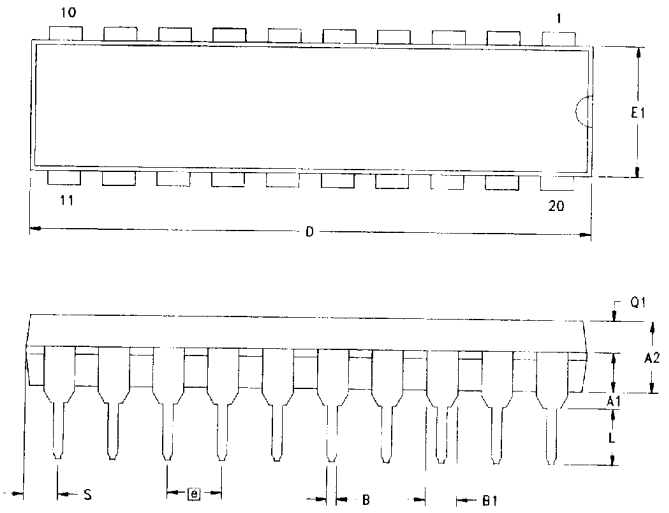


Figure 55. Stack Pointer Low ((0) FFH: Read/Write)

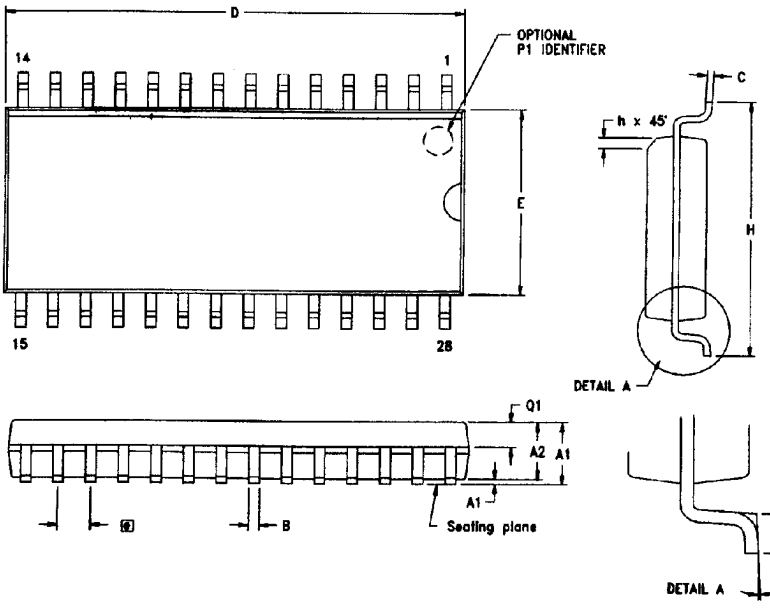
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	0.81	.015	.032
A2	3.25	3.68	.128	.145
B	0.41	0.5'	.016	.020
B1	1.47	1.57	.058	.062
C	0.20	0.30	.008	.012
D	25.65	26.16	1.010	1.030
E	7.49	8.26	.295	.325
E1	6.10	6.65	.240	.262
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.43	.125	.135
Q1	1.42	1.65	.056	.065
S	1.52	1.65	.060	.065

CONTROLLING DIMENSIONS : INCH

Figure 56. 28-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 typ		.050 typ	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 57. 28-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86L79/80

8.0 MHz

28-pin DIP	28-pin SOIC
Z86L7908PSC	Z86L7908SSC
Z86L8008PSC	Z86L8008SSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Codes

Package
P = Plastic DIP
S = SOIC (Small Outline Integrated Circuit)

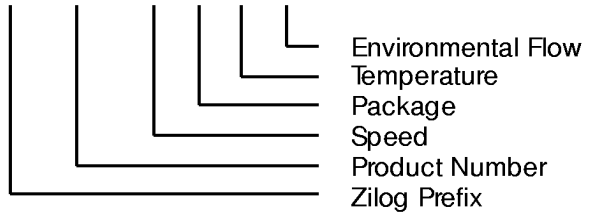
Temperature
S = 0°C to +70°C

Speed
8 = 8.0 MHz

Environmental
C = Plastic Standard

Example:

Z 86L79 08 P S C is a 4K ROM Z86L79, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



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