Z87000/Z87001

CORDLESS PHONE TRANSCEIVER/CONTROLLER

GENERAL DESCRIPTION

The Z87000 Cordless Phone Transceiver/Controller is expressly designed to implement a 900 MHz spread spectrum cordless phone compliant with U.S. FCC regulations for unlicensed operation. The Z87000 supports a specific cordless phone system design that uses frequency hopping and digital modulation to provide extended range, high voice quality, and low system costs, where the RF section in particular must be designed to be compatible.

The Z87000 uses Zilog's C00 16-bit fixed-point two's complement static CMOS Digital Signal Processor core as the phone and RF section controller. The Z87000's DSP core processor further supports control of the RF section's frequency synthesizer for frequency hopping and the generation of the control messages needed to coordinate interoperation of the phone's handset and base station.

The Z87001 is the in-circuit emulator (ICE) version of the Z87000, providing access to the DSP core.

Additional on-chip transceiver circuitry supports Frequency Shift Keying modulation/demodulation and multiplexing/demultiplexing of the 32 Kbps voice data and 4 Kbps command data between handset and base station. The Z87000 provides 32 I/O pins, including two wake-up inputs and two CPU interrupt inputs. These programmable I/O pins allow a variety of user-determined phone features and board layout configurations. Additionally, the pins may be used so that phone features and interfaces are supported by an optional microcontroller rather than by the Z87000's DSP core.

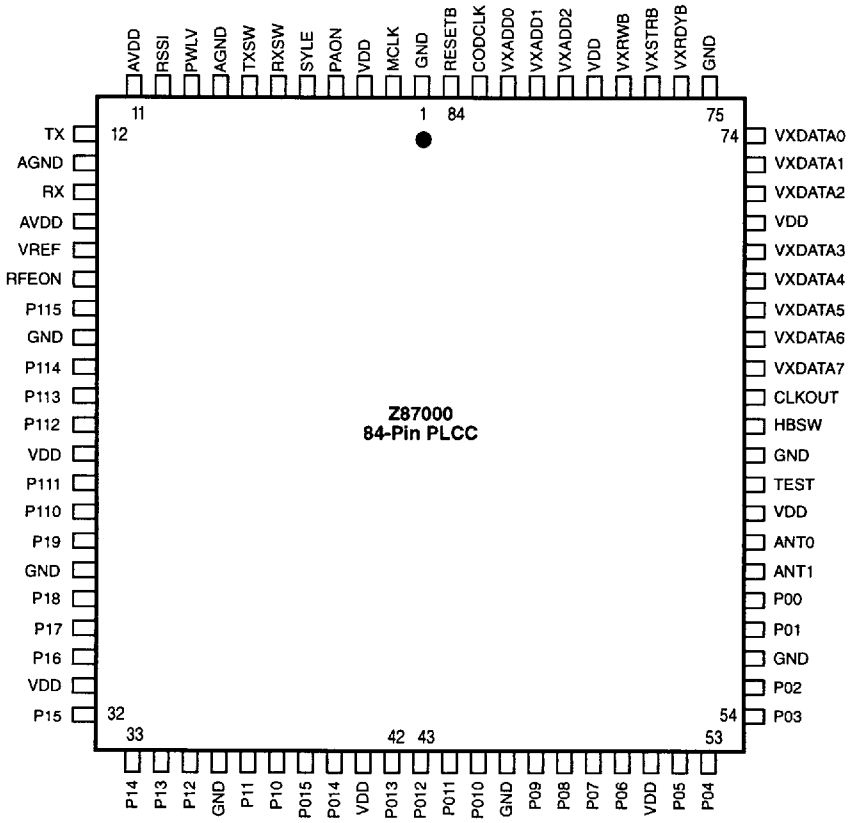
In combination with an RF section designed according to the system specifications, Zilog's Z87010 ADPCM Processor, and minimal additional phone circuitry, the Z87000 and its embedded software provide a total system solution.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

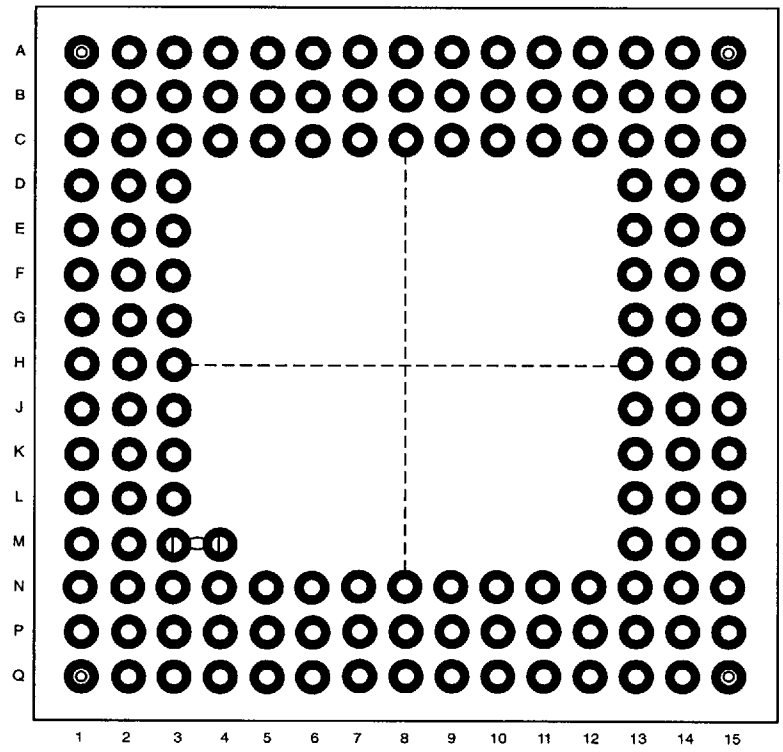
Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

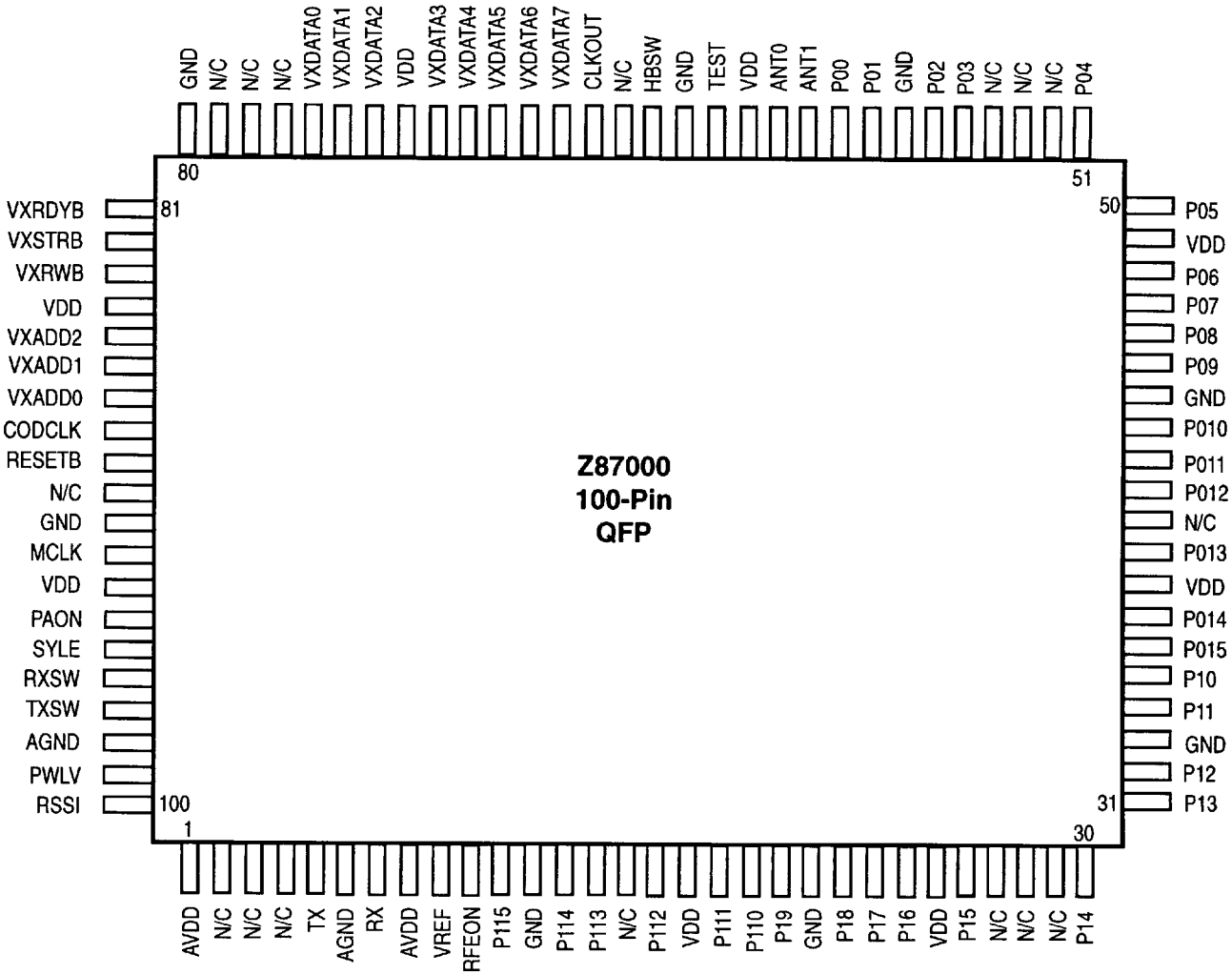
PIN DESCRIPTION



84-Pin PLCC Pin Assignments



144-Pin PGA Pin Assignments



100-Pin QFP Pin Assignments

PIN DESCRIPTION (Continued)

Table 1. Nominal Pin Description

PIN		CONFIGURATION		PACKAGE		
NAME	MAIN FUNCTION	Main Direction	Reset	Z87000 84-PLCC	Z87000 100-QFP	Z87001 144-PGA
VDD	Digital VDD	-	-	3, 23, 31, 41, 51, 61, 71, 79	17, 25, 38, 49, 62, 73, 84, 93	H3, N3, R7, R14, K15, E13, A12, B6
GND	Digital ground	-	-	1, 19, 27, 36, 46, 56, 63, 75	12, 21, 33, 44, 57, 64, 80, 91	F2, L2, P5, N10, L13, H14, C12, A7
AVDD	Analog VDD	-	-	11, 15	1, 8	D2, A1
AGND	Analog ground	-	-	8, 13	6,	C2, C4
VREF	Analog reference voltage for RX signal	AO	O	16	9	E3
RX	Analog receive IF signal	AI	I	14	7	B1
TX	Analog transmit IF signal	AO	O	12	5	D3
RXSW	RF receive switch control	O	O	6	96	B4
TXSW	RF transmit switch control	O	O	7	97	B3
PAON	RF power amplifier on/off control	O	O	4	94	A5
RFEON	RF module on/off control	O	O	17	10	C1
RSSI	RF receive signal strength indicator	AI	I	10	100	B2
PWLV	RF transmit power level	AO	O	9	99	C3
SYLE	RF synthesizer load enable	O	O	5	95	A4
ANT[1..0]	RF diversity antenna control Test mode controls	O I	O/I	[59, 60]	[60, 61]	[K14, J14]
MCLK	Master clock input (16.384 MHz)	I	I	2	92	B7
CLKOUT	Clock output to voice processor	O	O	65	67	G15
CODCLK	Clock output to codec	O	O	83	88	B8
RESETB	Reset signal	I	I	84	89	C8
VXADD[2..0]	Voice processor address bus	I	I	[80, 81, 82]	[85, 86, 87]	[B10, B9, A10]
VXDATA[7..0]	Voice processor data bus	I/O	I	[66, 67, 68, 69, 70, 72, 73, 74]	[68, 69, 70, 71, 72, 74, 75, 76]	[G14, F14, E15, D15, D14, B15, C13, A15]
VXSTRB	Voice processor data strobe	I	I	77	82	B12
VXRWB	Voice processor read/write control	I	I	78	83	A13
VXRDYB	Voice processor ready signal	O	O	76	81	B13
TEST	Main test mode control	I, PD	I	62	63	J15
HBSW	Handset/Base control	I, PU	I	64	65	H13
P0[15..0]	General purpose I/O port 0	I/O	I	[39, 40, 42, 43, 44, 45, 47, 48, 49, 50, 52, 53, 54, 55, 57, 58]	[36, 37, 39, 41, 42, 43, 45, 46, 47, 48, 50, 51, 55, 56, 58, 59]	[P7, R6, R8, N9, R10, P9, P11, R13, P12, P13, N13, R15, M13, P15, L14, M15]

PIN DESCRIPTION (Continued)

Table 1. Nominal Pin Description (continued)

PIN		CONFIGURATION		PACKAGE		
NAME	MAIN FUNCTION	Main Direction	Reset	Z87000 84-PLCC	Z87000 100-QFP	Z87001 144-PGA
P1[15..0]	General purpose I/O port 1	I/O	I	[18, 20, 21, 22, 24, 25, 26, 28, 29, 30, 32, 33, 34, 35, 37, 38]	[11, 13, 14, 16, 18, 19, 20, 22, 23, 24, 26, 30, 31, 32, 34, 35]	[D1, G2, F1, H2, J1, J2, K3, N1, L3, P1, R1, N4, R2, N5, R4, P6]
addr[15..0]	DSP core program address bus (tristatable)	O/Z	O/Z	NA	NA	[A3, C5, A2, E2, F3, E1, G3, G1, H1, J3, K1, K2, L1, M1, M2, N2]
data[15..0]	DSP core program data bus	I	I	NA	NA	[P14, N14, M14, N15, K13, L15, J13, H15, G13, F15, F13, E14, C15, C14, D13, B14]
triadd	Tristate control for program address bus	I, PU	I	NA	NA	C6
dspclk	DSP core clock	O/Z	O/Z	NA	NA	B5
halt	Halt/single step control	I, PD	I	NA	NA	A6
intenb	Enable interrupt control	I, PD	I	NA	NA	C7
iaddr[4..0]	External register address bus	O/Z	O/Z	NA	NA	[C11, C10, A11, C9, A9]
idata[15..0]	DSP core internal bus	O/Z	O/Z	NA	NA	[M3, P2, P3, P4, R3, N6, R5, N7, P8, N8, R9, P10, R11, R12, N11, N12]
eib	External register data strobe	O/Z	O/Z	NA	NA	A14
irwb	External register read/write control	O/Z	O/Z	NA	NA	A8
trice	ICE mode control	I, PU	I	NA	NA	B11
nc	null connect	NA	NA	NA	2, 3, 4, 15, 27, 28, 29, 40, 52, 53, 54, 66, 77, 78, 79, 90	NA

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min.	Max.	Units
V_{DD}.AV_{DD}	DC Supply Voltage[a]	-0.5	7.0	V
V_{IN}	Input Voltage[b]	-0.5	V_{DD}+0.5	V
V_{OUT}	Output Voltage[c]	-0.5	V_{DD}+0.5	V
T_A	Operating Temperature	-20	+85	°C
T_{STG}	Storage Temperature	-65	+150	°C

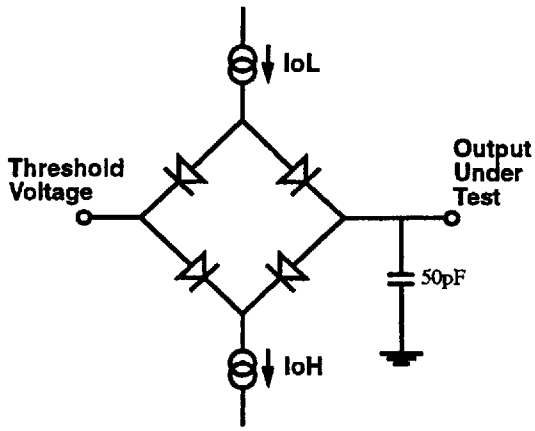
Notes:
a) Voltage on all pins with respect to GND.
b) Voltage on all inupts with respect to V_{DD}.
c) Voltage on all outputs with respect to V_{DD}.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pins. Standard test conditions are as follows:

- $4.0V \leq V_{DD} \leq 5.5V$
- GND = 0V
- T_A = -20 to +85 °C



Test Load Diagram

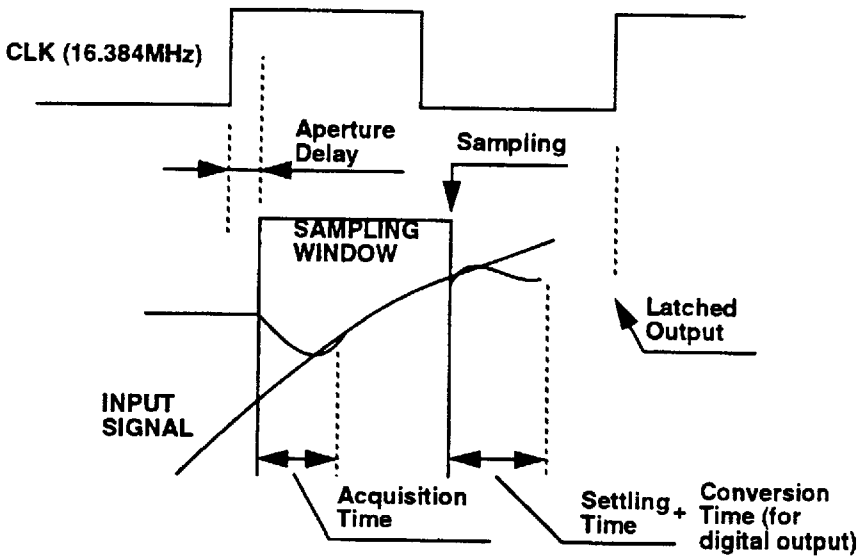
ANALOG CHARACTERISTICS

Table 2. 1-Bit ADC (Temperature: –20 ±85°C)

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
Resolution	-	1	-	bit
Power dissipation	0.54 (3V, 85°C)	1.0 (5V, 40°C)	2.75 (5.5V, -20°C)	mW
Power dissipation, stop mode	0.06 (3V, 85°C)	0.2 (5V, 40°C)	1.1 (5.5V, -20°C)	mW
Sample frequency	-	8.192	-	MHz
Sample window[a]	29	31	33	ns
Bandwidth	-	60	-	MHz
Supply range (= AVDD)	4.0		5.5	V
Acquisition time	2	3	8	ns
Settling time	8	10	18	ns
Conversion time	4	6	18	ns
Aperture delay	2	3	8.5	ns
Aperture uncertainty[b]	-	-	0.5	ns
Input voltage range (p-p)	800	1000	1200	mV
Reference voltage	1.68 (at 3V)	3.03 (at 5V)	3.36 (at 5.5V)	V
Input resistance	10	18	25	KOhm
Input capacitance	-	1.5	-	pF

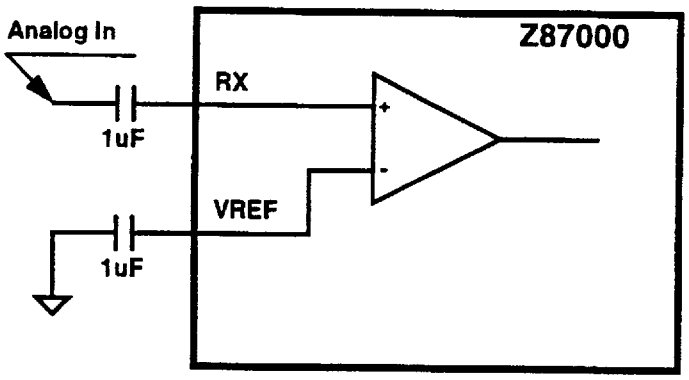
a. Window of time while input signal is applied to sampling capacitor; see next figure

b. Uncertainty in sampling time due to random variations such as thermal noise.



1-Bit ADC Definition of Terms

ANALOG CHARACTERISTICS (Continued)



Application Circuit

Table 3. 8-Bit ADC (Temperature: –20 ±85°C)

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
Resolution[a]	-	6	-	bit
Integral non-linearity	-	0.5	1	LSB
Differential non-linearity	-	-	0.5	LSB
Power dissipation (peak)	-	35 (at 5V)	70 (at 5.5V)	mW
Sample window	5	-	120	ns
Bandwidth	-	-	2	Msps
Supply range (=AVDD)	4.0		5.5	V
Input voltage range		0-AVDD		V
Conversion time	0.5	-	-	µs
Aperture delay	2	3	8.5	ns
Aperture uncertainty	-	-	1	ns
Input resistance	-	25	-	KOhm
Input capacitance	-	5	-	pF

a. 8-bit ADC only tested for 6-bit resolution

ANALOG CHARACTERISTICS (Continued)

Table 4. 4-Bit DAC (Temperature: –20°C ±85°C)

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
Resolution	-	4	-	bit
Integral non-linearity	-	0.25	0.5	LSB
Differential non-linearity	-	0.25	1	LSB
Settling time (1/2 LSB)	-	-	22.5	ns
Zero error at 25°C	-	1	2	mV
Power dissipation, 25pF load	1.2 (3V, 85°C)	20 (5V, 40°C)	24.1 (5.5V, -20°C)	mW
Power dissipation, 25pF load, stop mode	0.18 (3V, 85°C)	1.0 (5V, 40°C)	1.1 (5.5V, -20°C)	mW
Conversion time (input change to output change)	14.5	19.1	75.8	ns
Rise time (full swing)	11.5	15.4	70.3	ns
Output slew rate	8.5	66.7	95.6	V/µs
Supply range (= AVDD)	4.0		5.5	V
Output voltage range	-	0.2 VDD to 0.4 VDD	-	V
Resistive output load	-	330	-	Ohm
Capacitive output load	-	25	-	pF

DC ELECTRICAL CHARACTERISTICS

(Per Standard Test Conditions, Unless Otherwise Specified)

Symbol	Parameter	Condition	Min.	Max.	Units
ViH	Input High Voltage		0.7 VDD	VDD +0.3	V
ViL	Input Low Voltage		GND –0.3	0.1 VDD	V
VoH	Output High Voltage	I_{OH} = –2.0 mA	2.4		V
VoL1	Output Low Voltage	I_{OL} = +4.0 mA		0.4	V
VoL2	Output Low Voltage, Ports[a]	I_{OL} = +12.0 mA		1.2	V
IL	Input Leakage	V_{IN} = 0V, VDD	–2	2	µA
ICC	Supply Current	I_{OH} = –100 µA		80	mA
ICC2	Standby Mode Current			100[b]	µA

Notes:

a) Max. three pins total from P0[15..0] and P1[15..0].

b) Execution of LDA, RAM_BANK with null data is necessary to ensure low ICC2.

AC ELECTRICAL CHARACTERISTICS

(Per Standard Test Conditions, Unless Otherwise Specified)

Clocks, Reset, RF Interface, ADPCM Processor Interface

No.	Symbol	Parameter	Min.	Max.	Units
1	TpC	MCLK Input Clock Period[a]	61	61	ns
2	TwC	MCLK Input Clock Pulse Width	20	40	ns
3	TrC, TfC	MCLK Input Clock Rise/Fall Time		15	ns
4	TrCC, TfCC	CLKOUT Output Clock Rise/Fall Time	2	6	ns
5	TrCO, TfCO	CODCLK Output Clock Rise/Fall Time	2	6	
6	TwR	RESETB Input Low Width	18		TpC
7	TrRF, TfRF	RF Output Controls[b] Rise/Fall Time	2	6	ns
8	TsAS	Address, Read/Write Setup Time Before Strobe Falls	10		ns
9	ThSA	Address, Read/Write Hold Time After Strobe Rises	3		ns
10	TaDrS	Data Read Access Time After Strobe Falls		30[c]	ns
11	ThDrS	Data Read Hold Time After Strobe Rises	8.5	40[d]	ns
12	TwS	Strobe Pulse Width	20		
13	TsDwS	Data Write Setup Time Before Strobe Rises	10		ns
14	ThDwS	Data Write Hold Time After Strobe Rises	3		ns
15	TaDrRY	Data Read Access Time After Ready Falls	22		ns
16	TdSRY	Strobe High After Ready Falls	0		ns

Notes:

a) MCLK is 16.384 MHz ± 25 ppm.

b) RF Controls are TXSW, RXSW, PAON, RFEON, SYLE.

c) Requires Wait State on ADPCM processor read cycles.

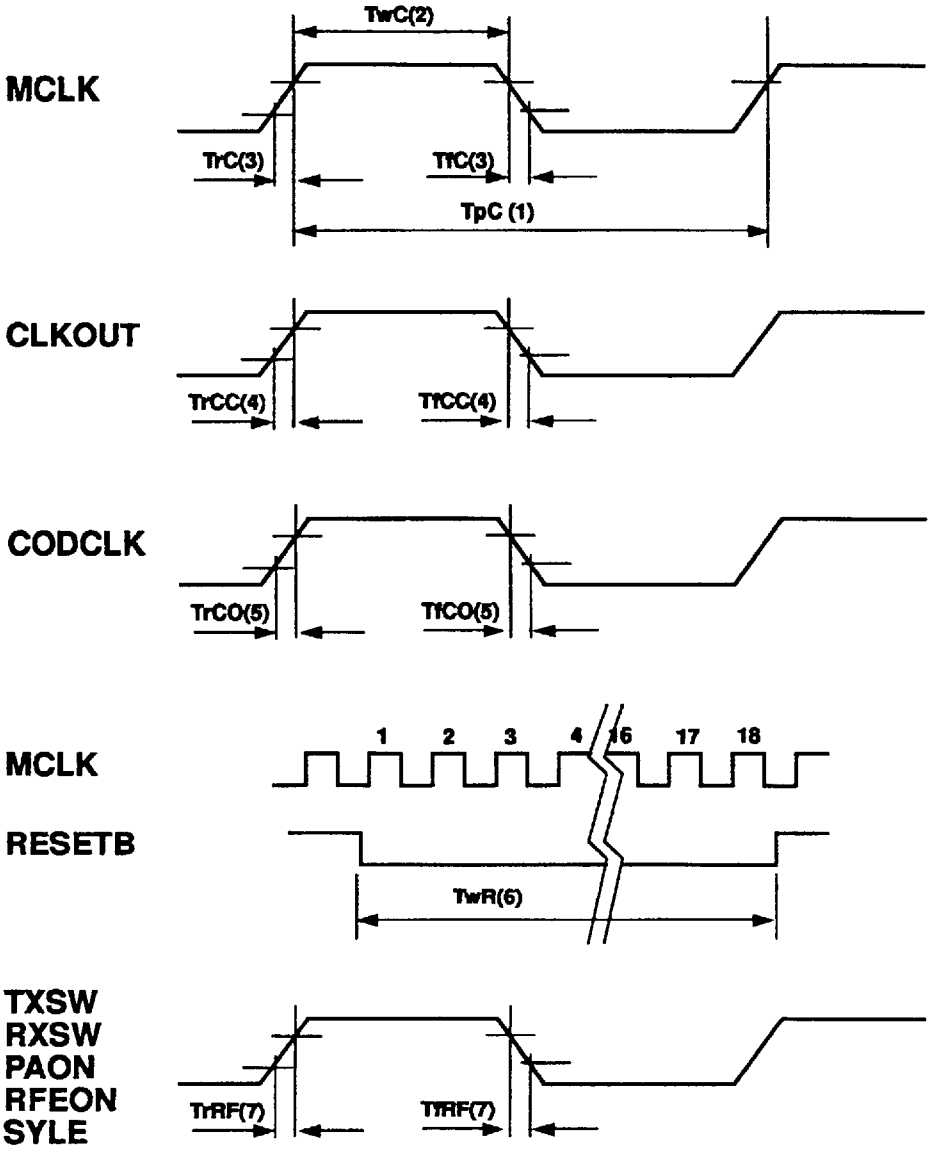
d) Requires no Write Cycle directly following Read Cycle on ADPCM processor.

AC ELECTRICAL CHARACTERISTICS (Continued)

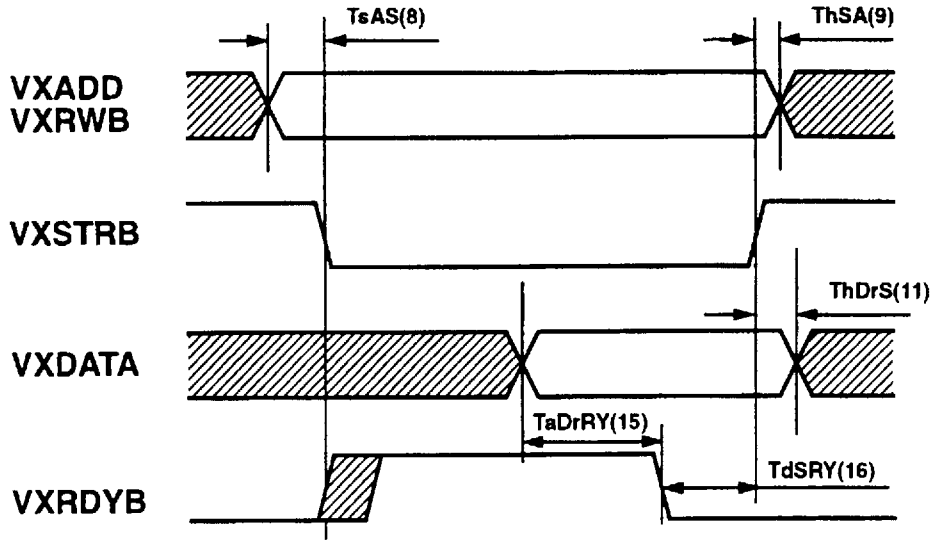
ADPCM Processor Interface

Signal Name	Function	Direction
VXADD[2..0]	Address Bus	ADPCM Processor to Z87000
VXDATA[7..0]	Data Bus	Bi-directional
VXSTRB	Strobe Control Signal	ADPCM Processor to Z87000
VXRWB	Read/Write Control Signal	ADPCM Processor to Z87000
VXRDYB	Ready Control Signal	Z87000 to ADPCM Processor

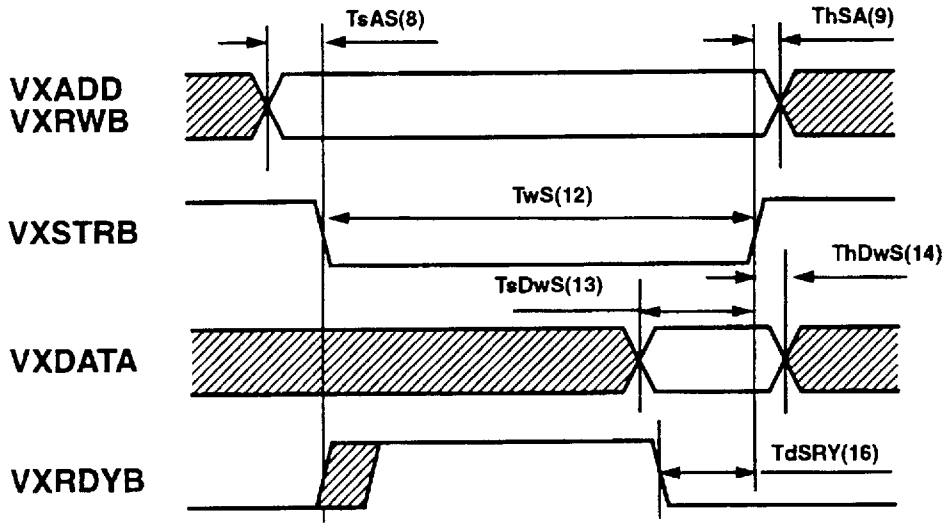
TIMING DIAGRAMS



TIMING DIAGRAMS (Continued)



VXDATA Read Cycle with Wait State



VXDATA Write Cycle with Wait State

Pre-Characterization Product:
The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Low Margin:
Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

Zilog's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the customer and Zilog prior to use. Life support devices or systems are those which are intended for surgical implantation into the body, or which sustains life whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

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