Z89300 SERIES

DIGITAL TELEVISION CONTROLLERS

FEATURES AND BENEFITS

- Advanced TV controller IC with sophisticated On-Screen Display capability and integral VBI data decoding.
- 40-pin DIP, 42-pin shrink DIP and 52-pin shrink DIP versions with ROM sizes varying from 10K words to 24K words provide application diversity.
- 40-pin DIP, 42-pin SDIP and 52-pin SDIP OTP versions enable easy development and flexible small scale production.
- 16-bit single cycle RISC core provides very fast instruction throughput.
- I.R. (Infrared) remote capture register facilitates reliable capture of remote data even in high noise environments.
- 6-channel, 4-bit ADC (Analog to Digital Converter) supports multiple tuner AFT, analog keypad entry, audio level input and VBI (Vertical Blank Interval) data capture. Subsequent digital processing of VBI data results in excellent signal to noise ratio performance.
- Up to 10 PWM (Pulse Width Modulator) outputs allow low cost digital to analog conversion (with addition of external low pass filter circuits). Eight PWM's have 8-bit resolution for control of video and audio attributes. Two PWMs have 14-bit resolution to optionally control external VST (Voltage Synthesis Tuner).
- Master/slave I^2C (Inter Integrated Circuit) Philips Standard Serial Interface provides serial system interconnect to common peripheral functions.
- Bit programmable I/O ports provide flexibility for miscellaneous digital input/output functions.
- 24.0 MHz nominal PLL (Phase Lock Loop) controlled oscillators provide stable system and video clocks. Only one external capacitor is required for the loop filter function. A 32 kHz oscillator is used for reference.
- Hsync, Vsync and Composite sync generation circuits provide a video timebase (typically for VCR and set-top applications) in the absence of an available video signal.
- Micro-programmable OSD (On-Screen Display) generation logic provides ultimate flexibility to tailor OSD features and functions. In addition to normal OSD functions Closed-Captioning is supported in accordance with FCC Report and Order on GEN Docket No. 91-1, dated April 12. 1991. EDS and StarSight Telecast, Inc. on-screen TV program guide capability can be implemented as well with the 89300.
- High definition characters offer the ability to display complex characters.
- Program and character generator data contained in the one ROM space-simplifies mask ROM code submission and gives flexibility in size of character ROM. Up to 512 characters with 16x16, 16x18 or 16x20 programmable matrix
- ICEBOX™ Emulator provides in-circuit emulation for program debug.
- Zilog supplied ATB (Application Tool Box) software provides microcode support for VBI data capture, I.R. remote data capture, and OSD display including specific requirements of Starsight and Closed Captioning.

DEVICE IDENTIFICATION AND SUMMARY

Zilog's Z893xx family of television controller products combine On-Screen Display and VBI data capture functions to provide a highly integrated solution for TV, VCR and set-top applications. Family members serve as either stand-alone controllers providing the most cost effective central processing facility or as add-on controllers where time-to-market is a key factor. Common to all devices is a high-speed 16-bit RISC controller that provides ultimate OSD flexibility and allows for digital VBI data capture. The power of the Z893xx family architecture is evident by it's ability to support a variety of OSD applications including Line 21 closed-caption, EDS and Starsight. Table 1 summarizes the features of the devices in the family.

In Circuit Emulation is facilitated by the Z89309 124-pin PGA device. The Z89332/6 are 24K/12K ROM variants in 42-pin SDIP package.

One Time Programmable versions of the parts Z89300/ Z89331, are offered for development and small scale production.

The Z89302, Z89303, Z89304, Z89305, Z89306 and Z89307/8/13/14 are mask ROM devices intended for high volume TV chassis production applications. They offer 40-pin, DIP and 52-pins DIP package configurations with 10K, 12K word, 16K word, and 24K word program memory sizes.

Table 1. Zilog Z893xx Product Family

Device	Application	Feature Summary							
		ROM (word)	RAM (word)	Pkg.	I^2C	IR Capture	ADC	Bit I/O	PWM
Z89300	TV Receiver Controller OTP	24K OTP	640	40-DIP	Yes	Yes	3-ch	19	7
Z89301	TV Receiver Controller OTP	24K OTP	640	50-SDIP	Yes	Yes	4-ch	26	9
Z89309	TV Receiver Controller ICE device	Bond Out	640	124 PGA	Yes	Yes	6-ch	26	10
Z89302	TV Receiver Controller	24K Mask	640	40-DIP	Yes	Yes	3-ch	19	7
Z89303	TV Receiver Controller	24K Mask	640	52-SDIP	Yes	Yes	4-ch	26	9
Z89313	TV Receiver Controller	24K Mask	640	52-SDIP	Yes	Yes	4-ch	26	9
Z89304	TV Receiver Controller	16K Mask	640	40-DIP	Yes	Yes	3-ch	19	7
Z89305	TV Receiver Controller	16K Mask	640	52-SDIP	Yes	Yes	4-ch	26	9
Z89306	TV Receiver Controller	12K Mask	640	40-DIP	Yes	Yes	3-ch	19	7
Z89307	TV Receiver Controller	12K Mask	640	52-SDIP	Yes	Yes	4-ch	26	9
Z89331	One Time Programmable	24K OTP	640	42-SDIP	Yes	Yes	5-ch	20	7
Z89332	TV Receiver Controller	24K Mask	640	42-SDIP	Yes	Yes	5-ch	20	7
Z89336	TV Receiver Controller	12K Mask	640	42-SDIP	Yes	Yes	5-ch	20	7
Z89314	TV Receiver Controller	16K Mask	512	40-DIP	No	Yes	3-ch	19	7
Z89318	TV Receiver Controller	10K Mask	512	40-DIP	No	Yes	3-ch	19	7

FUNCTIONAL DESCRIPTION

Capture Function

The capture function is intended for Infrared Remote data capture. It employs a capture register that holds the time value from one transition of I.R. data to the next.

The CPU can periodically check the capture status and read the value if a new capture has occurred. Subsequent decoding and command passing of the received I.R. signal is under program control.

Pulse Width Modulator Function

Pulse Width Modulation is used in conjunction with external low pass filters to perform digital to analog conversion. Eight PWM's of 8-bit resolution each find application in generating 0-12 volt signals for control of video and sound attributes. Two 14-bit resolution PWMs may be used with external circuits to generate the controlling voltage for voltage synthesis tuners. In the case of the chassis employing a frequency synthesis tuner, this PWM may also control video or sound attributes.

Each PWM circuit has a data register whose content are set under program control. The data in the register determines the ratio of PWM high to PWM low time.

Analog to Digital Converter Function

This function employs a 4-bit resolution, flash A to D converter. A six to one input multiplexor and conversion start circuits are controlled by the user program. The 4-bit conversion result is available to be read by the CPU at the end of each conversion.

One input channel (ADC0) is dedicated for quantizing VBI (vertical blank interval) data for subsequent digital signal processing. The other channel (ADC5) is typically used for V-SYNC separation from the composite TV signal. These channels have a special video clamp circuit that provides DC restoration of the composite video input signal. Typical VBI applications include Line 21 Closed-Caption, Electronic Data Services and Starsight Telecast. The range of ADC0 and ADC4 is 0.5V p-p from 1.5V to 2.0V.

The remaining four channels are general-purpose. They are typically used for implementation of tuner automatic frequency control and analog key entry. The range of ADC1/2/3/4 is from 0V to 5.0V.

Port Functions

Two input/output port blocks are available for general-purpose digital I/O application. Each port bit is programmable to be either input or output. To conserve device pin count, some port pins are mapped to provide I/0 to the A to D converter block and I²C interface block.

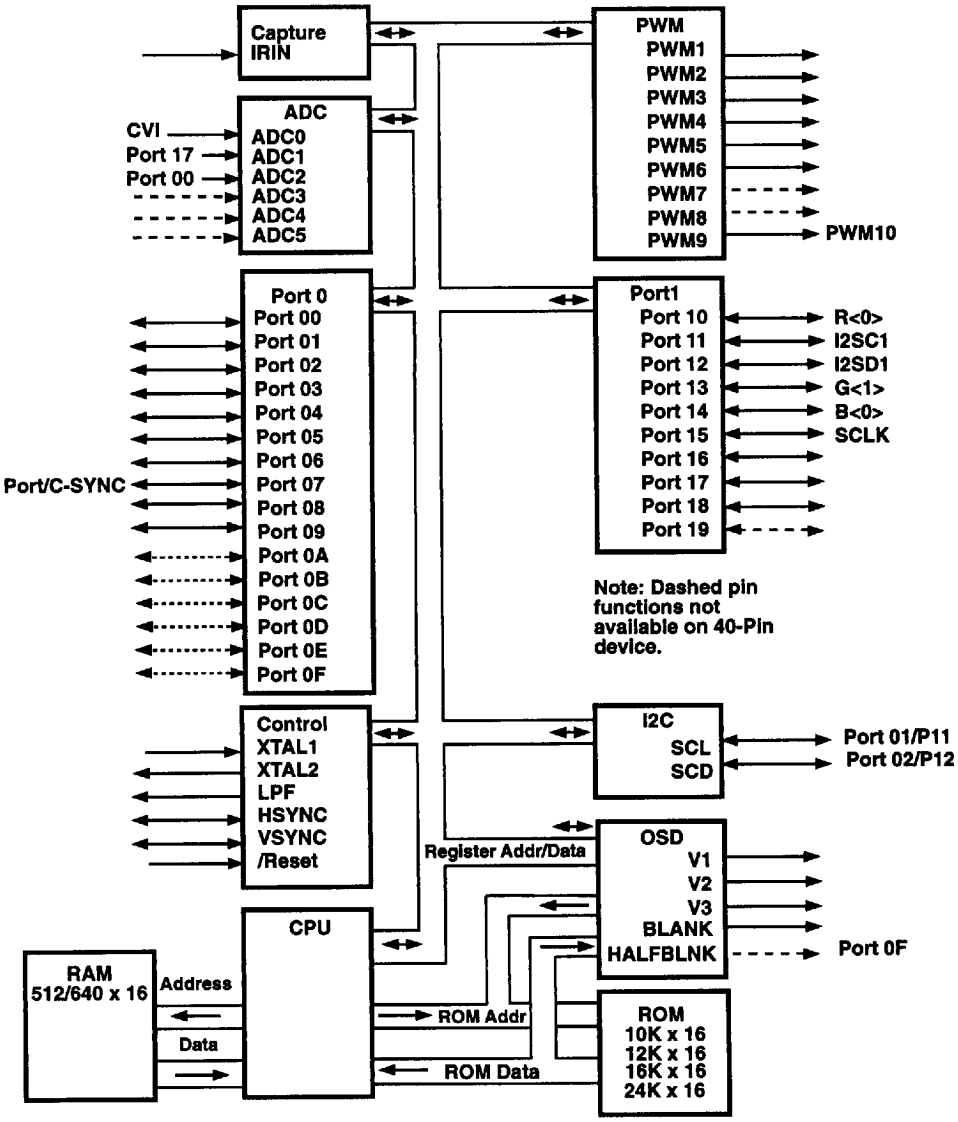


Figure 1. Z89300 Functional Block Diagram

PIN DESCRIPTION

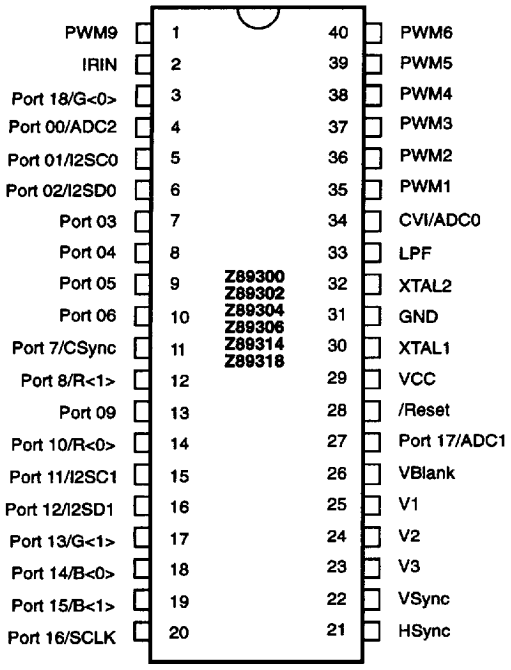


Figure 2. Z89300/02/06 40-Pin DIP

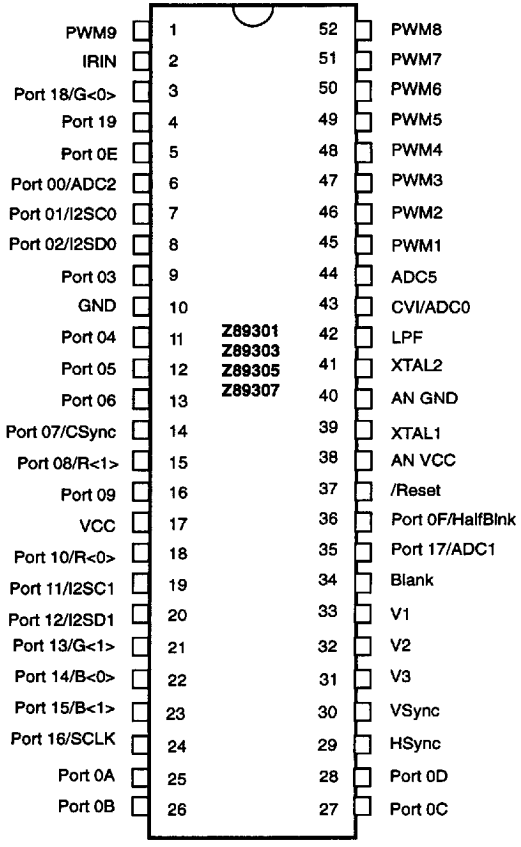


Figure 3. Z89301/03/07 52-Pin DIP

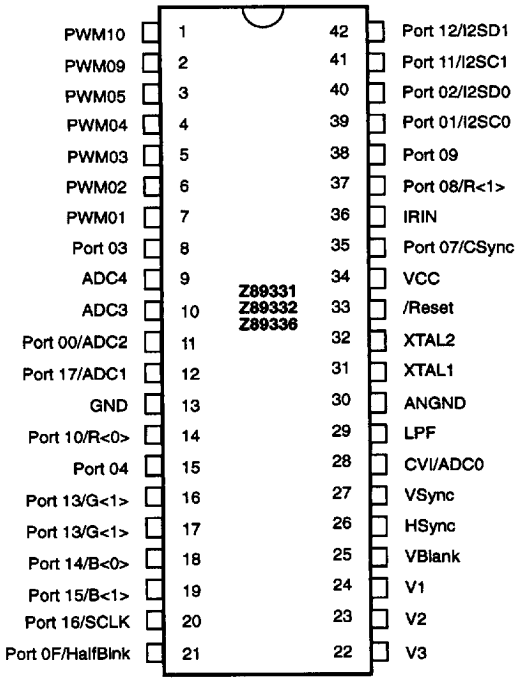


Figure 4. Z89332/336 42-Pin DIP

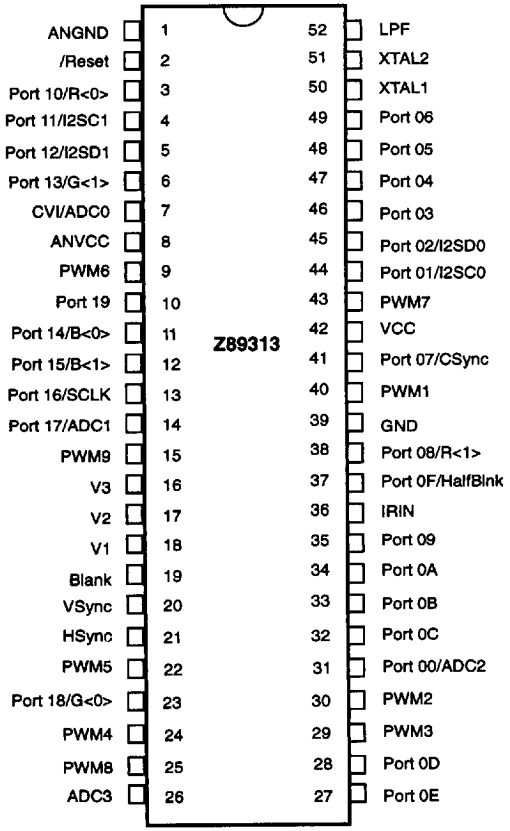


Figure 5. Z89313 52-Pin DIP

PIN IDENTIFICATION

Table 2. Pin Identification

Pin		Package				Configuration	
Name	**Function**	**Z89301/3/5/7 52-pin SDIP**	**Z89313 52-pin SDIP**	**Z89300/02/4/6 14/18 40-pin DIP**	**Z89331/332 /336 42-pin DIP**	**Direction**	**Reset**
VCC	+5 Volts	17,38	8,42	29,–,	34	PWR	–
GND	0 Volts	10,40	1,39	31,–,	13,30	PWR	–
IRIN	Infrared Remote Capture Input	2	36	2	36	I	I
ADC [5:0][1]	4-Bit Analog to Digital Converter input[2].	44,–,–,6, 35,43	–,–,26,31 14,7	–,–, –, 4,27 34	–, 9,10, 11,12,28	AI	I
PWM10, PWM9	14-Bit Pulse Width Modulator Output	–,1	–,15	–,1	1,2	OD	0
PWM[8:1][3]	8-Bit Pulse Width Modulator Output	52,51,50,49, 48,47,46,45	25,43,9,22, 24,29,30,40	–,–.40,39. 38,37,36,35	–,–, –,3,4, 5,6,7	OD	0
Port0[F:0][4]	Bit Programmable Input/Output Ports	36,5,28,27, 26,25,16,15, 14,13,12,11, 9,8,7,6	37,27,28,32, 33,34,35,38, 41,49,48,47, 46,45,44,31,	–,–,–,–,–,–, 13,12,11, 10,9,8,7, 6,5,4	21,–,–,–, –,–,38,37, 35,–,–,15, 8,40,39,11	B	I
Port1[9:0][5]	Bit Programmable Input/Output Ports	4,3,35,24, 23,22,21, 20,19,18	10,23,14, 13,12,11, 6,5,4,3	–,3,27, 20,19,18, 17,16,15, 14	–,16,12, 20,19,18, 17,42,41, 14	B	I
SCL[6]	I^2C Clock I/O	7 or 19	44 or 4	5 or 15	39 or 41	BOD	
SCD[7]	I^2C Data I/O	8 or 20	45 or 5	6 or 16	40 or 42	BOD	
XTAL1	Crystal oscillator input	39	50	30	31	AI	I
XTAL2	Crystal oscillator output	41	51	32	32	AO	0
LPF	LOOP FILTER	42	52	33	29	AB	0
HSYNC	H_SYNC	29	21	21	26	B	I
VSYNC	V_SYNC	30	20	22	27	B	I
/Reset	Device Reset	37	2	28	33	I	I
V[3:1]	OSD Video Output. Typically Drive B, G and R Outputs.	31,32,33	16,17,18	23,24,25	22,23,24	0	0
Blank	OSD Blank Output	34	19	26	25	0	0
HalfBlank[8]	OSD Half Blank Output	36	37	–	21	0	
RGB digital outputs[9]	R[1:0], G[1:0] and B[1:0] Outputs of the RGB Matrix	23,22,21, 20,19,18	12,11,6,5, 4,3	19,18,17,[11] 16,15,14	37,14,17, 16,19,18	0	
SCLK[10,11]	Internal Processor SCLK	24	13	20	20	0	
SCLK[11]	Internal Processor SCLK	–	–	–	L1	0	0
/IE	Data Strobe	–	–	–	K1	0	0
R/W	Read/Write	–	–	–	J3	0	0
EA[2:0]	External Registers Address Bus	–	–	–	L2,K3,H1	0	0

Notes:

1 ADC1 input pin is shared with Port 17, ADC2 input pin is shared with Port 00. ADC3 and ADC4 are not available on 40-Pin DIP version.
2 ADC0 and ADC4 have a clamp circuit that facilitates Composite Video input
3. PWM[8,7] is not available on the 40-Pin DIP version.
4 Port 0 [F.A] is not available on the 40-Pin DIP version
5 Port 19 is not available on the 40-Pin DIP version
6 SCL I/O pin is shared with Port 01 or Port 11
7. SCD I/O pin is shared with Port 02 or Port 12
8 HalfBlank output is a function shared with Port 0F HalfBlank output is not available on the 40-Pin DIP version
9. Digital RGB outputs and the internal SCLK are shared with Port 1 [5:0]
10. Internal processor SCLK is shared with Port 16
11 Not available on Z89314

GENERAL DESCRIPTION

The Z89300 Digital Television Controller is an application specific controller designed to provide compete audio and video control of television receivers and video recorders, and advanced on-screen display facilities.

System Description

Table 1 shows a typical application of the Z89300 Digital Television Controller as an embedded controller in a television receiver. It provides the ability to decode closed caption transmissions and display characters on the screen. Analog and digital control circuits can be manipulated. Keypad and infrared signals can be monitored directly. The Z89300 can also receive and provide vertical and horizontal synchronization signals.

In a typical system, normal transmission is received and demodulated, the CRT display is controlled by the signals received from the color decoder and deflection unit. In order to display characters generated by the Z89300, a video multiplexor must be provided which enables the CRT display's RGB signals and synchronization to be controlled by the video outputs from the processor. When the controller needs to display a character on the screen, the multiplexor is switched and the processor's video signals appear on the display.

The analog composite video signal is fed directly to the analog to digital converter on the chip, which is then decoded to extract the closed caption text embedded in the video signal. The characters received are generated as video signals and are then passed to the display.

When a detectable composite video signal is received the deflection unit extracts the horizontal and vertical synchronization signals and passes them to the CRT deflection plates as well as to the Z89300. The controller uses these signals to align its video signals with those of the normal display. In the case where the composite video signal is not present, video synchronization is able to be provided by the controller. In this case, the SYNC signal pins are set to be outputs and they are then fed to the deflection unit, which then controls the display. The SYNC generators can be configured to provide either H-SYNC and V-SYNC, or H-FLYBACK and V-FLYBACK.

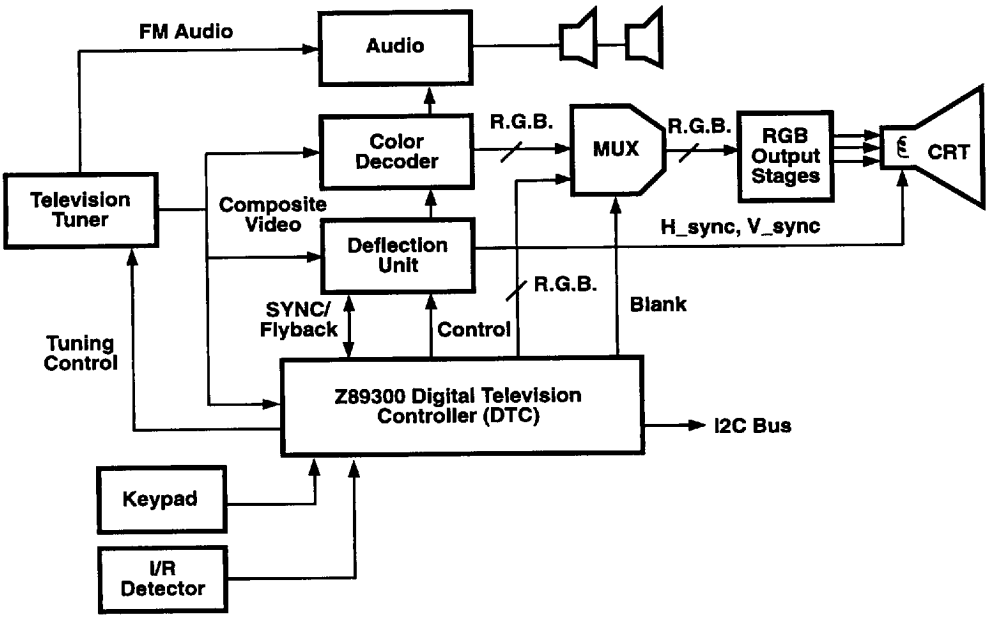


Figure 6. Z89300 Digital Television Controller System Application

System Description (Continued)

Analog functions such as volume and color controls can be controlled by the pulse width modulated outputs from the Z89300. Other digital controls such as channel fine tuning can be controlled through the serial I²C bus.

An infrared remote control receiver can be directly decoded through the capture register, and keypad input can be scanned by directly controlling I/0 pins as keyscan ports.

The processor clock is provided by referencing an internal phase locked loop to an external 32.768 kHz crystal oscillator, which enables EMI emissions from the clock circuitry to be minimized. The internal system clock frequency can be software selected to be up to 12.059 MHz in normal operation or 32.768 kHz in low power mode. The Z89300 can also be placed in STOP mode, suspending processor clocking for power down suspension of operation.

Program, display and character graphics memories are on the chip, eliminating the need for any external memory components. Characters can be displayed as two or three times normal size. Smoothing and fringing circuits are provided to enhance display appearance.

The device is available in a one-time-programmable version as well as a 12K, 16K and 24K masked ROM sizes and is available in 40 and 52-pin DIP packages

FUNCTIONAL DESCRIPTION

Core Processor

The processor core is a high-performance RISC processor.

The powerful 12 MHz Z89C00 RISC processor core allows the user to control the on-board peripheral functions and registers using the standard processor instruction set.

The Z89300 controller processor core is a Z89C00 high performance 16-bit RISC processor optimized for data processing and transfer. 16-bit peripheral registers are programmed to control the operation of the peripheral devices. Two banks of 256 words each of RAM in the processor core can be used for video character sequence storage. Program and character graphics are stored in the PROM.

External Registers

The C00 module is capable of directly accessing up to eight external registers using only the three external register address signals that are normally available. In this implementation, two user signals are combined with the register address signals to provide the ability to address four banks of eight registers each. The most speed critical registers are located together in bank 3. In this document all external registers will be referred to as follows:

RX(Y)<Z>;
where - X is a register number within a register bank;
Y is a bank number;
Z is a bit field number

The user can select a register by setting the user bits to define the bank that the register is in and then specifying the address of the register on the external register address bus.

The external registers reside on the chip and are used to control the operation of all of the peripheral modules of the device. By reading or writing to the fields in the external registers the user can interact with the peripheral devices of the chip.

Interrupt Control

The Z89C00 core has three external interrupt signals that are used to provide interrupt signalling from the Z89300 peripheral modules to the core. In order to provide handling of all four of the device's interrupt sources, that is, horizontal sync (H-SYNC), vertical sync (V-SYNC) and the two timers (1s/CAP), the latter interrupt source is treated as a vectored interrupt where the vector is a bit in a register that selects one of the two timers. The more critical synchronization interrupts are non-vectored.

Interrupt priorities are programmable and each interrupt can be masked by setting fields in the external registers.

The timer interrupts are wire ORed to a single interrupt input. When a timer generates an interrupt it sets the condition of the interrupt vector flag depending on which timer initiated the interrupt request. When the processor is ready to service the interrupt request, it reads the vector bit and executes the appropriate service routine.

When the Z89300 receives an interrupt request from one of the non-vectored interrupt sources it directly executes the interrupt service routine for that source.

Programmable Read Only Memory

The programmable ROM is designed to provide storage for both program memory PROGRAM and character set graphics pixel arrays (CGROM). The address boundaries between these applications is dependent on the storage required for character graphics.

The program ROM section can in theory be accessed anywhere in the addressable ROM space. However, since CGROM usually start at location 0000h, PROGRAM will reside in the higher address locations. The maximum available ROM space for program memory depends on the ROM reserved for CGROM for an application and the ROM size of the device selected. Memory accesses can be considered to be PROGRAM accesses when the ROM address is being provided by the processor ROM address bus.

The Z89300 ROM is either 10K, 12K, 16K or 24K words, depending on the part selected. The first byte of ROM is located at address 0000h, and is mapped as shown in Table 3.

Table 3. PROM Addressing

ROM Size (Words)	Low Address	High Address
12K	000h	2FFFh
16K	000h	3FFFh
24K	000h	5FFFh

The address multiplexor can be selected so that either the processor external address bus or the character registers provide the physical ROM address. For PROGRAM access the processor external address bus should be selected, otherwise the access is to CGROM space.

Clocks and Control

The Z89300 has two internal 12 MHz VCOs (PVCO - primary VCO &SVCO - Secondary - VCO) that are referenced to a 32 kHz internal oscillator to provide the system clock (SCLK). SCLK is generated internally by dividing the frequency of an appropriate oscillator (PVCO or SVCO) by 2. The frequency of the SCLK after POR is 12.058 MHz. In SLEEP mode the controller uses the 32 kHz clock for the system clock to reduce power consumption. The processor can be suspended by placing it into STOP mode when main power is not available for minimal power consumption.

An external crystal controls the internal 32 kHz oscillator, and is used as the clock source for the internal 24 MHz phase locked loop. The PLL provides the internal 12 MHz system clock for processor operation.

On-Screen Display

The extensive character attributes can be controlled in two modes by the on-screen display controller: character control mode for maximum display control flexibility and closed caption mode for optimum display of closed caption text.

Character control mode provides access to the full set of attribute controls. Each word of RAM specifies a single displayed character and basic character attributes, allowing the modification of attributes on a character-by-character basis. The insertion of control characters allows control of other character attributes.

The fully customizable 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes, including underlining, italics and blinking, eight foreground and background colors, character position offset delay, and background transparency. The 16-bit display character representation allows the modification of some key attributes on a character by character basis. A character's pixel array is stored as a 16,18 or 20 word representation in Character Graphics ROM (CGROM). The ROM contents are referenced by a 16-bit word stored in video RAM (VRAM) defining the character type and its key attributes.

Additional hardware provides the capability to display two and three times normal size characters. The smoothing logic contained in the on-screen display circuit improves the appearance of larger fonts. Fringing circuitry can be activated to improve the visibility of text by surrounding the character lines with a one pixel border.

RGB outputs provide the direct video signals, and a blanking output is provided to control the video multiplexor. Dot clock and vertical line synchronization is normally obtained from H_FLYBACK and V_FLYBACK, but can be generated by the Z89300 and driven to the external deflection unit through the bi-directional SYNC ports when external video synchronization signals are not present.

Character Generation ROM

The required Character Graphics ROM size is dependent on the number of characters that are stored in memory. CGROM always begins at address 0000h, the first byte of ROM. The CGROM is configured in two banks selectable by setting a control bit. Each bank provides up to 256 characters with 16x16,16x18 or 16x20 pixels matrix. Absolute maximum CGROM size is 9K words (9210 words).

Each character's pixel array is represented as 16 or 18 words of ROM storage,. Each word is 16 bits long. Pixel lines 1 to 16 are mapped sequentially to ROM addresses that are pointed to by the character pointer and a line number offset. In high resolution mode pixel lines 17 and 18 are offset to addresses beginning at the 4K boundary (1000h) for bank0 . Bank1 is mapped into ROM starting from address 1000h. Lines 17 and 18 of bank1 characters are mapped into ROM starting from address 2000h.

The first character in each bank should be a space character. In order to comply with the latter requirement it is recommended that bank0 character to be defined with 16x16 matrix. If the application requires bank0 characters to be in 16x18 pixel format, the first 32 characters of bank1 should be sacrificed and can't be used because line 17 and 18 of the bank0 characters will be mapped in their addresses and first eight characters of bank0 should not have any active dots in lines 17 and 18 in order to comply with the requirement that the first character in bank1 is a space character. For 16x20 format 32 characters need to be sacrificed.

In case, only bank0 of CGROM is used, there is no limitations on characters definition.

The CGROM data addressed by the contents of the character register is latched into the CGROM capture register. This contents of this register will contain a sequence of bits that represent whether the pixels on the pixel line currently being accessed for that character are on or off. This representation can be modified by the character multiplier to be two or three times normal character size by duplicating each bit in the word and expanding the representation to two or three of the character multiplier registers.

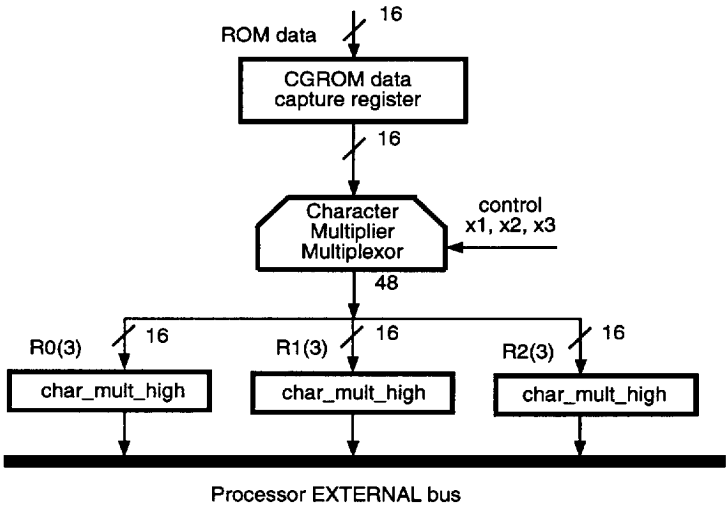


Figure 7. Character Multiplier

Character Multiplier Multiplexor

The character multiplier multiplexor can be controlled to double or triple the size of the pixel line presented to it from the CGROM capture register. It does not perform a numerical multiplication. The bits of the word contained in the capture register are duplicated to enlarge the character as it would be displayed horizontally on the screen. A model of the operation of the character multiplier multiplexor is shown below:

Capture Register Contents	abcdefghijklmnop	abcdefghijklmnop	abcdefghijklmnop
	char_mult_high	char_mult_mid	char_mult_low
x1 operation			abcdefghijklmnop
x2 operation	aabbccddeeffgghh	iijjkkllmmnnoopp	
x3 operation	aaabbbcccdddeeef	ffgggghhhiiijjjkk	kllllmmmnnnooopppp

Tuner Control

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices such as digital channel tuning adjustment may be accessed through the industry standard I^2C port.

Voltage synthesis tuning systems are supported by 14-bit PWM (PWM9/10).

Video and Sound Attribute Control

Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports and one 14-bit pulse width modulated port[1].

Two 14-bit and up to eight 8-bit pulse width modulated are available to provide PWM control of analog signal levels such as volume or color.

Vertical Blank Interval Data Capture

Closed caption text can be decoded directly from the composite video signal with the assistance of the processor's digital signal processing capabilities and displayed on the screen. The character representation in this mode allows for simple attribute control through the insertion of control characters, and each word of RAM specifies two displayed characters.

The 4-bit flash A/D converter provides the ability to directly receive the composite video signal and process the closed caption text embedded in the signal. Signal processing can be applied directly to the signal to improve decoder performance.

I/O Ports

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register.

Up to[2] 26 configurable I/O pins are general-purpose pins that can be utilized to provide functions such as serial data I/0, LED control, key scanning, power control and monitoring and I^2C serial data communications.

Notes:

1. All nine PWM ports are only available in the 52-pin package. In the 40-pin package only six 8-bit and one 14-bit PWM output pins are available
2. The 52-pin device has one 10-bit port and one 16-bit port The 40-pin device has one 10-bit port and one 9-bit port.
3. The 42-pin device has two 14-bit PWMs and five 8-bit PWMs.

REGISTERS

The register file of the Z893xx is organized in four banks selectable by writing bits 5 and 6 ("bank switch" bits) in Status Register of the Z89C00. All registers are mapped into an external register space of the Z89C00 RISC core and each bank consists of 8 registers. Status register is available for reading/writing any time. In order to access the register file, the appropriate bank of registers should be switched on. It is responsibility of the S/W to keep track on which register bank is accessible at any time.

Table 4. Bank Switching

Bank	Status Reg.	Bank Functionality
Bank 0	xxxx xxxx x00x xxxx b	I/O ports, I2C interface, PLL frequency, PWM9, PWM10- 14-bit
Bank 1	xxxx xxxx x01x xxxx b	Control registers
Bank 2	xxxx xxxx x10x xxxx b	PWM1..PWM8-8-bit
Bank 3	xxxx xxxx x11x xxxx b	OSD, palette control

Bank 0 (I/O Ports, I2C Interface, PLL Frequency, PWM9)

Table 5. Register0 - R0(0) PWM9 Data Register

Reg field	Bit position	R	W	Data	Description
Port/PWM	f---------------	R	W	1 0	Output port mode Output PWM mode (push-pull)
Port_data	-e--------------	R	W	x	Output data in Port mode
PWM_data	--dcba9876543210	R	W	xxx	Output data in PWM mode

Port/PWM bit defines the mode of the PWM9 output. When set to a "1" the PWM9 output monitors the data specified by the Port_data field. Otherwise the PWM_data field defines the waveform on the PWM9 pin.

Table 6. Register1 - R1(0) PWM10 Data Register

Reg field	Bit position	R	W	Data	Description
Port/PWM	f---------------	R	W	1 0	Output port mode Output PWM mode (push-pull)
Port_data	-e--------------	R	W	x	Output data in Port mode
PWM_data	--dcba9876543210	R	W	xxx	Output data in PWM mode

Table 7. Register2 - R2(0) PLL Frequency Data Register

Reg field	Bit position	R	W	Data	Description
Port/PWM	fedcba98--------	R	W		Return"0" No effect
PLL_data	--------76543210	R	W	xx	PLL divider = 256 + xx

The VCO, DOT and SCLK frequency are defined as

Fvco = Fdot = Fsclk = 32 kHz x (256 + PLLdata)

Upon POR the PLL frequency data register is preset to %70, which corresponds to the VCO frequency of 12.058 MHz.

REGISTERS (Continued)

Table 8. Register3 - R3 (0) I2C Interface Register

Reg field	Bit position	R	W	Data	Description
Command	fedc----------	R			Return"0"
			W	%DD	See footnote below the Table
Reset	----b----------	R			Return "0"
			W	1	Reset the I2C interface
				0	No effect
HI/LO_ Speed	-----a----------	R	W	1	High speed (400 kHz) - implemented in Rev. BA
				0	Low Speed (100 kHz)
Slave_ mode	------9---------	R		1	Slave mode
			W	0	Master mode
					No effect
Busy	-------8--------	R		1	I2C interface is busy
			W	0	I2C interface is idle
					No effect
Data	--------76543210	R		xx	Received data
			W	xx	Data to be sent

Master Mode

0000 - Send start bit followed by address byte <Data>
0010 - Send data byte specified in <Data>
0100 - Send <7> as an Ack to Slave after Data byte was received **IN READ FRAME** and receive next Data byte.
0110 - Send <7> as an Ack to Slave, do nothing
1001 - Set Slave address defined in <Data> (BE PREPARED FOR SLAVE MODE)
1100 - Receive Ack from Slave after Address byte was transmitted IN READ FRAME If Ack=0, receive Data, else (Ack=1) do nothing.
1110 - Send stop bit
0011,0101,0111,10xx,1101,1111 - RESERVED COMBINATIONS (SHOULD NOT BE USED).

Slave Mode

0010 - Send <Data> **IN READ FRAME** then latch Master's Ack
0100 - Send <7> = 0 as an Ack **IN WRITE FRAME**.
1110 - Send <7> -1 as an Nak **IN WRITE FRAME** OR Send <7> as an Ack **IN READ FRAME** If <7>=0, "Send <Data>" **IN READ FRAME** command should be executed next, else (<7>!=0) release the bus.
1001 - Set Slave address defined in <Data>
ALL THE RESET COMBINATIONS ARE RESERVED AND SHOULD NOT BE USED.

The received data is available for reading only when the "busy" bit is reset to "0". Upon POR the speed of the I2C interface is set to "low".

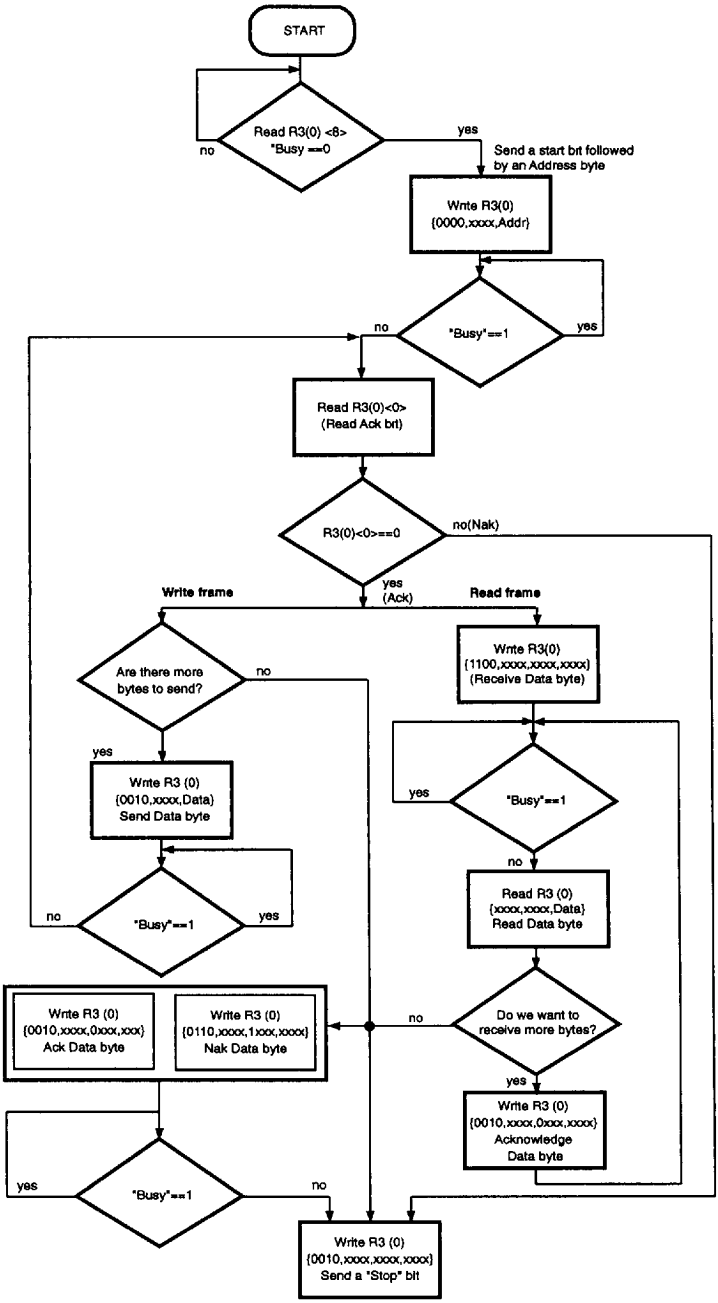


Figure 8. Master Mode

REGISTERS (Continued)

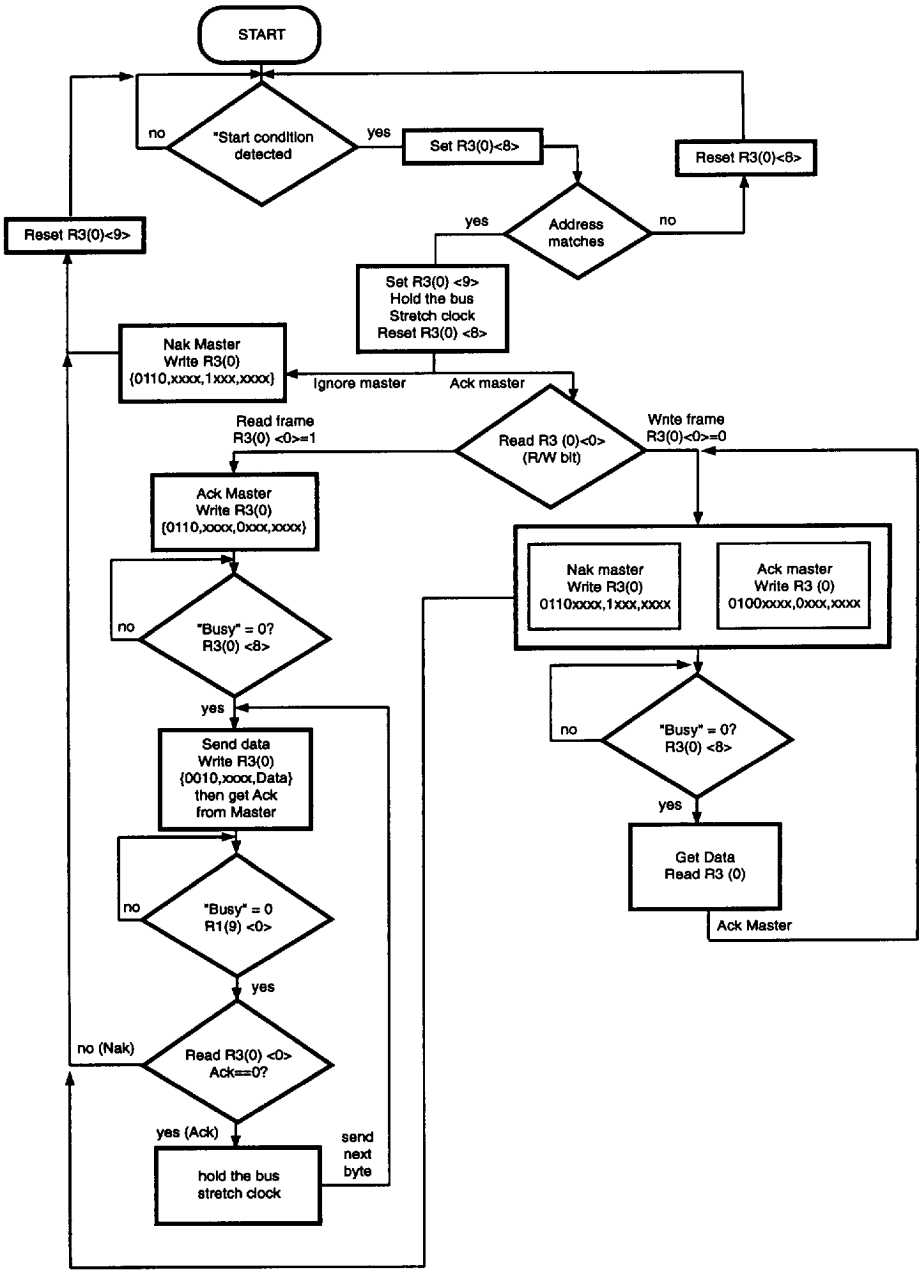


Figure 9. Slave Mode

Table 9. Register4 - R4(0) Port 0 Data Register

Reg field	Bit position	R	W	Data	Description
Port_data	fedcba9876543210	R		xxxx	If port is configured in input mode - the input data on the port pins If Port is configured in Output mode - the data actually written to the port Data
			W	xxxx	

Table 10. Register5 - R5 (0) Port 1 Data Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba----------	R	W		Return "0" No effect
Port_data	------9876543210	R		xxxx	If port is configured in input mode - the input data on the prot pins If Port is configured in Output mode - the data actually written to the port Data
			W	xxxx	

Table 11. Register6 - R6(0) Port 0 Direction Register

Reg field	Bit position	R	W	Data	Description
Port_ direction	fedcba9876543210	R	W	xxxx	1 Input mode for corresponding bit 0 Output mode for corresponding bit

REGISTERS (Continued)

Table 12. Register 7 - R7(0) Port 1 Direction Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba----------	R	W		Return "0" No effect
Port_ direction	------9876543210	R	W	xxxx	1 Input mode for corresponding bit 0 Output mode for corresponding bit

Bank 1 (Control Registers)

Table 13. Register0 - R0(1) Clamp Position Register

Reg field	Bit position	R	W	Data	Description
Disable_clamp_1	f---------------	R	W	1 0	ADC0 Clamp generation is disabled ADC0 Clamp generation is enabled
Disable_clamp_2	-e--------------	R	W	1 0	ADC5 Clamp generation is disabled ADC5 Clamp generation is enabled Implemented in Rev. BA
Reserved	--dcba987-------	R	W		Return "0" No effect
Position	---------6543210	R	W	xx	Position of clamp pulse (from leading edge of the H-FLYBACK)

Upon POR both disable_clamp bits are set to a "1".

The clamp pulse will be generated if it is Enabled bit (bit <f>) and the SCLK frequency was switched "back" to PVCO (SVCO/PVCO flag in R6 (1) should be reset to "0") before the current h-sync regardless whether the SVCO is enabled or disabled. Clamp position is defined by the "Position" field. The width of clamp pulse cannot be modified and is set to 1 µs. The value which can be assigned to the "Position" field should be >%10 and <%ff. The time interval between the leading edge of the H-FLY-BACK and the beginning of the clamp pulse can be calculated from:

$$Tdelay = Position \times \frac{1}{Tsclk} = Position \times 82\ ns$$

Table 14. Register 1 - R1(1) Speed Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba98765432--	R	W		Return"0" No effect
Fast_enable	--------------1-	R	W	1 0	PVCO,SVCO enabled PVCO,SVCO disabled
Fast/Slow	---------------0	R	W	1 0	SCLK is 12 MHz SCLK is 32 kHz

Upon POR, SMR and WDT reset both of these bits are reset to "0", which corresponds to SCLK frequency of 32 kHz.

In order to switch from 32 kHz SCLK to 12 MHz, the following procedure is recommended:

- Setting Fast_enable bit to a "1":
- Waiting for 300 .. 400 ms for 12 MHz PLL to be stabilized (approximately 15000 clock cycles)
- Setting Fast/Slow bit to a "1":

In order to switch from 12 MHz SCLK to 32 kHz, the following procedure is recommended:

- Setting Fast/Slow bit to a "0":
- Waiting for 32 µs for SCLK to be switched (approximately 360 clock cycles);
- Setting Fast_enable bit to a "0".

Table 15. Register2 - R2(1) WDT/STOP Mode Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba98765432--	R	W		Return"0" No effect
WDT_instr	--------------1-	R	W	1 0	Return "0" WDT enable, WDT reset No effect
STOP_instr	---------------0	R	W	1 0	Return "0" STOP instruction No effect

Upon POR, SMR and WDT reset the WDT is disabled. The WDT can be re-enabled only after the PVCO and SVCO are enabled and the part is switched into a Fast mode (SCLK = 12 MHz). Upon switching the part into a Slow mode (SCLK = 32 MHz) the WDT will be suspended and the WDT counter will resume count when the Fast operation will be restored. In the latter case an additional re-initialization of the WDT is not necessary.

REGISTERS (Continued)

Table 16. Register3 - R3(1) Standard Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fe----------	R W			Return"0" No effect
Mask HV-SYNC	--d----------	R	W	1 0	Enable HV output HV input only - POR
Char_Size 16_18/20	---c----------	R	W	1 0	16x20 Char. Matrix 16x16 or 16x18 Char. - POR
Bank0_128/ Bank0_256	----b----------	R	W	1 0 POR	Extended RAM - 128 words Basic Bank - 256 words - POR condition
P07/ ComSYNC	-----a----------	R	W	1 0 POR	Composite SYNC output P07 I/O - POR condition
RGBC/ Port1	------9---------	R	W	1 0 POR	SCLK, R<1:0>,G<1:0>,B<1:0> P16,P08,P10,P13,P18,P15,P14
I2C_port	-------8--------	R	W	1 0	I2C data - P12, I2C clock - P11 I2C data - P02, I2C clock - P01
CGROM blank	--------7-------	R	W	1 0	Bank1 is selected (starts @ % 1000) Bank0 is selected (starts @ % 0000)
HBLANK/ P0f	---------6------	R	W	1 0	HBLANK output P0f output
OSD_ on/off	----------5-----	R	W	1 0	OSD is enabled OSD is disabled
RGB_ polarity	----------4----	R	W	1 0	Negative Positive
Positive/ Negative	----------3---	R	W	1 0	Negative HV-SYNC in output mode Positive HV-SYNC in output mode
SYNC/BLANK	----------2--	R	W	1 0	HV-SYNC outputs HV-SYNC outputs
25/30_Hz and HV polarity	----------10	R	W	 10 00 10 00	Internal mode ONLY (TV Standard) 50 Hz/625 lines support 60 Hz/525 lines support External mode ONLY (HV Polarity) Positive Negative
External/ Internal	----------0	R	W	1 0	External (HV-SYNC in input mode) Internal (HV-SYNC in output mode)

Upon POR the HV-SYNC pins are configured in input mode and OSD_on/off bit is reset to "0".

There are two different bits which define polarity of HV-SYNC signals. Bit <3> defines polarity of the output signals on the pads of the device (it does not effect the internal HV-SYNC signals). Bit <1> defines the polarity of the external HV-SYNC signals and effects the synchronization of the device.

Table 17. Register4 - R4(1) A to D Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcb----------	R	W		Return"0" No effect
ADC_ select	-----a----------	R	W	1 0	ADC4,ADC5 select ADC0, ADC1, ADC2, ADC3 select-POR condition
Reserved	------98---------	R	W		Return"0" No effect
AtoDspeed	-------76--------	R	W	00 01 10 11	Single conversion - POR condition SCLK/4 SCLK/6 SCLK/8
AtoDsource	----------54----	R	W	00 01 10 11	ADC0 (Composite video input) /ADC4 ADC1 (P17) ADC5 ADC2 (P00) ADC3
AtoDdata	------------3210	R	W	%D	AtoD data No effect

There are four different source of A to D converter available in Z89300. Three of them are fixed: ADC0 has a range from 1.5 to 2.0V always connected to Composite Video Input pin of a device and can be clamped to a Ref - voltage (1.5V); ADC1 and ADC2 have a range from 0 to 5V, and are multiplexed with P17 and P00 port pins: ADC3 is available in 52 and 124-pin packages only and has a range from 0 to 5V; ADC4 has a range from 1.5 to 2.0V always connected to Composite Video Input signal and can be clamped to a Ref+ voltage (2.0V).

ADC3 and ADC4 are not available at the same time on 52-pin package. Either one of them can be bonded out according to the customer requirements. Bit <8>of the A to D control register defines the signal source (ADC3/ADC4).

Upon POR the input multiplexor is reset so to select A to D0.
Upon POR A to D control register is not initialized.

REGISTERS (Continued)

Table 18. Register5 - R5(1) Timer Control Register

Reg field	Bit position	R	W	Data	Description
CAPint_r	f----------	R		1 0	Rising edge is captured No rising edge is captured
			W	1 0	Reset flag No effect
CAPint_f	-e---------	R		1 0	Falling edge is captured No falling edge is captured
			W	1 0	Reset flag No effect
Tout_1s	--d--------	R		1 0	Timeout of 1s timer No timeout of 1s timer
			W	1 0	Reset flag No effect
Tout_CAP	---c-------	R		1 0	Timeout of Capture timer No timeout of Capture timer
			W	1 0	Reset flag No effect
Reserved	----ba------	R			Return "0"
			W		No effect
Speed_1s	------98-------	R	W	00 01 10 11	1s 250 ms 62.5 ms 15.625 ms
1s/CAP_int	--------7------	R	W	1 0	int2 source is 1s timer int2 source is Capture timer
CAP_halt	---------6-----	R	W	1 0	Capture timer is halted Capture timer is running
CAP_edge	----------54----	R	W	00 01 10 11	No Capture Capture on rising edge only Capture on falling edge only Capture on both edges
CAP_glitch	------------32--	R	W	00 01 10 11	Glitch filter is disabled <8TSCLK is filtered out <32TSCLK is filtered out <128TSCLK is filtered out
CAP_speed	--------------10	R	W	00 01 10 11	SCLK/4 SCLK/8 SCLK/16 SCLK/32

When capture register is initialized together with a glitch filter, the CAP_speed field should specify the clock of the capture register with the period shorter than the glitch filter for setting defined by the CAP_glitch field.

For example, the following setting is invalid: CAP_glitch = 10b; CAP_speed = 10b;
The example of valid setting is CAP_glitch = 10b; CAP_speed = 11b

Table 19. Register6 - R6(1) Clock Switch Control Register

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba9876------	R	W		Return "0" No effect
SVCO/PVCO	----------5-----	R	W	1 0 1 0	SCLK=SVCO (flag) SCLK=PVCO (flag) Switch SCLK to PVCO No effect
No_switch	----------4----	R	W	1 0	SCLK=PVCO, NO clock switching Clock switching is enabled
H_position	----------3210	R	W	%D	Defines delay of Hint by 4D SCLK cycles

The clock switch control register defines the source of SCLK fed into the Z89C00 core. The block diagram of the clock switch circuit is presented on figure below.

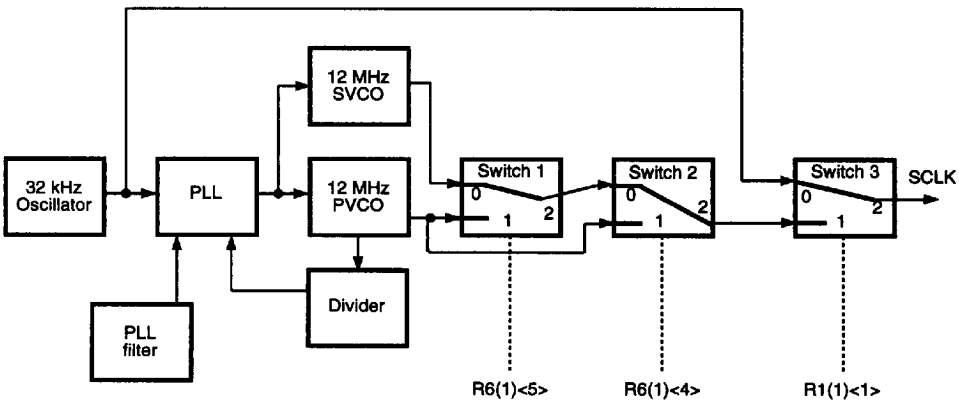


Figure 10. Clock Switch Control Register

Switch1 positioning defines the source of the signal on terminal 0 of switch2. Switch2 is used to override the frequency setting in "no_switch" mode. Whenever "no_switch" mode is set, switch1 continues to switch between PVCO and SVCO. Because of that it is not recommended to switch2 if it is not guaranteed that PVCO signal is fed to terminal0 of switch2. The recommended sequence is as follows:

1. Switch SCLK to PVCO
2. Wait for 2..3 SCLK cycles to ensure that the SCLK is switched
3. Switch R6 (1) <4> to enable/disable "no_switch" mode.

REGISTERS (Continued)

The user of the Z89300 should be aware that clamp pulse (defined in R0 (1)) will be generated only if switch1 is set to a PVCO. It is a S/W responsibility to guarantee correct setting of switch1 before every H-SYNC.

Table 20. Register7 - R7(1) Interrupts/WDT/SMR Control Register

Reg field	Bit position	R	W	Data	Description
Int_priority	fed----------	R	W	x	See a priority table
Int_mask	---cba----------	R	W	1xx 0xx x1x x0x xx1 xx0	int2 is enabled int2 is disabled int1 is enabled int1 is disabled int0 is enabled int0 is disabled
WDTspeed	------98--------	R	W	00 01 10 11	1.83 ms 7.68 ms 31.12 ms 124.8 ms
SMRflag	--------7-------	R W		0 1	No Stop mode Stop mode recovery No effect
SMRpolarity	---------6------	R	W	0 1	OR of all SMR sources NAND of all SMR sources
SMRsource smr5 smr4 smr3 smr2 smr1 smr0	----------543210 ----------5----- ----------4---- ----------3--- ----------2-- ----------1- ----------0	R	W	xx	Bit which corresponds to a "1" in xx binary representation is active p09 p14 p13 p12 p11 p10

The priority of Z89C00 core interrupts is set to int0>int1>int2. These priorities cannot be changed and are embedded in the core. Nevertheless, the Z89300 architecture provides the customer with an ability to change the priority of interrupts be switching interrupts sources between interrupt inputs of the Z89C00 core. The priority table provides the correspondence between H-SYNC, V-SYNC and 1s/CAP interrupts sources and int0, int1 and int2 interrupts inputs of the Z89C00 core.

Table 21. Priority Table

Int_priority field	H-SYNC is switched to	V-SYNC is switched to	1s/CAP is switched to
000	int0	int1	int2
001	int0	Int2	int1
010	int0	Int0	int2
011	int0	Int0	int1
100	int1	int2	int0
101	Int2	int1	int0

Bank 2 (PWM Registers)

Table 22. Register0. Register7 - R0(2)..R7(2) PWM1..8 Registers

Reg field	Bit position	R	W	Data	Description
Reserved	fedcba98--------	R W			Return "0" No effect
PWM_data	--------76543210	R	W	xx	8-bit PWM data

All of the PWMs have open-drain outputs. The outputs of all PWMs are staged by one PVCO clock. The repetition frequency of PWM output signals can be calculated from:

$$Fpwm = \frac{Fpvco}{8(256)} = \frac{12\ MHz}{2048} = 6\ kHz$$

Bank 3 (On-Screen Display [OSD] Registers)

Table 23. Register 0. Register2 - R0(3).R2(3) Character Multiplier Registers (Read Only)

Reg field	CGROM data	Reg addr.	Description
cgrom_x2_hi cgrom_x3_hi	ffeeddccbbaa9988 ffeeddccbbaa9988	R0(3)	High word of double size character R4(3)<6>=0 High word of triple size character R4(3)<6>=1
cgrom_x2_lo cgrom_x3_mid	7766554433221100 aa99988877766655	R1(3)	Low word of double size character R4(3)<6>=0 Middle word of triple size character R4(3)<6>=1
cgrom_x1 cgrom_x3_lo	fedcba9876543210	R2(3)	Single size character R4(3)<6>=0 Low word of triple size character R4(3)<6>=1

Table 24. Register0..Register1-R0(3)..R1(3) Shift Registers (Write Only)

Reg field	CGROM data	Reg addr.	Description
current_reg	fedcba9876543210	R0(3)	current line shift register
next/previous_reg	fedcba9876543210	R1(3)	next/previous line shift register

These register should be loaded with video data once every 16 cycles. The current line register should be loaded first, followed by next/previous register during the next cycle. The next/previous register should be loaded only if smoothing/fringing attributes are activated for the current character. If both of those registers are not loaded, the space character will be displayed. There is no difference between loading "000" h into either of the registers or not loading them at all.

REGISTERS (Continued)

Table 25. Register2 - R2(3) Attributes Register (Write Only)

Reg field	Bit position	Data	Description
Reserved	f---------------	x	No effect
Background color	-edc----------	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	Black Blue Green Light Blue Red Magenta Yellow White
Foreground color NOT PALETTE MODE	----ba9---------	%D	Same as Background mode
Palette selection PALETTE MODE	----ba----------	0 0 0 1 1 0 1 1	Palette0 Palette1 Palette2 Palette3
2nd_underline PALETTE MODE	------9---------	1 0	Underline is active Underline is NOT active
1st_underline	-------8--------	1 0	Underline is active Underline is NOT active
Shift_video	--------7-------	1 0	Video signal is delayed by 8 pixels Standard character positioning
Transparent	---------6------	1 0	Transparent background Background color defined by "background color" field
Blinking	----------5-----	1 0	Blinking character Not blinking character
Italic	-----------4----	1 0	Italic character Not italic character
Color_ delay	------------32--	0 0 0 1 1 0 1 1	Char. color changes instantly Color changes with 4 pixels delay Color changes with 8 pixels delay Color chagnes with 12 pixels delay
Fringing	--------------1-	1 0	Fringing logic is enabled Fringing logic is disabled
Smoothing	---------------0	1 0	Smoothing logic is enabled Smoothing logic is disabled

The attributes register should be loaded 8 cycles after the current line register R0(3) is loaded. Loading of the attributes register enables the OSD logic during next 16 cycles. If attributes register is not loaded there will be no active OSD even though the current line register (R0(3) was loaded.

Table 26. Register3 - R3(3) Attribute_Data Register (Read Only)

Reg field	Bit position	Data	Description
Same as R2(3)			

The data read from the attribute_data register is a combination of attribute fields of the last displayed and control character codes loaded into attributes_data register. The character codes are fetched from Video RAM and should be loaded into attribute_data register R3(3). Bit <f> of attribute_data register (upon reading) indicates whether the last character was a control or a displayed one. The data read from the attribute_data register should be directly loaded into an attribute register R2(3).

Table 27. Register3 - R3(3) Attribute_Data Register (Write Only)

Reg field	Bit position	Data	Description
VRAM_data	fedcba9876543210	xxxx	Character code fetched from VRAM

Loading VRAM data into an attribute_data register will initialize a CGROM access cycle. Four clock cycles after the LD instruction the Z89C00 core will be halted for three clock cycles in order to fetch the data from CGROM and latch it into a CGROM data capture register. After the CGROM data is latched the core operations is resumed. When control character code is loaded into attribute_data register, the CGROM data from address "000" h will be fetched. Therefore it is recommended to place a space character at location "0000" h in CGROM.

REGISTERS (Continued)

Table 28. Register4 - R4(3) OSD Control Register

Reg field	Bit position	R	W	Data	Description
Underline	fe----------	R	W	1x 0x x1 x0	Second underline is active Second underline is inactive First underline is active First underline is inactive
OSD/CCD	--d----------	R	W	1 0	OSD mode CCD mode
CCD_ top/btm	---c----------	R	W	1 0	Blinking character is displayed Blinking character is NOT displayed (hidden)
Italic_shift	-----ba98-------	R	W	x	Defines delay of the character
Blink on/off	---------7------	R	W	1 0	Blinking character is not displayed Blinking character is displayed (hidden)
MPX_bus	---------65-----	R	W	0 0 0 1 1 0 1 1	x1 character size x2 character size x3 character size Reserved
CGROM scan_line	----------43210	R	W	%D	Defines CGROM addressing IN REV.BA also defines italic shift

The Underline field should be set by the firmware during the line/lines of the OSD when the second/first underline is active. The bits will be ANDed with the 2nd/1st underline active fields of data loaded into an attribute register R2(3) allowing character on screen to be underlined.

Italic shift field defines the delay of current video data. Typically it is used to generate italic characters. The firmware decrements by "1" the value of the Italic_shift field for each consecutive line. The video signal will be delayed only for those characters, which have R2(3)<4>("italic") bit set to a "1"

Table 29. Register5 - R5(3) Capture Register

Reg field	Bit position	R	W	Data	Description
Capture_data	fedcba9876543210	R	W	%xxxx	16-bit captured data No effect

Table 30. Register6 - R6(3) Palette Control Register

Reg field	Bit position	R	W	Data	Description
Palette	f---------------	R	W	1 0	Palette mode is active Palette mode is inactive
Underline color	-edc------------	R	W	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	Black Blue Green Light Blue Red Magenta Yellow White
Palette1	----ba9---------	R	W	%D	Same as Underline color
Palette0	-------876------	R	W	%D	Same as Underline color
Palette3	----------543---	R	W	%D	Same as Underline color
Palette2	------------210	R	W	%D	Same as Underline color

Upon POR the palette control register is reset to "0".

REGISTERS (Continued)

Table 31. Register7 - R7(3) Output Palette Control Register

Reg field	Bit position	R	W	Data	Description
Reserved HBLANK_Delay	fedc----------	R W			Return "0" Delay Value No effect %00 - POR Condition
Background_on/off	----b----------	R	W	1 0	Background is on Background is off - POR condition
Background_color	-----a98--------	R	W	%D	Defines the color of the background (the same as the Palette)
Reserved	--------7-------	R W			Return "0" No effect
StarSight palette	---------6------	R	W	0 1 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	Palette is defined by bits <5..0> StarSight palette: Black V1=0; V2=0; V3=0; Blue V1=0; V2=99% V3=99%; Green V1=66%, V2=99%; V3=99%; Grey V1=66%; V2=66%; V3=66%; Red V1=99%; V2=33%; V3=33%; LtYell V1=99%; V2=99%; V3=0; Yellow V1=99%; V2=99%, V3=0; White V1=99%; V2=99%; V3=99%;
Palette_ red (V1)	----------54----	R	W	0 0 0 1 1 0 1 1	66% red 66% red + 33% blue 66% red + 33% green 66% red + 33% blue + 33% green
Palette_ green (V2)	------------32--	R	W	0 0 0 1 1 0 1 1	66% green 66% green + 33% blue 66% green + 33% red 66% green + 33% blue + 33% red
Palette_ blue (V3)	--------------10	R	W	0 0 0 1 1 0 1 1	66% blue 66% blue + 33% green 66%blue + 33% red 66% blue + 33% green + 33% red
Digital_ mode	----------543210	R	W	000000	Outputs V1, V2, V3 correspond to 100% red, green, and blue outputs

Upon POR the Output palette register is set to "0" - digital output.

Note: If bit R7(3)<6> is set to "1", while bits R7(3)<5:0> are reset to a "0". the outputs V1, V2 and V3 of Z89300 will be switched into a "Digital mode".

REGISTER SUMMARY

Table 32. Register Utilization Rev 2.0

BANK	BANK Sub Address	READ Register	WRITE Register	Description
Bank 0	7	dir1		10-bit I/O port 1 direction control
	6	dir0		16-bit I/O port 0 direction control
	5	port1		10-bit I/O port 1
	4	port0		16-bit I/O port 0
	3	i2c_int		I2C interface register
	2	pll_freq		PLL frequency control
	1	pwm_data10		14-bit PWM10 data
	0	pwm_data9		14-bit PWM9 data
Bank 1	7	wdt_smr_ctl		Stop-Mode Recovery/Watch-Dog Timer Control
	6	clock_ctl		Clock control (switch VCO/DOT)
	5	cap_1s_ctl		Counter timers control
	4	atod_ctl		A/D converter control
	3	standard_ctl		Output H/V-sync/blnk control
	2	stop_wdt_ctl		Stop and Watch-Dog Timer Control
	1	sclk_freq		Stop/Sleep/Normal Mode
	0	clamp_pos		Defines position of video clamp pulse
Bank 2	7	pwm_data8		8-Bit PWM 8 data
	6	pwm_data7		8-Bit PWM 7 data
	5	pwm_data6		8-Bit PWM 6 data
	4	pwm_data5		8-Bit PWM 5 data
	3	pwm_data4		8-Bit PWM 4 data
	2	pwm_data3		8-Bit PWM 3 data
	1	pwm_data2		8-Bit PWM 2 data
	0	pwm_data1		8-Bit PWM 1 data
Bank 3	7	output palette		Output palette
	6	palette_color		Display palette color/underline color
	5	capture_data	(no effect)	Capture register data
	4	osd_control		On-Screen Display Control
	3	attribute_data	vram_data	Character attribute/video ram data
	2	ch_x1_lo_x3	cg_attribute	Character mult./char. graphics attribute
	1	lo_x2_mid_x3	cg_nxt_prv	Character mult./next or previous data
	0	hi_x2_hi_x3	cg_current	Character mult./current data

Video RAM Specification (Supported data format in VRAM)

The H/W of the Z893xx supports two different data formats in the VRAM. The first one supports a standard OSD with full set of features (OSD mode). The second format supports reduced features which comply with the recommendations of the FCC on Closed Caption support (CCD mode). In CCD mode the background color of the characters can not be changed and is always preset to a "black".

In OSD mode each character occupies 16-bit word in VRAM. There are two possible character formates defined: a "display" character and a "control" character. The code stored in a "display" character format defines a character code and up to 7 attributes of the character. The "control" character defines up to eight attributes of the next character and is presented on screen as a space character. Combination of "display" and "control" characters allows to generate a versatile OSD.

Table 33. Display Character Format (OSD Mode)

Reg field	Bit position	Data	Description
Control bit	f---------------	1 0	Control character Display character
Background color	-edc------------	000 001 010 011 100 101 110 111	Black Blue Green Light Blue Red Magenta Yellow White
Foreground color (Not palette mode)	----ba9---------	%D	Same as Background_color
Foreground palette (Palette mode)		00x 01x 10x 11x	Palette 0 (defined in R6(3)<8..6> Palette 1 (defined in R6(3)<b..9> Palette 2 (defined in R6(3)<5..3> Palette 3 (defined in R6(3)<2..0>
Second underline (Palette mode)		xx1 xx0	Second underline attribute is active Second underline attribute is inactive
First underline	-------8--------	1 0	First underline attribute is active First underline attribute is inactive
Character code	--------76543210	%DD	Defines the character in CGROM

If background and foreground colors of a character are set to be the same, the character will be displayed as a transparent one.

Table 34. Control Character Format (OSD Mode)

Reg field	Bit position	Data	Description
Control bit	f---------------	1 0	Control character Display character
Reserved	-edcba98--------	x	Reserved - do not effect OSD
Shift_video	--------7-------	1 0	Video signal is delayed by 8 pixels Standard character positioning
Transparernt	---------6------	1 0	Transparent background Background color defined by "background color" field
Blinking	----------5-----	1 0	Blinking character Not blinking character
Italic	-----------4----	1 0	Italic character Not italic character
Color_delay	------------32--	0 0 0 1 1 0 1 1	Character color changes instantly Color changes with 4 pixels delay Color changes with 8 pixels delay Color changes with 12 pixels delay
Fringing	--------------1-	1 0	Fringing logic is enabled Fringing logic is disabled
Smoothing	---------------0	1 0	Smoothing logic is enabled Smoothing logic is disabled

In CCD mode each character occupies 8-bit (one byte) in VRAM. The CCD characters should be mapped into a 16-bit VRAM data field. The H/W supports the compressed placement of the characters in VRAM. Each word in VRAM is represented by HIGH byte and LOW byte. The currently active byte is selected by R4(3)<c>. The format and data representation in both bytes is exactly the same. There are two possible character formats defined: a "display" character and a "control" character. The code stored in a "display" character format defines a character code. The "control" character defines up to seven attributes of the next character and is presented on-screen as a space character. Combination of "display" and "control" characters allows to generate a CCD OSD according to FCC specification.

Table 35. Display Character Format (CCD Mode)

Reg field	Bit position	Data	Description
Control bit	7-------	1 0	Control character Display character
Character code	-6543210	%DD	Defines the character in CGROM.

REGISTER SUMMARY (Continued)

Table 36. Control Character Format (CCD Mode)

Reg field	Bit position	Data	Description
Control bit	7-------	1 0	Control character Display character
Transparernt	-6------	1 0	Transparent background Background color defined by "background color" field
Blinking	--5-----	1 0	Blinking character Not blinking character
Italic	---4----	1 0	Italic character Not italic character
Foreground color	----321-	000 001 010 011 100 101 110 111	Black Blue Green Light blue Red Magenta Yellow White
First underline	-------0	1 0	Underline attribute is active Underline attribute is inactive

By default background color in CCD mode is "black"; foreground and background color, blinking and italic attributes are delayed by 1/2 character, smoothing attribute is always enabled.

A to D and Clamp Circuit Operation (Recommended Practice)

A 4-bit A to D implemented in Z89300 has five multiplexed inputs. Three of them are available in 40-pin package (CVI, ADC1/P17 and ADC2/P00). There are two configurations of 52-pin package with different ADC inputs bonded out: 52-pinN - CVI, ADC1/P17, ADC2/P00 and ADC4 and 52-pinW - CVI, ADC1/P17, ADC2/P00 and ADC3. On 124-pin package all five A to D inputs are bonded out.

The allowed range of the input signals is different for different A to D inputs according to the following table:

Table 37. A to D Inputs Typical Range

Input	Range (V)	Clamping	Typical Application
CVI/ADC0	1.5..2.0	Yes-Ref-	CCD sampling input
ADC1/P17	0 ..5.0	No	AFC input
ADC2/P00	0 ..5.0	No	Key scanning input
ADC3	0 ..5.0	No	Key scanning input
ADC4	0 ..5.0	No	Key scanning input
ADC5	1.5 ..2.0	Yes - Ref+	V-SYNC decoder sampling input

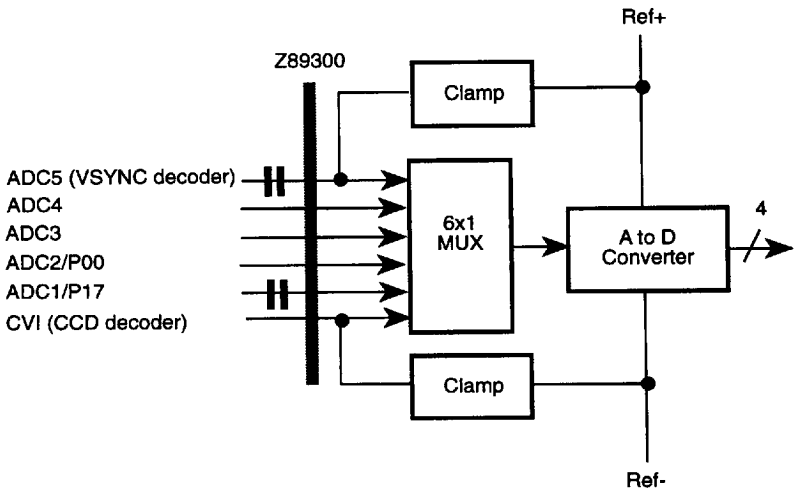


Figure 11. A to D Block Diagram

Internally generated reference voltages define the maximum range of the input signal of the A to D. Nominal values of Ref+ = 2.0V: Ref= 1.5 V @ V_{CC} = 5V for different values of V_{CC} the reference voltages should be pro-rated.

The maximum sampling rate of the A to D converter is 3 MHz. It takes 4 SCLK cycles for the valid data at the output of the A to D to become available. This matter should be taken into consideration especially if application is utilizing a single shot mode.

A to D and Clamp Circuit Operation (Recommended Practice) (Continued)

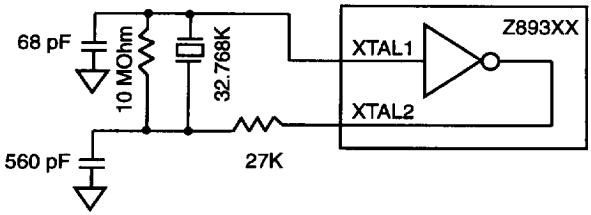


Figure 12. 32K Oscillator Recommended Circuit

V1, V2, V3 Analog Output

Table 38. V_{cc} = 5.25V

VCC=5.25V	Condition	Limit
Output Voltage	bit=11	4.55V ± 0.25V
	bit=10	3.25V ± 0.2V
	bit=01	1.95V ± 0.15V
	bit=00	0.65V ± 0.1V
Settling Time	70% of DC level, 10 pf load	<50 nsec

Table 39. V_{cc} = 4.75V

VCC=5.25V	Condition	Limit
Output Voltage	bit=11	3.90V ± 0.25V
	bit=10	2.90V ± 0.2V
	bit=01	1.90V ± 0.15V
	bit=00	0.1V ± 0.1V
Settling Time	70% of DC level, 10 pf load	<50 nsec

V1, V2, V3 Analog Output (Continued)

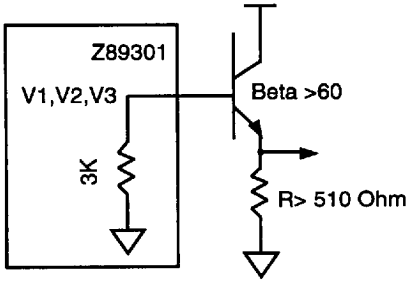


Figure 13. Recommended Circuit

MODULE DESCRIPTIONS

Z89COO Core Processor Module

Memory Organization

The C00 core has access to three types of memory that are of interest here:

1. **Program Read Only Memory (PROGRAM)**
   Size: 12K, 16K or 24K words (16 bytes) depending on device version selected.

2. **External Registers**
   Addressable Size: Four selectable banks of up to eight registers each, providing access to up to 32 register addresses. Registers can be selected for read or write operations. Some registers are only accessible in either read mode or write mode.

3. **Processor RAM**
   Size: Two banks of 256 words of 16 bits each, providing a total of 512 words of RAM on 89314, extra 128 words on all other parts in the range on third bank.

Other memory exists in the form of internal registers in the processor and registers that are not part of the processor's direct memory map.

32K PROGRAM ROM

int0 vector	7FFFH
int1 vector	7FFEH
int2 vector	7FFDH
reset vector	7FFCH

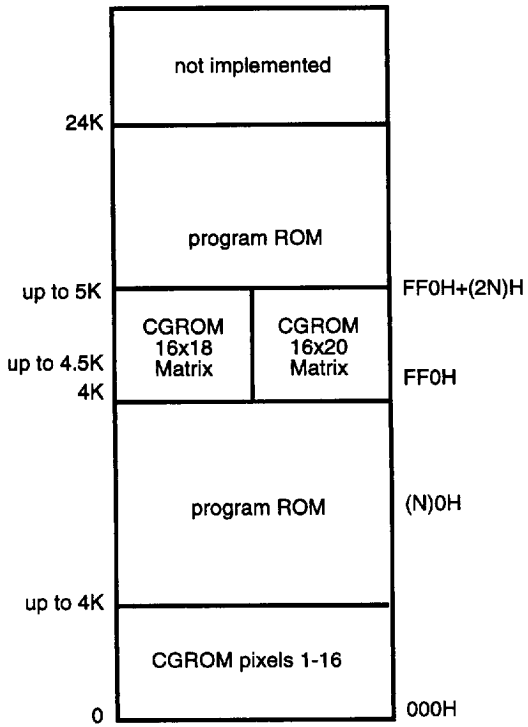


Figure 14. Program Read Only Memory

MODULE DESCRIPTIONS (Continued)

The size of memory used as CGROM depends on the number and resolution of characters stored in memory. 'N' represents the number of characters stored, ranging from 0 to 256. If characters are 16 x 18 or 16 x 20 pixels then the upper region of memory starting at the 4K boundary is used for character storage. If not it can be used as program memory.

Clocking Operation

The processor is able to operate from a number of clock sources.

1. Primary Phase Locked Loop V_{co} source (PVCO)
2. Secondary V_{co} phase-aligned with VSYNC timing (SVCO)
3. 32 kHz oscillator clock (OSC)

In addition the processor clock may be halted temporarily to allow clock selection or ROM accesses to be performed without disrupting normal operation of the processor.

PADS CONFIGURATION

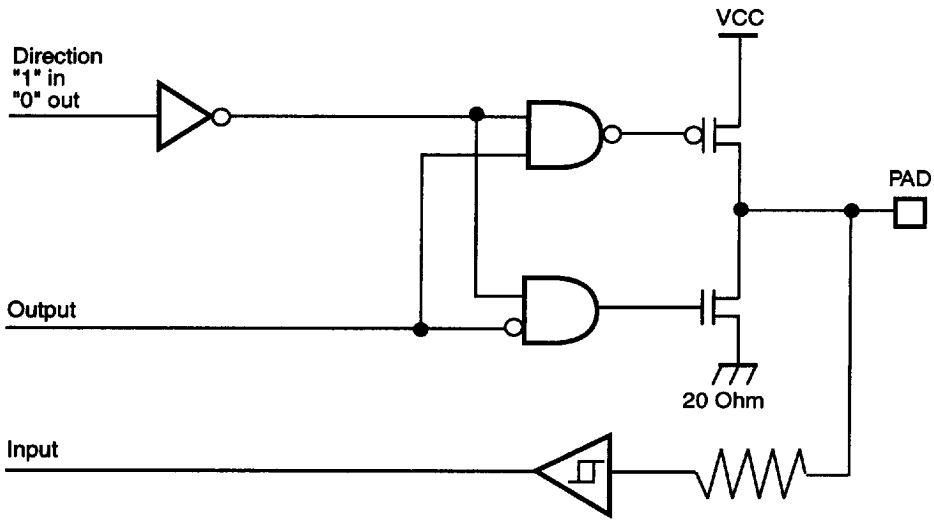


Figure 15. Type1 Bi-directional Port pins (Port 3, Port0f, Port 10, Port 13, Port 16, Port 18, Port 19, H-SYNC and V-SYNC)

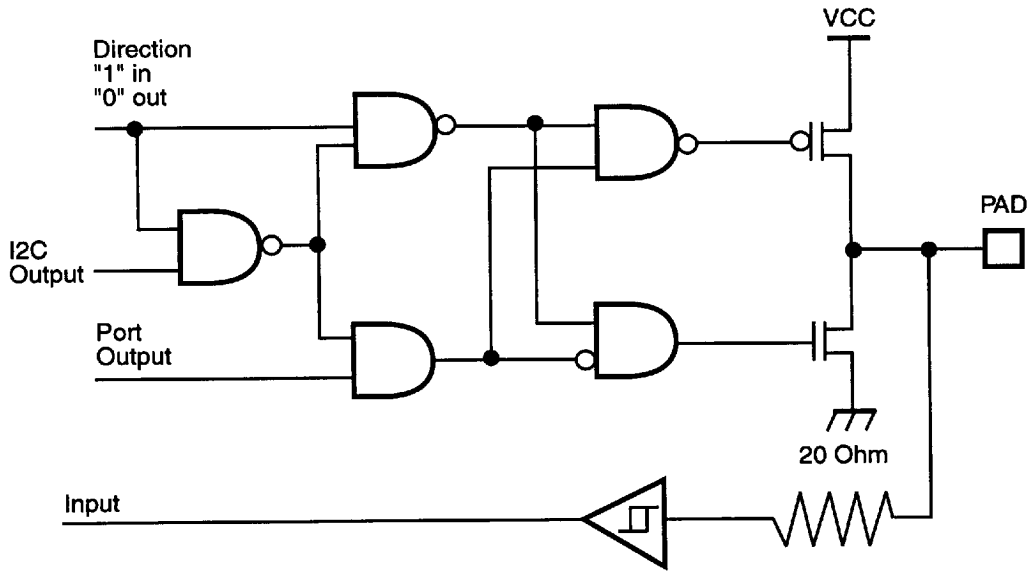


Figure 16. Type2 Bi-directional Port pins multiplexed with I²C port (Port 1, Port 2, and Port 11, Port 12)

PADS CONFIGURATION (Continued)

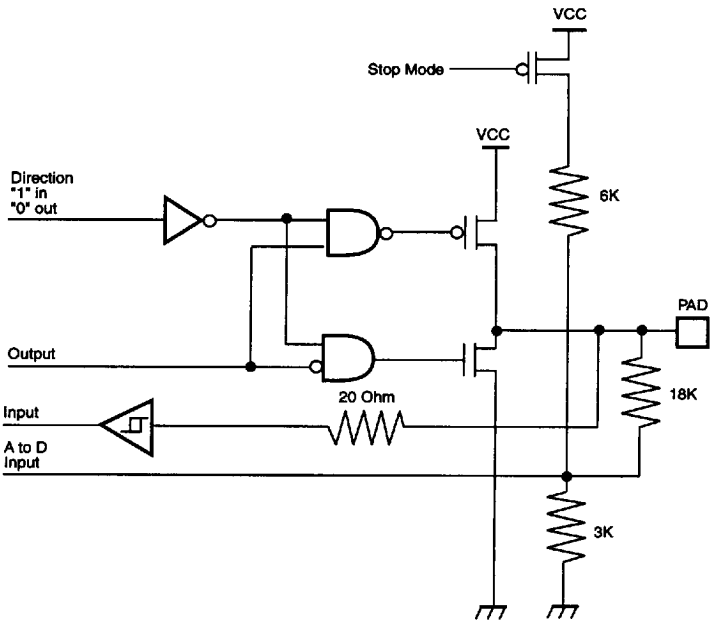


Figure 17. Type3 Bi-Directional Pins Multiplexed with AtoD Inputs (Port 00/AtoD2 and Port 17/AtoD1)

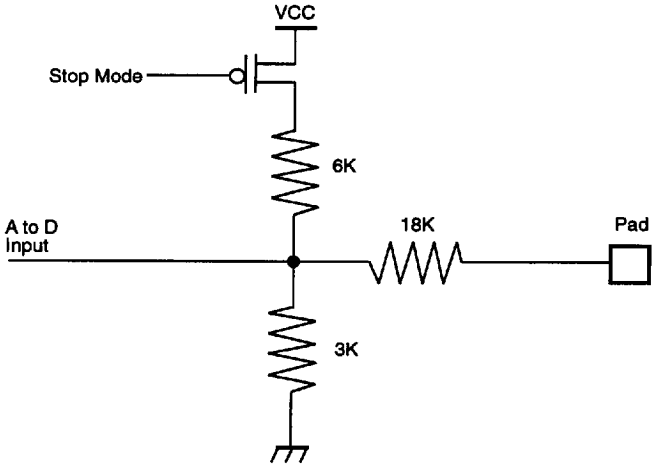


Figure 18. Type4 AtoD Input (AtoD3)

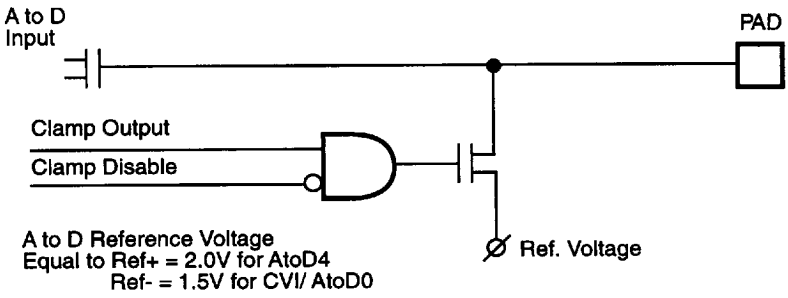


Figure 19. Type5 AtoD Inputs Combined with an Internal Clamp (Composite Video Input/AtoD0 and AtoD4).

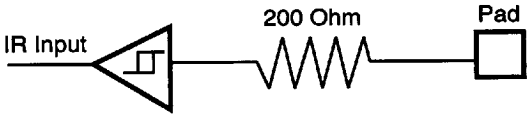


Figure 20. Type6 IR Capture Register Input

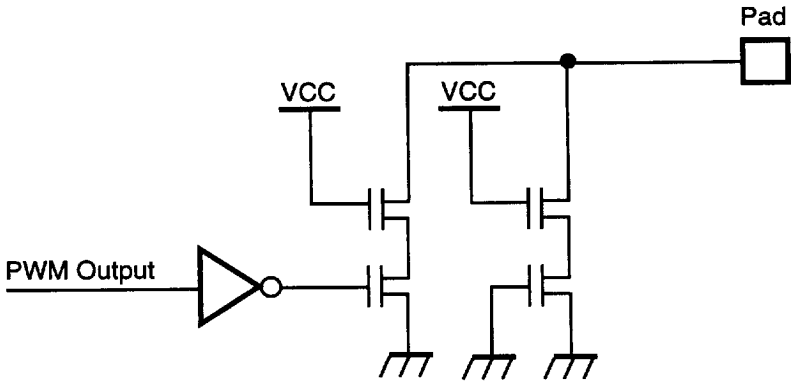


Figure 21. Type7 PWM1, PWM8 Open-Drain Outputs

PADS CONFIGURATION (Continued)

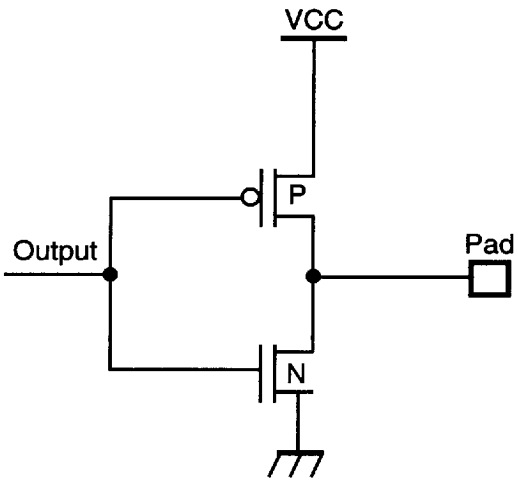


Figure 22. Type8 PWM9 and BLANK outputs; V1, V2, V3 outputs in digital mode

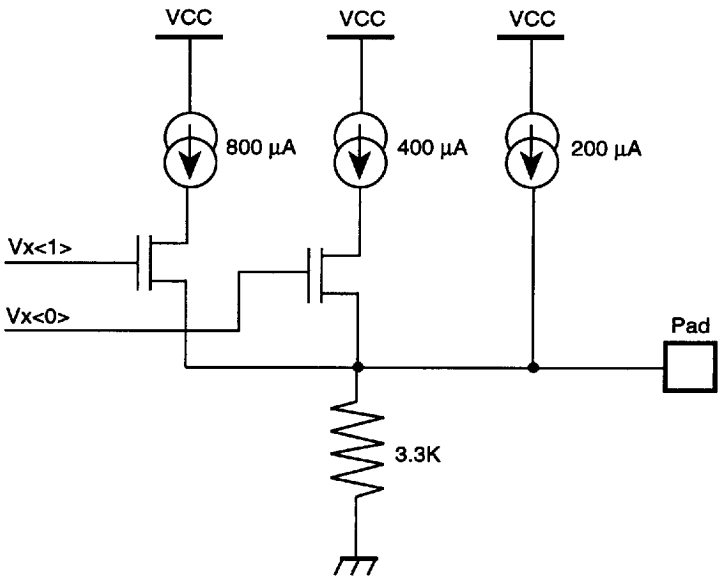


Figure 23. V1, V2 and V3 outputs in analog (palette) mode.

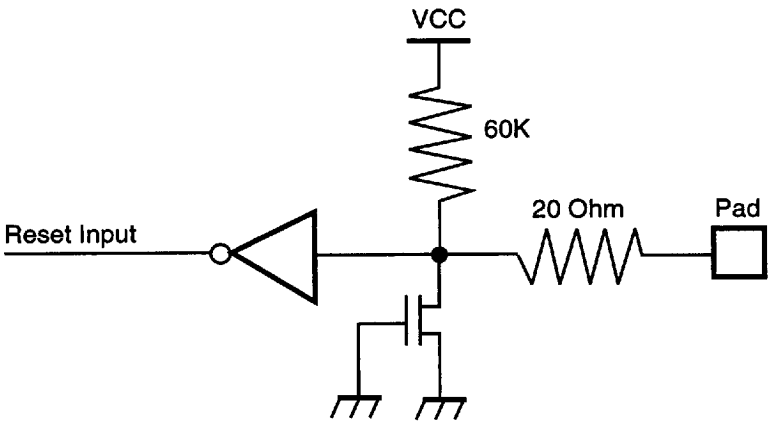


Figure 24. Reset Input

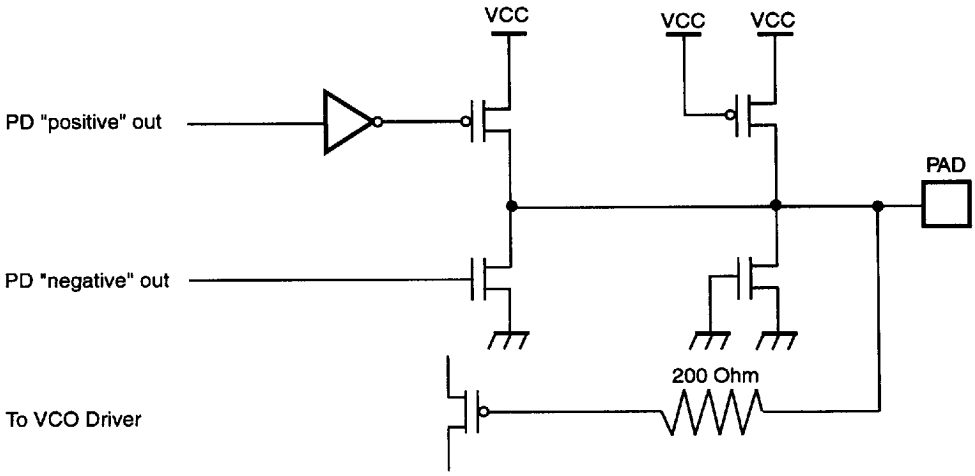


Figure 25. Loop Filter Pin

ABSOLUTE MAXIMUM/MINIMUM RATINGS

Sym	Parameter	Min	Max	Units	Conditions
V_{CC}	Power supply voltage	0	7	V	
V_{ID}	Input voltage	-0.3	V_{CC}+0.3	V	Digital inputs
V_{IA}	Input voltage	-0.3	V_{CC}+0.3	V	Analog inputs (A/D0..A/D4)
V_O	Output voltage	-0.3	V_{CC}+0.3	V	All push-pull digital outputs
V_O	Output voltage	-0.3	V_{CC} +8.0[1]	V	Open-drain PWM outputs (PWM1..PWM8)
I_{OH}	Output current high		-10	mA	one pin
I_{OH}	Output current high		-100	mA	All pins
I_{OL}	Output current low		20	mA	one pin
I_{OL}	Output current low		200	°C	All pins
T_A	Operating Temperature	0	70	°C	
T_A	Storage Temperature	-65	150	°C	

Note:
1. Momentary withstand voltage 16V

DC CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 4.5V to 5.5V; F_{OSC} = 32.768 kHz)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IL}	Input voltage low	0	0.4	0.2 V_{CC}	V	
V_{IH}	Input voltage high	0.6 V_{CC}	3.6	V_{CC}	V	
V_{IH}	Input voltage high	0.75 V_{CC}	4.2		V	Reset pin only
V_{PU}	Maximum pull-up voltage			12	V	For PWM1..PWM8 only
V_{OL}	Output voltage low		0.16	0.4	V	@ I_{OL} = 1 mA
V_{OL}	Output voltage high	V_{CC} -0.9	4.75		V	@ IOL = 0.75 mA
V_{XL}	Input voltage XTAL1 low		1.0	0.3 V_{CC}	V	External clock generator driven
V_{XH}	Input voltage XTAL1 high	0.6 V_{CC}			V	
V_{HY}	Schmitt Hysteresis	0.3	0.5	0.75	V	XTAL1 input pin
I_{IR}	Reset input current		90	150	µA	VRL = 0V
I_{IL}	Input leakage	-3.0	0.01	3.0	µA	@ 0V and V_{CC}
I_{CC}	Supply current		60	100	mA	
I_{CCIE}	Supply current of the OTP		300	700	µA	Sleep mode @ 32 kHz
I_{CC1}	Supply current		100	300	µA	Sleep mode @ 32 kHz
I_{CC2}	Supply current		5	10	µA	Stop mode

AC CHARACTERISTICS

(T_A = 0°C to 70°C; V_{CC}=4.5V to 5.5V; F_{OSC} = 32.768 kHz)

Sym	Parameter	Min	Typ	Max	Units
T_pC	Input clock period	16	32	100	µs
T_RC, T_fC	Clock input Rise and Fall		12		µs
T_DPOR	Power-on reset delay	0.8	1.2		S
T_wRES	Power-on reset minimum			5 TpC	µs
T_DH_S	H-SYNC incoming signal width	5.5	11	12.5	µs
T_DV_S	V-SYNC incoming signal width	0.15	1.0	1.5	ms
T_DE_S	Time delay between leading edge of V-SYNC and H-SYNC in EVEN filed	-12	0	+12	µs
T_DO_S	Time delay between leading edge of V-SYNC and H-SYNC in ODD field	20	32	44	µs
T_wHV_S	H-SYNC/V-SYNC edge width		0.5	2.0	µs

Note:
All timing of the I²C bus interface are defined by related specifications of the I²C bus interface

RECOMMENDATIONS

Reset Circuit

The 32 kHz crystal oscillator of the Z89300 has a typical setting time of 800 ms. The reset will be supplied to the Microprocessor core only if the "reset" pin of the device is held "low" for more than 5 clock cycles. In case of the POR, the external RC circuit should provide a time delay of more than the longest possible setting time of the oscillator.

The typical value of the internal pull-up resistor is 60±20 Kohm.

Assuming that the RC constant of the reset circuit should be >1s, the value of the capacitor can be calculated from:

$$C=\frac{1}{R}=\frac{1}{60x10^{3}}=15x10^{-6}=15.0\ \mu f$$

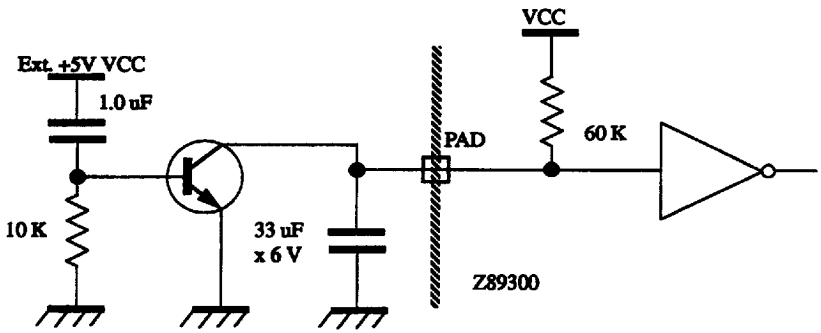


Figure 26. Reset Circuit

Unused/Unbonded Ports

Upon POR all ports are configured as an inputs. It is not recommended to leave inputs floating even though they are not bonded out.

It is good practice to configure unused ports as outputs - both P0f P00 and P19.. P10

HSYNC (HFLYBACK) Recommended Timing

In a standard application using Zilog's ATB there are two S/W processes related to the incoming HSYNC signal:

- OSD Generation
- CCD Data Captioning

The OSD generated by Z89300 is positioned relative to the trailing edge of the incoming HSYNC signal. There is a delay implemented in hardware which allows the customer to adjust positioning of the OSD (H-position field in Register R6 (1)) up to 4.5 µs. The following timing diagram clarifies the H/W requirements.

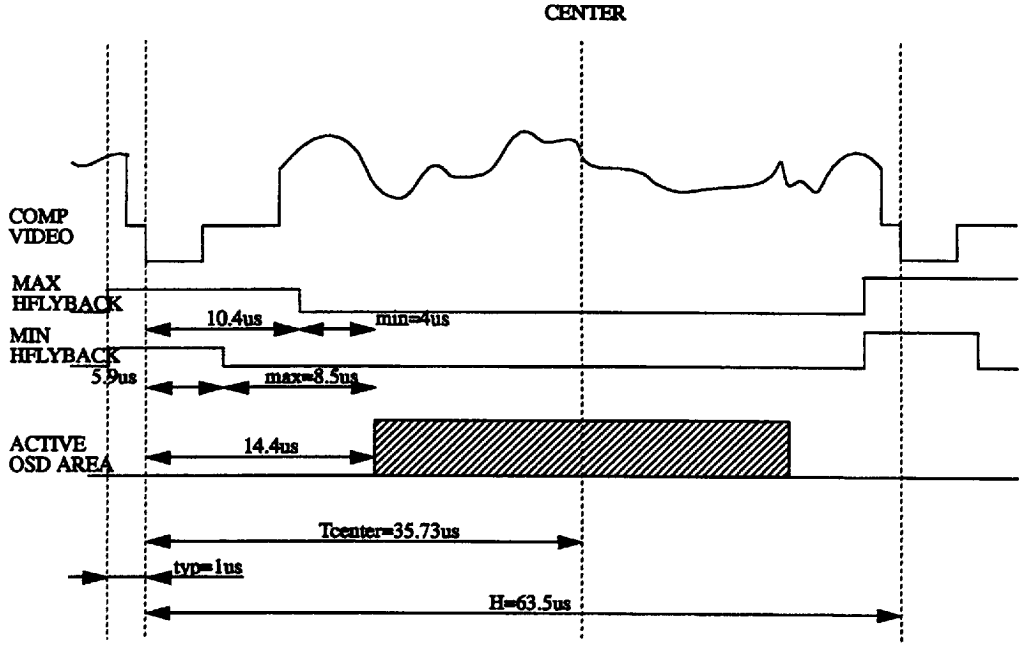


Figure 27. HSYNC Timing Diagram

Time from leading edge of HSYNC to trailing edge of HFLYBACK should be maintained from 5.9 to 10.4 µs in order to ensure centering of the OSD. Assuming the HFLYBACK typically starts 1 µs before leading edge of HSYNC, the width of HFLYBACK should be set to 6.9 µs <Thflb<11.4 µs.

HSYNC (HFLYBACK) Recommended Timing (Continued)

CCD data captioning algorithm utilizes sampling of the Composite Video signal during line 21. In order for the CCD algorithm to recognize CCD burst (seven clock cycles of 503 kHz) certain timing relationships between incoming Composite Video signal and HFLYBACK should be maintained.

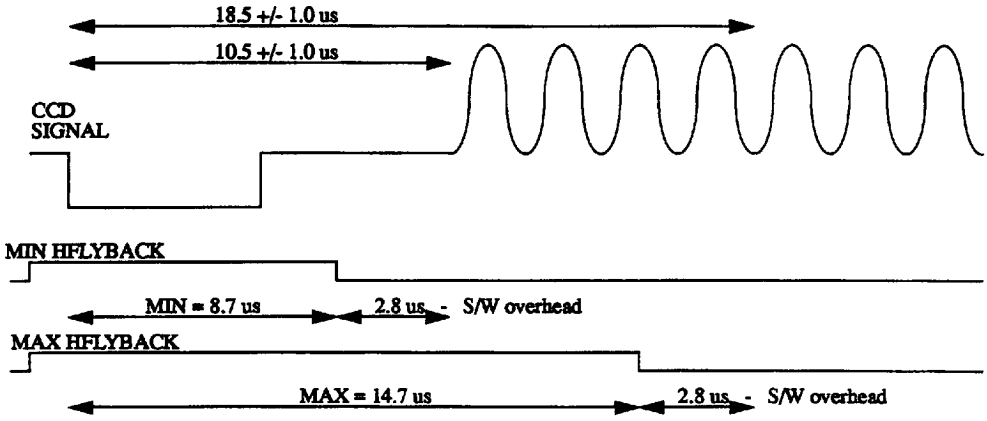


Figure 28. HFLYBACK Timing Diagram

In order to guarantee CCD algorithm performance, the time delay from leading edge of HSYNC to trailing edge of HFLYBACK should be maintained from 8.7 µs to 14.7 µs.

In order to comply with both OSD centering and CCD performance requirements, the time delay of trailing edge of HFLYBACK should be from 8.7 µs to 10.4 µs, which corresponds to HFLYBACK width of 9.7 µs....11.4 µs if leading edge of HFLYBACK is 1.0 µs ahead of leading edge of HSYNC.

Clamp Positioning

The black level of Composite Video signal fed to Z89300 should be set to Ref - voltage of the A to D. In order to shift the DC level of the incoming signal, there is an internal clamp in the Z89300. The clamp pulse should be located during the back porch of the HSYNC.

Clamp position is defined by the "Position" field (bits <6:0>) in Clamp Position register R0(1). The width of clamp pulse cannot be modified and is set to 1 µs. The value which can be assigned to the "Position" field should be >10% and <7%f. The time interval between the leading edge of the H-FLYBACK and the beginning of the clamp pulse can be calculated from:

$$Tdelay = Position \times \frac{1}{Tsclk} = Position \times 82\ ns$$

Because the clamp pulse is generated from the leading edge of the incoming HFLYBACK signal, there are certain constraints imposed on the relative positioning of the leading edge of HFLYBACK relative to leading edge of HSYNC.

By setting the "Position" field of Clamp Position register, the clamp pulse can be positioned at 1.3 µs....10.5 µs after the leading edge of HFLYBACK.

The optimal position of the clamp pulse is 6.5 µs after the leading edge of the HSYNC (in the middle of the back porch interval). Wide setting of "Position" field allows for possible variations in HFLYBACK positioning of up to +4.0 µs....-5.0 µs.

Practical example of registers setting implementation

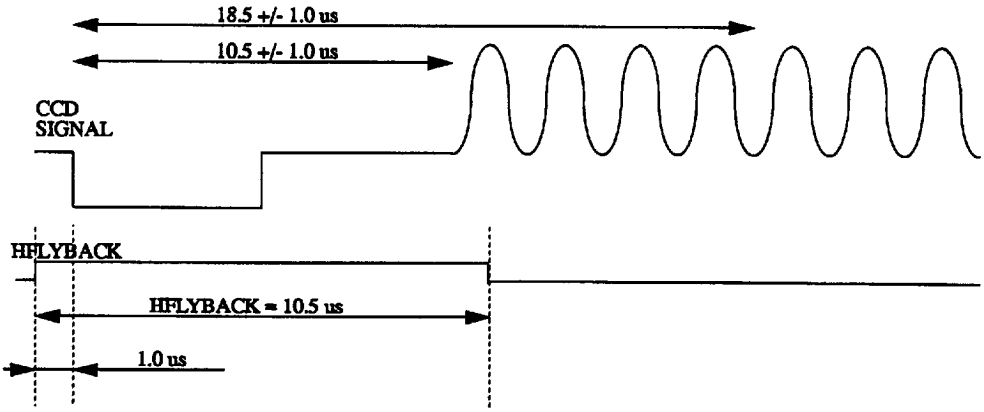


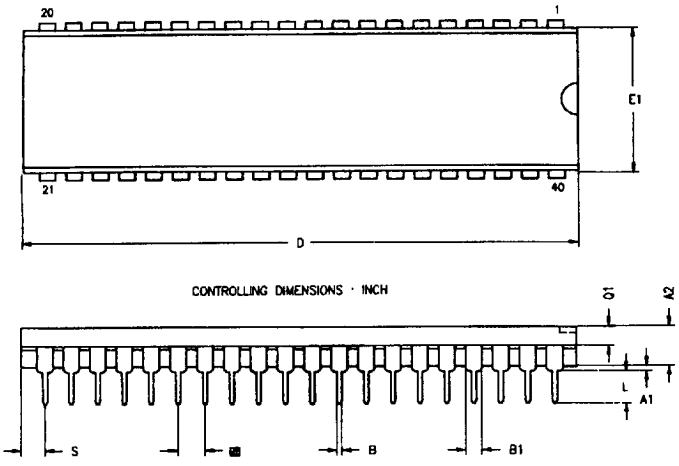
Figure 29. Register Settling Timing Diagram

In this example the time delay from leading edge of HSYNC to trailing edge of HFLYBACK is specified to be 9.5 µs.

In order to position the clamp in the middle of the back porch, the "Position" field of Clamp Position register should be set to 57% (7.2 µs).

The CCD data capture algorithm requirements are satisfied and this particular setting corresponds to the middle of the operating range.

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	060	.075
S	1 52	2.29	.060	.090

40-DIP Package Diagram

ORDERING INFORMATION

Z89300

24 MHz
42-Pin DIP
Z8930024PSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
P = Plastic DIP

Temperature
S = 0°C to 70°C

Speeds
24 = 24 MHz

Environmental
C = Plastic Standard

Example:

Z 89300 24 P S C is a Z89300, 24 MHz, DIP, 0°C to +70°C, Plastic Standard Flow