Z89321/371/391

16-BIT DIGITAL SIGNAL PROCESSORS

FEATURES

Part	DSP ROM (K Words)	OTP (K Words)	DSP RAM (Words)	MIPS (Max)
Z89321	4		512	20
Z89371		4	512	16
Z89391	64*		512	20

Package Part	40-Pin DIP	44-Pin PLCC	44-Pin QFP	84-Pin PLCC
Z89321	X	X	X	
Z89371	X	X	X	
Z89391				X

* External

- 0°C to +70°C Operating Temperature Range
- 4.5- to 5.5-Volt Operating Range

DSP Core

- 20 MIPS @ 20 MHz, 16-Bit Fixed Point DSP
- 50 ns Instruction Cycle Time
- Six-Level Hardware Stack
- Six Register Address Pointers
- Optimized Instruction Set (30 Instructions)

On-Board Peripherals

- Dual 8/16-Bit CODEC Interface Capable of up to 10 Mbps
- μ-Law Compression Option (Decompression is performed in software)
- 16-Bit I/O Bus (Tri-Stated)
- Three I/O Address Pins (Latched Outputs)
- Wait-State Generator
- Three Vectored Interrupts
- 13-Bit General-Purpose Timer

GENERAL DESCRIPTION

The Z893XX family of products are high-performance Digital Signal Processors (DSPs) with a modified Harvard-type architecture featuring separate program and data memory. The design has been optimized for processing power and minimizing silicon space.

The single-cycle instruction execution and bus structure promotes efficient algorithm execution, while the six register pointers provide circular buffering capabilities and dual operand fetching.

Three vectored interrupts are complemented by a six level stack, and the CODEC interface allows high-speed transfer rates to accommodate digital audio and voice data.

A dedicated Counter/Timer provides the necessary timing signals for the CODEC interface, and an additional 13-bit timer is available for general-purpose use.

The Z893XX DSPs are optimized to accommodate advanced signal processing algorithms. The 20 MIPS (maximum) operating performance and efficient architecture provides real-time instruction execution. Compression, filtering, frequency detection, audio, voice detection/synthesis and other vital algorithms can all be accommodated.

GENERAL DESCRIPTION (Continued)

The Z89321/371/391 devices feature an on-board CODEC interface, compatible with 8-bit PCM and 16-bit CODECs for digital audio applications. Additionally, an on-board wait-state generator is provided to accommodate slow external peripherals.

For prototypes, as well as production purposes, the Z89371 member of the DSP product family is a one-time programmable (OTP) device with a 16 MHz maximum operating frequency.

Throughout this specification, references to the Z89321 device applies equally to the Z89371 and Z89391, unless otherwise specified.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

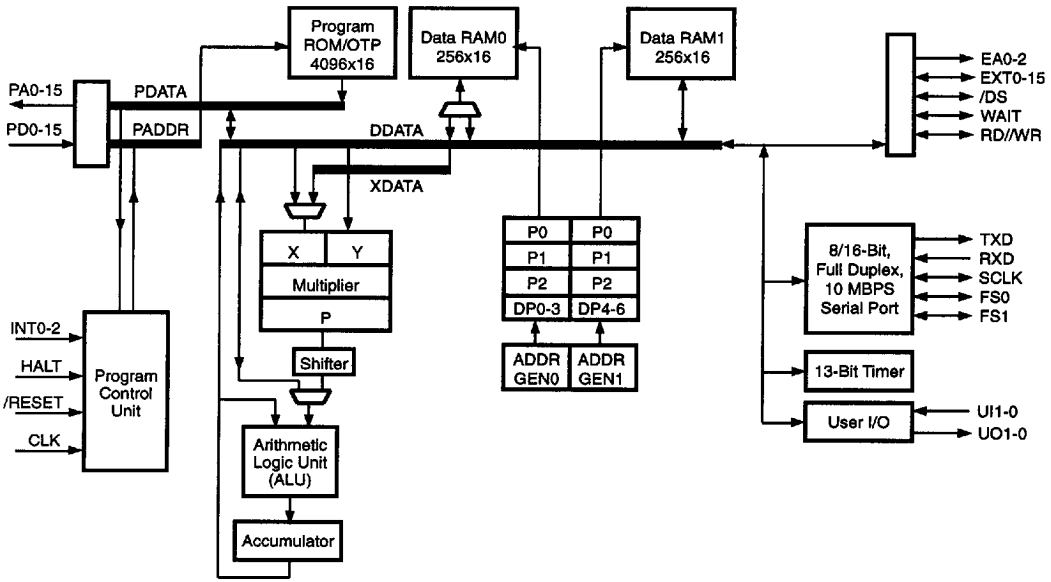


Figure 1. Z89321/371/391 Functional Block Diagram

PIN DESCRIPTION

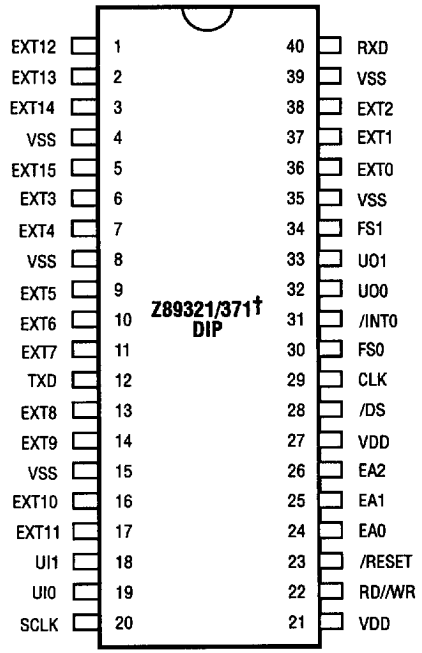


Figure 2. Z89321/371 40-Pin DIP Pin Assignments

Table 1. Z89321/371 40-Pin DIP Pin Identification

No.	Symbol	Function	Direction
1-3	EXT12-EXT14	External data bus	Input/Output
4	V_{SS}	Ground	
5	EXT15	External data bus	Input/Output
6-7	EXT3-EXT4	External data bus	Input/Output
8	V_{SS}	Ground	
9-11	EXT5-EXT7	External data bus	Input/Output
12	TXD	Serial output to CODECs	Output
13-14	EXT8-EXT9	External data bus	Input/Output
15	V_{SS}	Ground	
16-17	EXT10-EXT11	External data bus	Input/Output
18	UI1	User input	Input
19	UI0	User input	Input
20	SCLK	CODEC serial clock	Input/Output*
21	V_{DD}	Power supply	Input
22	RD//WR	Strobes for external bus	Output
23	/RESET	Reset	Input
24-26	EA0-EA2	External address bus	Output
27	V_{DD}	Power supply	Input
28	/DS	Data strobe for external bus	Output
29	CLK	Clock	Input
30	FS0	CODEC 0 frame sync	Input/Output*
31	/INT0	Interrupt	Input
32-33	UO0-UO1	User output	Output
34	FS1	CODEC 1 frame sync	Input/Output*
35	V_{SS}	Ground	
36-38	EXT0-EXT2	External data bus	Input/Output
39	V_{SS}	Ground	
40	RXD	Serial input from CODECs	Input

Notes:
* Input or output is defined by interface mode selection.
† HALT and WAIT pins are not available on the 40-pin DIP package.

PIN DESCRIPTION (Continued)

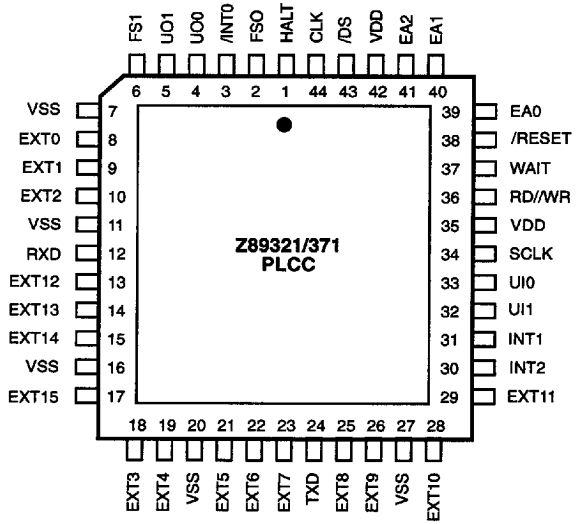


Figure 3. Z89321/371 44-Pin PLCC Pin Assignments

Table 2. Z89321/371 44-Pin PLCC Pin Identification

No.	Symbol	Function	Direction
1	HALT	Stop execution	Input
2	FS0	CODEC 0 frame sync	Input/Output*
3	/INT0	Interrupt	Input
4-5	UO0-UO1	User output	Output
6	FS1	CODEC 1 frame sync	Input/Output*
7	V_{SS}	Ground	
8-10	EXT0-EXT2	External data bus	Input/Output
11	V_{SS}	Ground	
12	RXD	Serial input from CODECs	Input
13-15	EXT12-EXT14	External data bus	Input/Output
16	V_{SS}	Ground	
17	EXT15	External data bus	Input/Output
18-19	EXT3-EXT4	External data bus	Input/Output
20	V_{SS}	Ground	
21-23	EXT5-EXT7	External data bus	Input/Output
24	TXD	Serial output to CODECs	Output
25-26	EXT8-EXT9	External data bus	Input/Output
27	V_{SS}	Ground	
28-29	EXT10-EXT11	External data bus	Input/Output
30	/INT2	Interrupt	Input
31	/INT1	Interrupt	Input
32	UI1	User input	Input
33	UI0	User input	Input
34	SCLK	CODEC serial clock	Input/Output*
35	V_{DD}	Power supply	Input
36	RD//WR	RD//WR strobe for EXT bus	Output
37	WAIT	WAIT state	Input
38	/RESET	Reset	Input
39-41	EA0-EA2	External address bus	Output
42	V_{DD}	Power supply	Input
43	/DS	Data strobe for external bus	Output
44	CLK	Clock	Input

Note:
* Input or output is defined by interface mode selection.

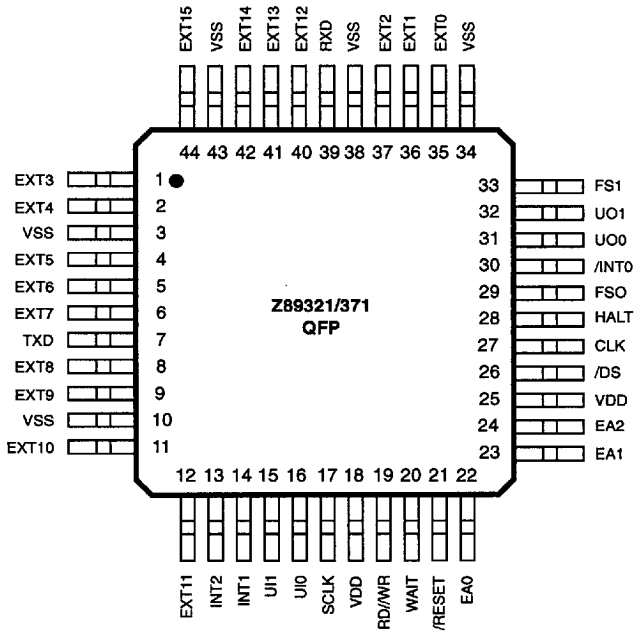


Figure 4. Z89321/371 44-Pin QFP Pin Assignments

Table 3. Z89321/371 44-Pin QFP Pin Identification

No.	Symbol	Function	Direction
1-2	EXT3-EXT4	External data bus	Input/Output
3	V_{SS}	Ground	
4-6	EXT5-EXT7	External data bus	Input/Output
7	TXD	Serial output to CODECs	Output
8-9	EXT8-EXT9	External data bus	Input/Output
10	V_{SS}	Ground	
11-12	EXT10-EXT1	External data bus	Input/Output
13	/INT2	Interrupt	Input
14	/INT1	Interrupt	Input
15	UI1	User input	Input
16	UI0	User input	Input
17	SCLK	CODEC serial clock	Input/Output*
18	V_{DD}	Power supply	Input
19	RD//WR	RD//WR strobe EXT bus	Output
20	WAIT	WAIT state	Input
21	/RESET	Reset	Input
22-24	EA0-EA2	External address bus	Output
25	V_{DD}	Power supply	Input
26	/DS	Data strobe for external bus	Output
27	CLK	Clock	Input
28	HALT	Stop execution	Input
29	FS0	CODEC 0 frame sync	Input/Output*
30	/INT0	Interrupt	Input
31-32	UO0-UO1	User output	Output
33	FS1	CODEC 1 frame sync	Input/Output*
34	V_{SS}	Ground	
35-37	EXT0-EXT2	External data bus	Input/Output
38	V_{SS}	Ground	
39	RXD	Serial input to CODECs	Input
40-42	EXT12-EXT14	External data bus	Input/Output
43	V_{SS}	Ground	
44	EXT15	External data bus	Input/Output

Note:
*Input or output is defined by interface mode selection.

PIN DESCRIPTION (Continued)

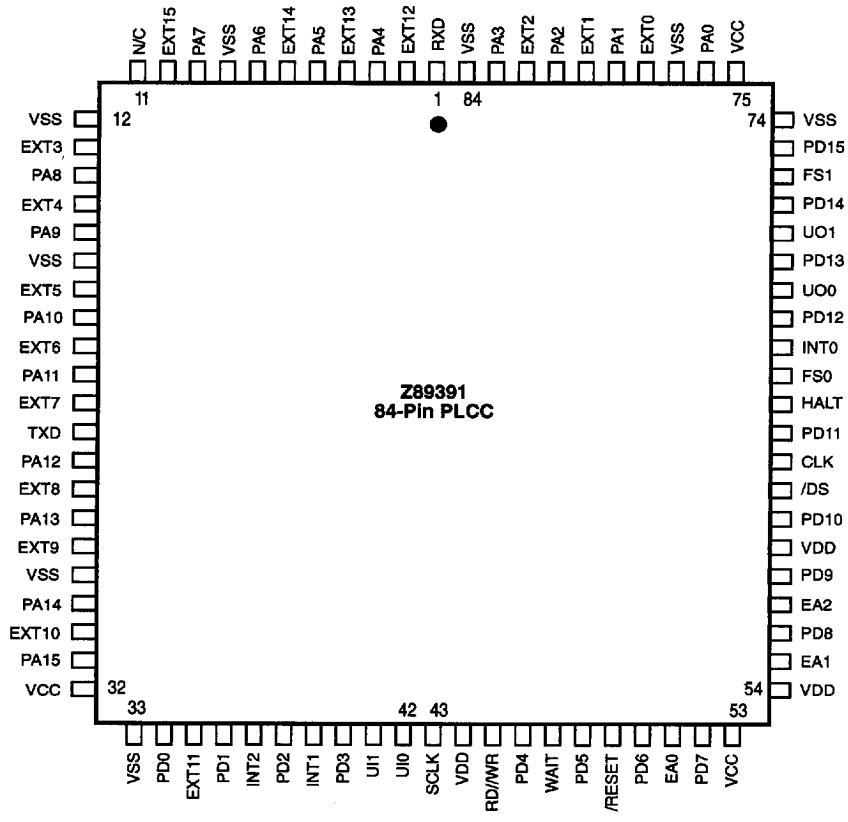


Figure 5. Z89391 84-Pin PLCC Pin Assignments

Table 4. Z89391 84-Pin PLCC Pin Identification

Symbol	Function	Direction
EXT15-EXT0	External data bus	Input/Output
V_{SS}	Ground	
PD15-PD0	Program data bus	Input
PA15-PA0	Program address bus	Output
V_{DD}	Power supply	Input
EA2-EA0	External address bus	Output
/DS	Data strobe	Output
RD//WR	READ//WRITE strobe	Output
WAIT	WAIT state	Input
/RESET	Reset	Input

Symbol	Function	Direction
CLK	Clock	Input
HALT	Stop execution	Input
UI1-UI0	User inputs	Input
INT2-INT0	Interrupts	Input
UO1-UO0	User outputs	Output
SCLK	CODEC serial clock	Input/Output*
FS0	CODEC 0 frame sync	Input/Output*
FS1	CODEC 1 frame sync	Input/Output*
RXD	Serial input to CODECs	Input
TXD	Serial output to CODECs	Output

Note:
* Input or output is defined by interface mode selection.

PIN FUNCTIONS

CK *Clock* (input). This pin controls the external clock.

EXT15-EXT0 *External Data Bus* (input/output). These pins control the data bus for user-defined outside registers, such as an ADC or DAC. The pins are normally tri-stated, except when the outside registers are specified as destination registers in the instructions. All the control signals exist to allow a read or a write through this bus.

RD/WR *Read/Write Strobe* (output). This pin controls the data direction signal for EXT-Bus. Data is available from the CPU on EXT15-EXT0 when this signal is Low. EXT-Bus is in input mode (high-impedance) when this signal is High.

EA2-EA0 *External Address* (output). These pins control the user-defined register address output (latched). One of eight user-defined external registers is selected by the processor with these address pins for read or write operations. Since the addresses are part of the processor memory map, the processor is simply executing internal reads and writes. External Addresses EXT4-EXT7 are used internally by the processor if the CODEC interface and 13-bit timer are enabled.

/DS *Data Strobe* (output). This pin control the data strobe signal for EXT-Bus. Data is read by the external peripheral on the rising edge of /DS. Data is also read by the processor on the rising edge of CK /DS.

HALT *Halt State (input).* This pin controls Stop Execution. The CPU continuously executes NOPs and the program counter remains at the same value when this pin is held High. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT. (HALT is not available on the 40-pin DIP package.)

/INT2-/INT0 *Three Interrupts* (input, active Low). These pins control interrupt requests 2-0. Interrupts are generated on the rising edge of the input signal. Interrupt vectors for the interrupt service starting address are stored in the following program memory locations:

Device	/INT0	/INT1	/INT2
Z89321/371	0FFFH	0FFEH	0FFDH
Z89391	FFFFH	FFFEH	FFFDH

Priority is: INT2 = lowest, INT0 = highest. INT1 is dedicated to the CODEC interface and INT2 is dedicated to the 13-bit timer if both peripherals are enabled. (**Note:** INT1 and INT2 pins are not bonded-out on the 40-pin DIP package.)

/RESET *Reset* (input, active Low). This pin controls the asynchronous reset signal. The /RESET signal must be kept Low for at least one clock cycle. The CPU pushes the contents of the Program Counter (PC) onto the stack and then fetches a new PC value from program memory address 0FFCH (or FFFCH for the Z89391) after the reset signal is released.

WAIT *WAIT State* (input). The wait signal is sampled at the rising edge of the clock with appropriate setup and hold times. The normal write cycle will continue when wait is inactive on a rising clock. A single wait-state can be generated internally by setting the appropriate bits in the EXT7-2 register. (WAIT is not available on the 40-pin DIP package.)

UI1-UI0 *Two Input Pins* (input). These general-purpose input pins are directly tested by the conditional branch instructions. These are asynchronous input signals that have no special clock synchronization requirements.

UO1-UO0 *Two Output Pins* (output). These general-purpose output pins reflect the value of two bits in the status register S5 and S6. These bits have no special significance and may be used to output data by writing to the status register. A mask option is available for open-drain or push-pull outputs. **Note:** The user output value is the opposite of the status register content.

ADDRESS SPACE

Program Memory. Programs of up to 4 Kwords can be masked into internal ROM (OTP for Z89371). Four locations are dedicated to the vector address for the three interrupts (0FFDH-0FFFH) and the starting address following a Reset (0FFCH). Internal ROM is mapped from 0000H to 0FFFH, and the highest location for program is 0FFBH. A 64 Kword External Program Memory Space is available on the Z89391. The vector addresses for the Z89391 reside at FFFCH-FFFFH (Figure 6).

Internal Data RAM. The Z89321, 371 and 391 all have internal 512 x 16-bit word data RAM organized as two banks of 256 x 16-bit words each: RAM0 and RAM1. Each data RAM bank is addressed by three pointers: Pn:0 (n = 0-2) for RAM0 and Pn:1 (n = 0-2) for RAM1. The RAM addresses for RAM0 and RAM1 are arranged from 0-255 and 256-511, respectively. The address pointers, which may be written to, or read from, are 8-bit registers connected to the lower byte of the internal 16-bit D-Bus and are used to perform modulo addressing. Three addressing modes are available to access the Data RAM: register indirect, direct addressing, and short form direct. The contents of the RAM can be read to, or written from, in one machine cycle per word, without disturbing any internal registers or status other than the RAM address pointer used for each RAM. The contents of each RAM can be loaded simultaneously into the X and Y inputs of the multiplier.

Registers. The Z89321 has 19 internal registers and up to an additional eight external registers. The external registers are user-definable for peripherals, such as A/D or D/A, or to DMA, or other addressing peripherals. Both external and internal registers are accessed in one machine cycle.

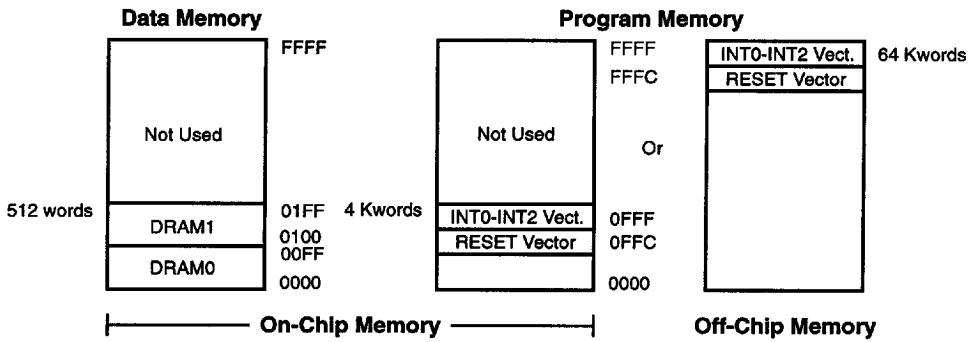


Figure 6. Memory Map

FUNCTIONAL DESCRIPTION

Instruction Timing. Most instructions are executed in one machine cycle. Long immediate instructions and Jump or Call instructions are executed in two machine cycles. A multiplication or multiplication/accumulate instruction requires a single cycle. Specific instruction cycle times are described in the Condition Code section.

Multiply/Accumulate. The multiplier can perform a 16-bit x 16-bit multiply, or multiply accumulate, in one machine cycle using the Accumulator and/or both the X and Y inputs. The multiplier produces a 32-bit result, however, only the 24 most significant bits are saved for the next instruction or accumulation. For operations on very small numbers where the least significant bits are important, the data should first be scaled by eight bits (or the multiplier and multiplicand by four bits each) to avoid truncation errors. Note that all inputs to the multiplier should be fractional two's-complement, 16-bit binary numbers (Figure 7). This puts them in the range [–1 to 0.9999695], and the result is in 24 bits so that the range is [–1 to 0.9999999]. In addition, if 8000H is loaded into both X and Y registers, the resulting multiplication is considered an illegal operation as an overflow would result. Positive one cannot be represented in fractional notation, and the multiplier will actually yield the result 8000H x 8000H = 8000H (–1 x –1 = –1).

ALU. The ALU has two input ports, one of which is connected to the output of the 24-bit Accumulator. The other input is connected to the 24-bit P-Bus, the upper 16 bits of which are connected to the 16-bit D-Bus. A shifter between the P-Bus and the ALU input port can shift the data by three bits right, one bit right, one bit left or no shift (Figure 8).

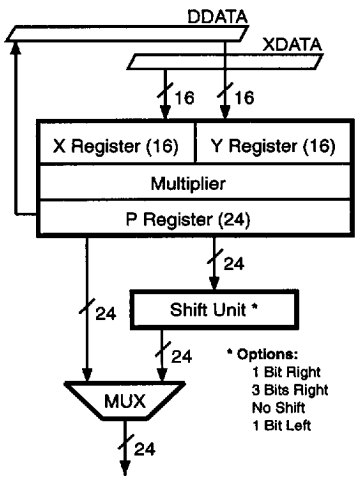


Figure 7. Multiplier Block Diagram

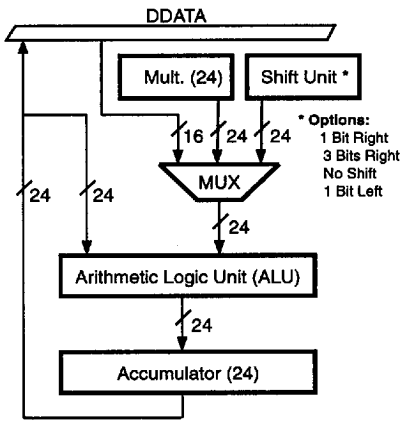


Figure 8. ALU Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Hardware Stack. A six-level hardware stack is connected to the D-Bus to hold subroutine return addresses or data. The Call instruction pushes PC+2 onto the stack, and the RET instruction pops the contents of the stack to the PC.

User Inputs. The Z89321 has two inputs, UI0 and UI1, which may be used by Jump and Call instructions. The Jump or Call tests one of these pins and if appropriate, jumps to a new location. Otherwise, the instruction behaves like a NOP. These inputs are also connected to the status register bits S10 and S11, which may be read by the appropriate instruction (Figure 8).

User Outputs. The status register bits S5 and S6 connect directly to UO0 and UO1 pins and may be written to by the appropriate instruction. **Note:** The user output value is the opposite of the status register content.

Interrupts. The Z89321 has three positive edge-triggered interrupt inputs. An interrupt is acknowledged at the end of an instruction execution. It takes two machine cycles to enter an interrupt instruction sequence. The PC is pushed onto the stack. A RET instruction transfers the contents of the stack to the PC and decrements the stack pointer by one word. The priority of the interrupts is INT0 = highest, INT2 = lowest. INT1 is dedicated to the CODEC interface and INT2 is dedicated to the 13-bit timer if both peripherals are enabled. **Note:** The SIEF instruction enables the interrupts. The SIEF instruction must be used before exiting an interrupt routine since the interrupts are automatically disabled when entering the routine.

Registers. The Z89321 has 19 physical internal registers and up to eight user-defined external registers. The EA2-EA0 determines the address of the external registers. The signals are used to read from or write to the external registers /DS, WAIT, RD//WR.

I/O Bus. The processor provides a 16-bit, CMOS-compatible bus. I/O Control pins provide convenient communication capabilities with external peripherals, and single-cycle access is possible. For slower communications, an on-board hardware wait-state generator can be used to accommodate timing conflicts. Three latched I/O address pins are used to access external registers. The EXT 4, 5, 6, 7 pins are used by the internal peripherals. Disabling a peripheral allows access to these addresses for general-purpose use.

CODEC Interface. The multi-compatible, dual CODEC interface provides the necessary control signals for transmission of CODEC information to the DSP processor. The interface accommodates 8-bit PCM or 16-bit Linear CODECs. Special compatibility with Crystal Semiconductor's 4215/4216 CODECs provides the necessary interface for audio applications. Many general-purpose 8-, 16-bit A/Ds, D/As are adaptable. The interface can also be used as a high-speed serial port.

μ-Law Compression. The 8-bit CODEC interface mode provides μ-law compression from 13-bit format to 8-bit format. Decompression is performed in software by use of a 128-word lookup table.

Timer. Two programmable timers are available. One is dedicated to the CODEC interface, the other for general-purpose use. When a time-out event occurs, an interrupt request is generated. Single pass and/or continuous modes are available. If the CODEC interface is not used, both timers can be used for general-purpose.

Wait-State Generator. An internal wait-state generator is provided to accommodate slow external peripherals. A single wait-state can be implemented through control registers EXT7-2. For additional states, a dedicated pin (WAIT) can be held High. The WAIT pin is monitored only during execution of a read or write instruction to external peripherals (EXT bus). **Note:** A WAIT pin is not available on the 40-pin DIP package.

REGISTERS

There are 19 internal registers which are defined below:

Register	Register Definition
P	Output of Multiplier, 24-bit
X	X Multiplier Input, 16-bit
Y	Y Multiplier Input, 16-bit
A	Accumulator, 24-bit
SR	Status Register, 16-bit
Pn:b	Six Ram Address Pointers, 8-bit each
PC	Program Counter, 16-bit
EXT4	13-Bit Timer Configuration Register
EXT5-1	CODEC Interface Channel 0 Data
EXT5-2	CODEC Interface Channel 0 Data
EXT6-1	CODEC Interface Channel 1 Data
EXT6-2	CODEC Interface Channel 1 Data
EXT7-1	CODEC Interface Configuration Register
EXT7-2	Wait-State Generator/CODEC Interface Configuration Register

The following are virtual registers as physical RAM does not exist on the chip.

Register	Register Definition
EXTn	External Registers, 16-bit
BUS	D-Bus
Dn:b	Eight Data Pointers*

Note:
* These occupy the first four locations in RAM bank.

P holds the result of multiplications and is read-only.

X and **Y** are two 16-bit input registers for the multiplier. These registers can be utilized as temporary registers when the multiplier is not being used.

A is a 24-bit Accumulator. The output of the ALU is sent to this register. When 16-bit data is transferred into this register, it is placed into the 16 MSBs and the least significant eight bits are set to zero. Only the upper 16 bits are transferred to the destination register when the Accumulator is selected as a source register in transfer instructions.

Pn:b are the pointer registers for accessing data RAM, (n = 0,1,2 refer to the pointer number) (b = 0,1 refers to RAM Bank 0 or 1). They can be directly read from or written to, and can point to locations in data RAM or Program Memory.

EXTn are external registers (n = 0 to 7). There are eight 16-bit registers provided here for mapping external devices into the address space of the processor. Note that the actual register RAM does not exist on the chip, but would exist as part of the external device, such as an ADC result latch. Use of the CODEC interface and 13-bit timer reduces the number of external registers to four.

BUS is a read-only register which, when accessed, returns the contents of the D-Bus. Bus is used for emulation only.

Dn:b refers to locations in RAM that can be used as a pointer to locations in program memory which is efficient for coefficient addressing. The programmer decides which location to choose from two bits in the status register and two bits in the operand. Thus, only the lower 16 possible locations in RAM can be specified. At any one time, there are eight usable pointers, four per bank, and the four pointers are in consecutive locations in RAM. For example, if S3/S4 = 01 in the status register, then D0:0/D1:0/D2:0/D3:0 refer to register locations 4/5/6/7 in RAM Bank 0. Note that when the data pointers are being written to, a number is actually being loaded to Data RAM, so they can be used as a limited method for writing to RAM.

SR is the status register (Figure 8) which contains the ALU status and certain control bits (Table 5).

Table 5. Status Register Bit Functions

Status Register Bit	Function
S15 (N)	ALU Negative
S14 (OV)	ALU Overflow
S13 (Z)	ALU Zero
S12 (L)	Carry
S11 (UI1)	User Input 1
S10 (UI0)	User Input 0
S9 (SH3)	MPY Output Arithmetically Shifted Right by three bits
S8 (OP)	Overflow Protection
S7 (IE)	Interrupt Enable
S6 (UO1)	User Output 1
S5 (UO0)	User Output 0
S4-S3	"Short Form Direct" bits
S2-S0 (RPL)	RAM Pointer Loop Size

REGISTERS (Continued)

The status register can always be read in its entirety. S15-S10 are set/reset by hardware and can only be read by software. S9-S0 control hardware looping and can be written by software (Table 6).

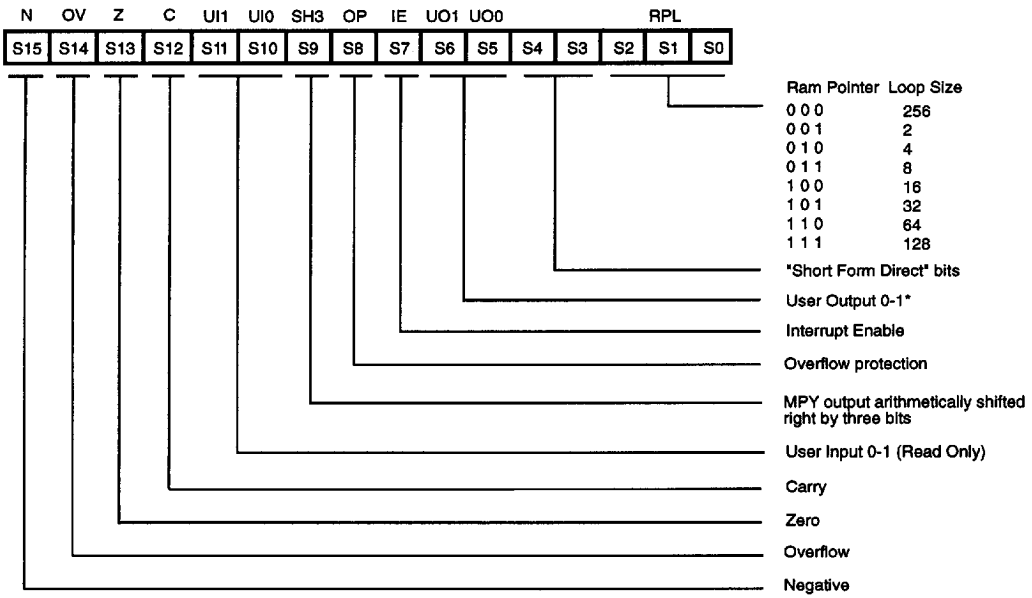
Table 6. RPL Description

S2	S1	S0	Loop Size
0	0	0	256
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

S15-S12 are set/reset by the ALU after an operation. S11-S10 are set/reset by the user inputs. S6-S0 are control bits described in Table 5. S7 enables interrupts. If S8 is set, the hardware clamps at maximum positive or negative values instead of overflowing. If S9 is set and a multiple/shift option is used, then the shifter shifts the result three bits right. This feature allows the data to be scaled and prevents overflows.

PC is the Program Counter. When this register is assigned as a destination register, one NOP machine cycle is added automatically to adjust the pipeline timing.

External Register, EXT4-EXT7, are used by the CODEC interface and 13-bit timer, the registers are reviewed in the CODEC interface section.



* The output value is the opposite of the status register content.

Figure 8. Status Register

PERIPHERAL OPERATION

Disabling Peripherals

Disabling a peripheral (CODEC Interface, Counter) allows general-purpose use of the EXT address for the disabled peripheral. If the peripheral is not disabled, the EXT control signals and EXT data are still provided, but transfer of data on the EXT pins is not available (because internal transfers are being processed on the internal bus). Care must be taken to ensure that control of the EXT bus does not cause bus conflicts.

Reading Data from CODEC Interface*

External data is serially transferred into the CODEC interface registers from an external CODEC. This serial data is loaded into EXT5-2 (8- or 16-bit modes). Because the interface is double-buffered, data must be transferred to EXT5-1 before being transferred along the internal data bus of the processor. This is accomplished by writing data to EXT5-2.

Writing Data to CODEC Interface*

Internal data is transferred from the internal data bus of the processor to the EXT5-2 register. The CODEC interface constantly transfers and receives data during normal operation. Data to be transferred is loaded to EXT5-2 and is automatically serially transferred.

Note: *EXT5-1 and EXT5-2 are used in the example, but this information applies equally to EXT6-1 and EXT6-2. (Refer to Figure 10, CODEC Block Diagram.)

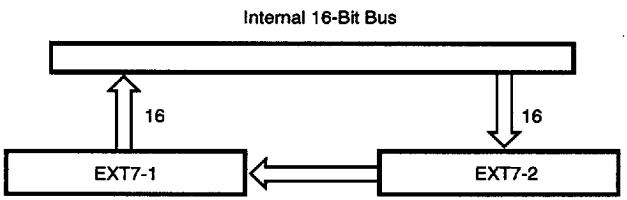


Figure 9. EXT7 Register Configuration

Loading EXT7

Because EXT7 is double-buffered, a pair of writes are performed when loading the EXT7 registers (Figure 9).

LD EXT7, #%54F4	Loads CODEC Timer Register
LD EXT7, #%6CDA	Loads Wait-State Register
LD @P0:0, EXT7	Reads EXT7-1 and places data in RAM

Interrupts

The Z89321 features three interrupts:

INT0	General-Purpose
INT1	CODEC Interface
INT2	13-Bit Timer

If all peripherals are enabled, INT0 (general-purpose) can be used.

PERIPHERALS (Continued)

CODEC Interface

The CODEC Interface provides direct-connect capabilities for standard 8-, 16-bit CODECs. The interface also supports 8-bit PCM, 8-bit PCM with hardware μ-law conversion (μ-law expansion is done in software), 16-bit Linear and Crystal's Sigma-Delta Stereo CODEC modes. Registers are used to accommodate the CODEC Interface (EXT5, EXT6 and EXT7). The CODEC interface provides two Frame Sync signals, which allows two channels of data for transmission/receiving.

CODEC Interface Hardware

The CODEC Interface hardware uses six 16-bit registers, μ-law compression logic and general-purpose logic to control transfers to the appropriate register (Figure 10).

CODEC Interface Control Signals

SCLK (Serial Clock)

The Serial Clock provides a clock signal for operating the external CODEC. A 4-bit prescaler is used to determine the frequency of the output signal.

SCLK = (0.5* CLK)/PS where: CLK = System Clock
PS = 4-bit Prescaler*

* The Prescaler is an up-counter.

Note: An internal divide-by-two is performed before the clock signal is passed to the Serial Clock prescaler.

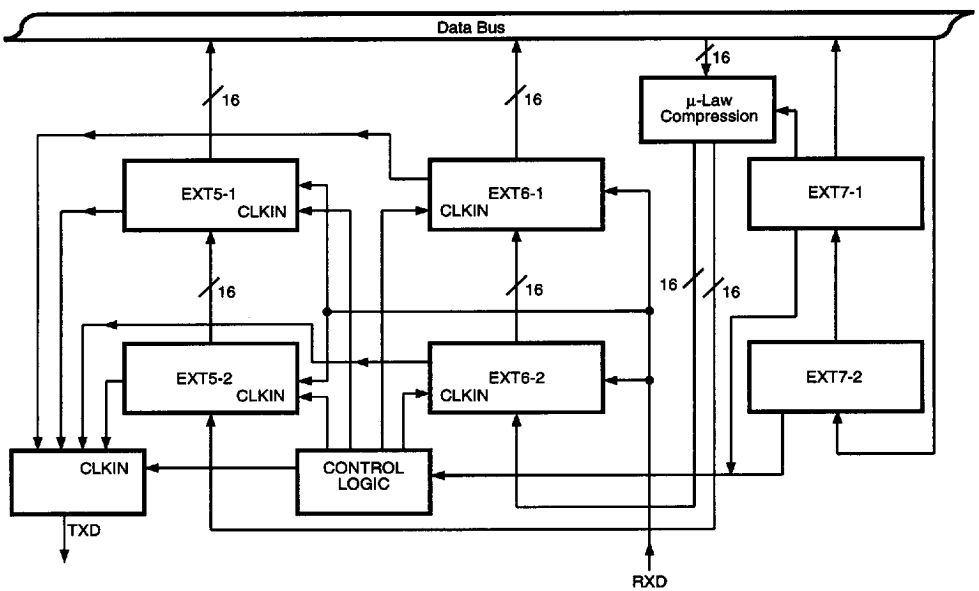


Figure 10. CODEC Interface Block Diagram

TXD (Serial Output to CODEC)
The TXD line provides 8-, 16-, and 64-bit data transfers. Each bit is clocked out of the processor by the rising edge of the SCLK, with the MSB transmitted first.

RXD (Serial Input from CODEC)
The RXD line provides 8-, 16-, and 64-bit data transfers. Each bit is clocked into the processor by the falling edge of the SCLK, with the MSB received first.

FS0, FS1 (Frame Sync)
The Frame Sync is used for enabling data transfer/receive. The rising and falling edge of the Frame Sync encloses the serial data transmission.

Interrupt
Once the transmission of serial data is completed an internal interrupt signal is initiated. A single-cycle Low pulse allows an interrupt on INT1. When this occurs, the processor will jump to the defined Interrupt 1 vector location (Figure 11).

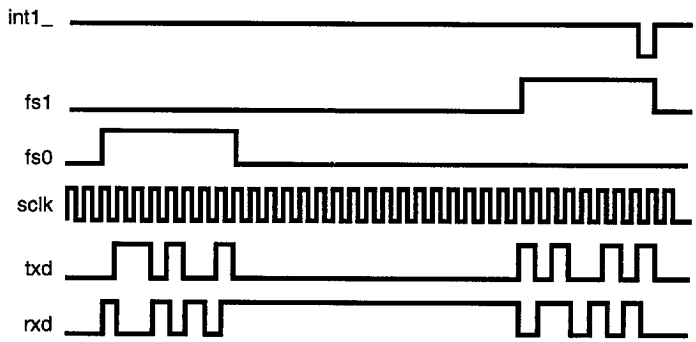


Figure 11. CODEC Interface Timing (8-Bit Mode)

CODEC Interface Timing

Figure 11 depicts a typical 8-bit serial data transfer using both of the CODEC Interface Channels. The transmitting data is clocked out on the rising edge of the SCLK signal. An external CODEC clocks data in on the falling edge of the SCLK signal. Once the serial data is transmitted, an interrupt is given. The CODEC interface signals are not initiated if the CODEC interface is not enabled.

The following modes are available for FSYNC and SCLK signals:

SCLK	FSYNC
Internal	Internal
External	External
External	Internal
Internal	External

The CODEC interface timing is independent of the processor clock when external mode is chosen. This feature provides the capability for an external device to control the transfer of data to the Z89321. The Frame Sync signal envelopes the transmitted data, therefore care must be taken to ensure proper sync signal timing (Figure 11).

Full Duplex Operation

The Transmit and Receive lines are used for transfer of serial data to or from the CODEC interface. The CODEC interface performs both data transmit and receive simultaneously.

PERIPHERALS (Continued)

Control Registers

The CODEC interface is double-buffered, therefore, four registers are provided for CODEC interface data storage. EXT5-1 and EXT5-2 operate with the Frame Sync 0 while EXT6-1 and EXT6-2 operate with Frame Sync 1. In 8- or 16-bit mode, the CODEC interface uses EXT5-1 and EXT6-1. For Stereo mode, all four registers are used (Figures 12 and 13).

The CODEC Interface Control Register (EXT7-1) is shown in Figure 14. Setting of the CODEC mode, FSYNC, and Enable/Disable of CODEC 0 is done through this register. The Wait-State Generator, SCLK, and CODEC 1 are controlled from EXT7-2 (Figure 14).

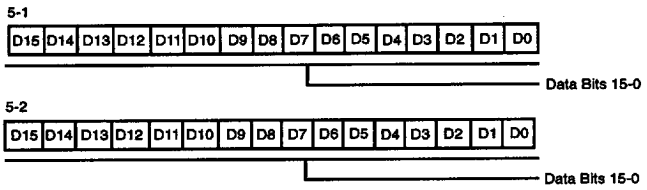


Figure 12. CODEC Interface Data Registers (Channel 0)

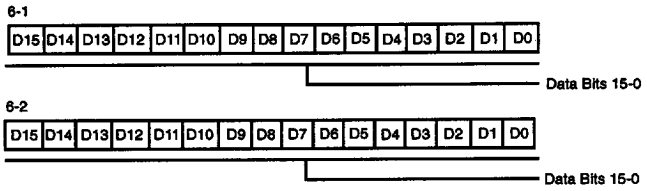


Figure 13. CODEC Interface Data Registers (Channel 1)

Registers

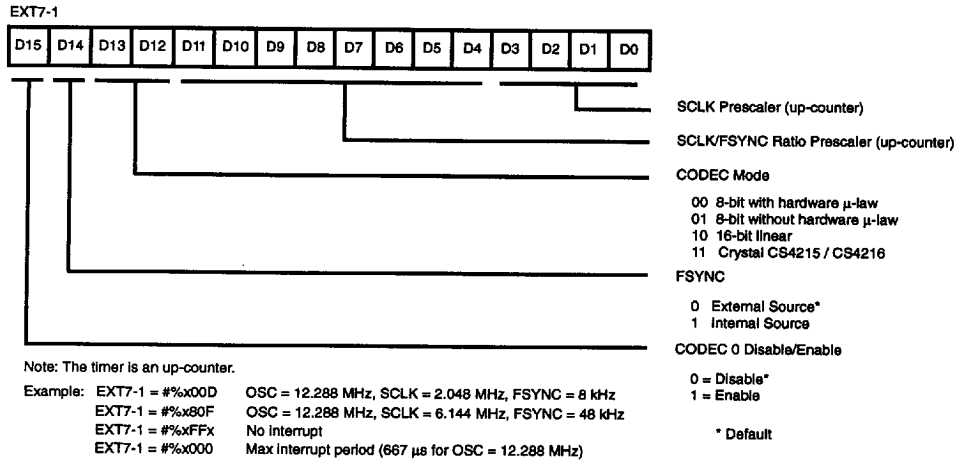


Figure 14. CODEC Interface Control Register

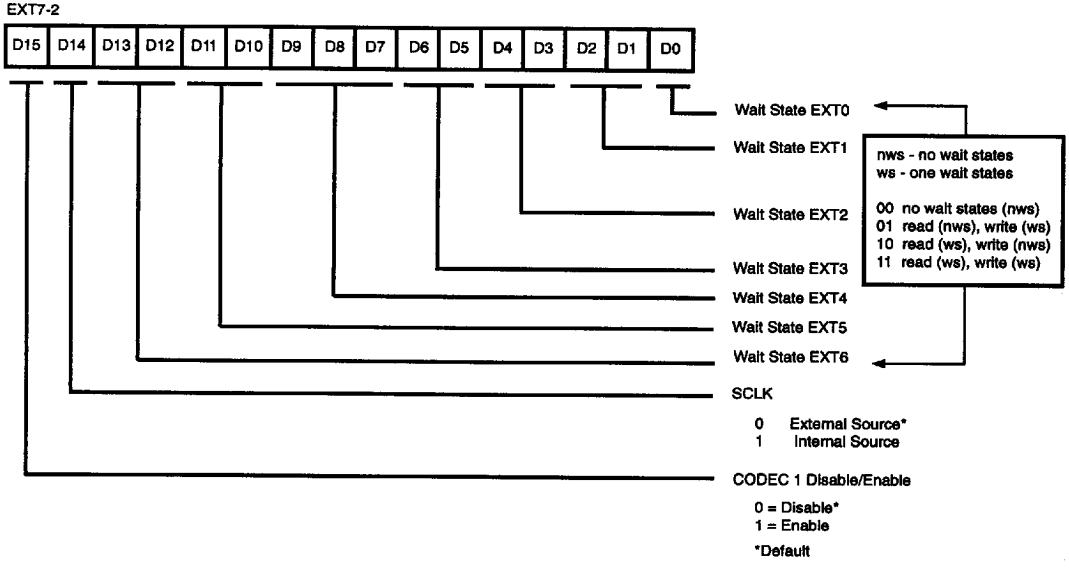


Figure 15. WSG, SCLK and CODEC Interface Control Register

PERIPHERALS (Continued)

A/D Accommodation

The CODEC interface can be used for serial A/D or serial D/A transmission. The interface provides the necessary control signals to adapt to many standard serial converters. The low-pass and smoothing filters are necessary for systems with converters.

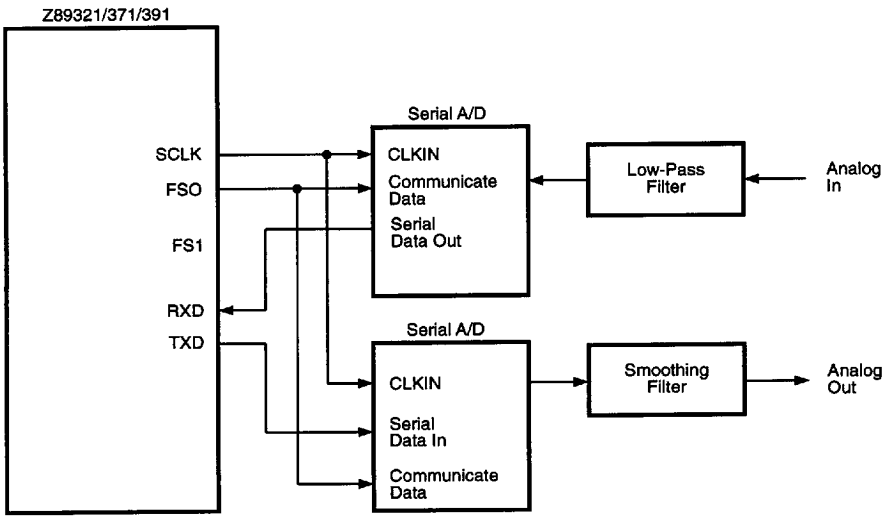


Figure 16. A/D, D/A Implementation Block Diagram

High-Speed Serial Port

The Z89321 CODEC interface can be used as a high-speed serial port. The necessary control signals are provided for adaptation to standard processors or external peripherals. Byte, word, or 64-bit data can be transmitted at speeds up to 10 Mbps. (Condition includes a 20 MHz oscillator. Data can be transferred with single-cycle instructions to an internal register file.)

Table 7. Tabulated Transmission Rates*

Transmission	Rate
Maximum SCLK	10 Mbps
Maximum Frame Sync	
8-bit	769.2 kHz
16-bit	476.2 kHz
Stereo (64-bit)	263.2 kHz

Notes:
* Calculations consider the interrupt access time (typically four cycles), transfer of data, loading of new data, and latency periods between CODEC transfers. During the interrupt cycle, developers often execute additional software, affecting the maximum transfer rate. Calculations are for single-channel transfers only.

8-Bit CODEC Interface

The Z89321 provides an option for a standard 8-bit CODEC interface. Hardware μ-law compression is available (expansion performed by software lookup table). The CODEC interface transmits data consisting of 8-bit or compounded 8-bit information. Figure 17 shows a typical schematic arrangement.

The timing for this type of arrangement is presented in Figure 18. The flexible design provides adaptation for 16-bit linear CODEC.

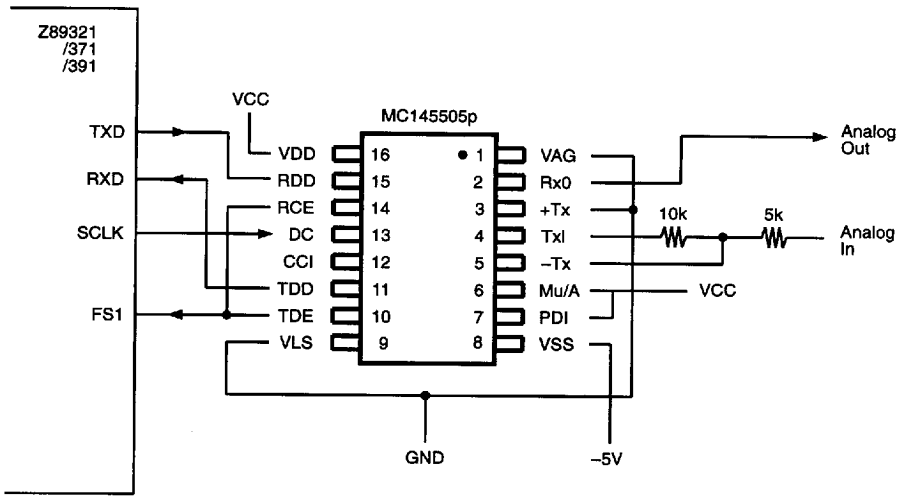


Figure 17. 8-Bit CODEC Schematic

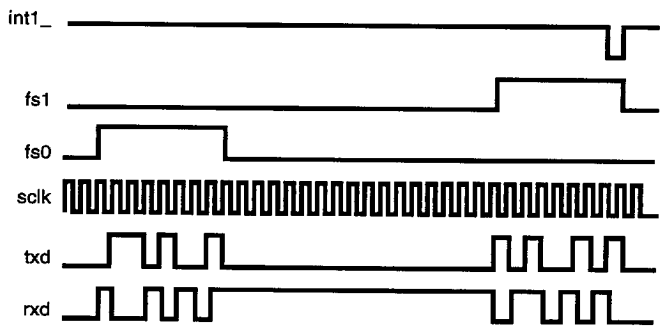


Figure 18. 8-Bit Mode Timing Diagram

PERIPHERALS (Continued)

16-Bit Linear CODEC Interface

For higher precision transmissions, a 16-bit linear CODEC is used, however, data is not compressed in this mode of transmission. The Z89321 provides accommodation for two channels of 16-bit transmission (Figure 19). For data acquisition systems, designers may opt for a 16-bit serial A/D. A block diagram of the Z89321 with the AD1876 16-bit 100 Kbps sampling ADC is shown in Figure 20.

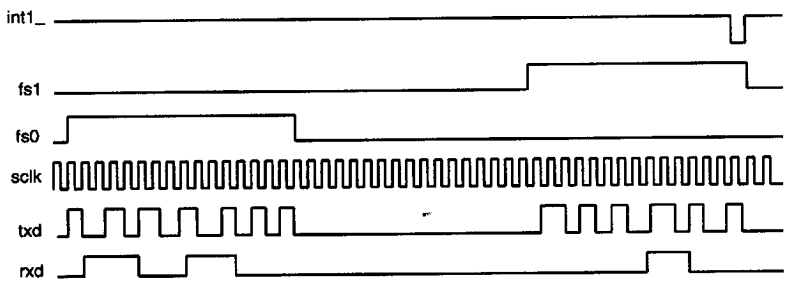


Figure 19. 16-Bit Mode Timing Diagram

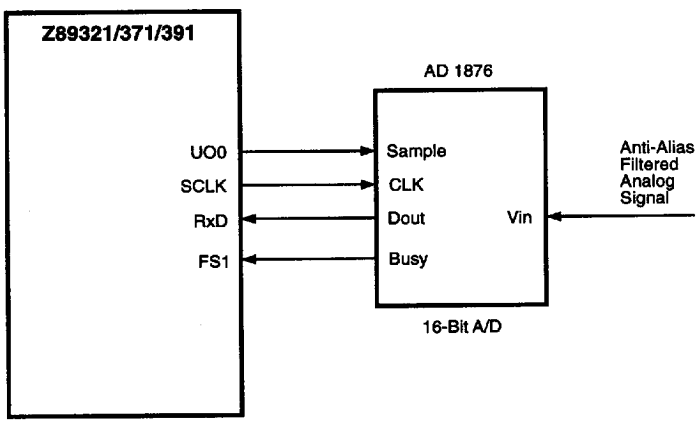


Figure 20. 16-Bit Serial A/D

Stereo CODEC Interface

The Z893XX DSP product family CODEC interface provides direct connection to other CODECs for master or slave modes, supporting 64 bits of transmission data (16 bits right channel, 16 bits left channel, and 32 bits of configuration information). This configuration information consists of input gain, input MUX, output attenuation, ADC clipping, and mute and error functions of the CODECs. A key feature of the Z893XX DSP product family is that it adapts easily to other stereo CODECs, including Crystal Semiconductor's CS4215 and CS4216 devices (Figure 21).

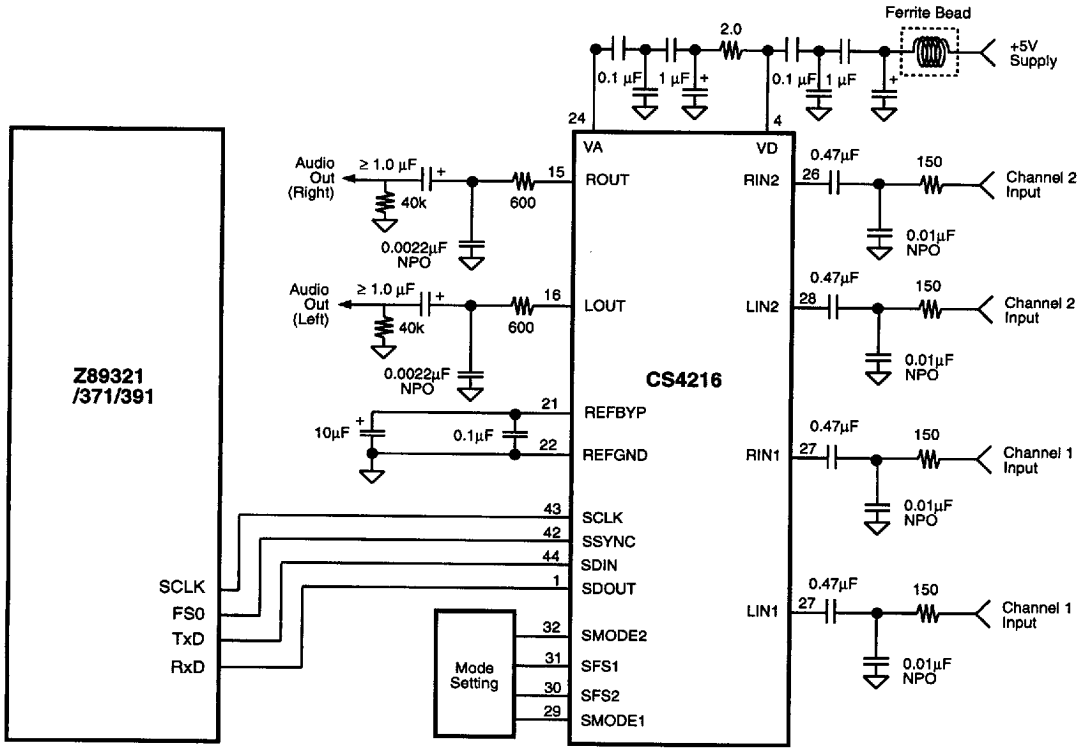


Figure 21. Z893XX and CS4216 CODEC Interface

PERIPHERALS (Continued)

The 64 bits of data transferred from the CODEC are placed in four registers, EXT5-1, 5-2, 6-1, and 6-2 (Figure 22).

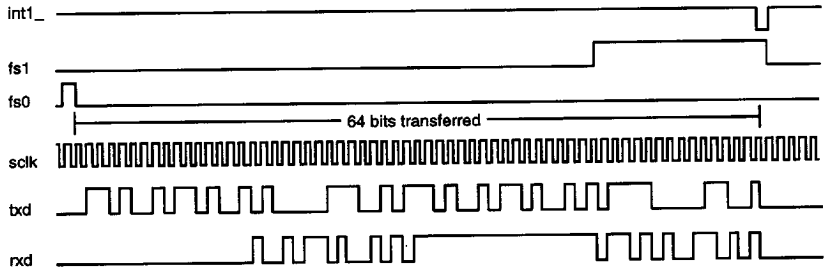


Figure 22. CODEC Stereo Mode Timing Diagram

13-Bit General-Purpose Timer

The 13-bit counter/timer is available for general-purpose use. When the counter counts down to the zero state, an interrupt is received on INT2. If the counter is disabled, EXT4 can be used as a general-purpose address. The counting operation of the counter can be disabled by resetting bit 14. Selection of the clock source allows the ability to extend the counter value past the 13 bits available in the control register. Use of the CODEC counter output can extend the counter to 26 bits (see Figure 23).

Notes:
Placing zeroes into the count value register does not generate an interrupt. Therefore, it is possible to have a single-pass option by loading the counter with zeroes after the start of count.

The counter is defaulted to the enable state, but if it is not needed, it can be disabled. However, once disabled, the counter cannot be enabled unless a reset of the processor is performed.

Example:

```
LD   EXT, #%C008   ;1100 0000 0000 1000
                   ; Enable Counter
                   ; Enable Counting
                   ; Clock Source = OSC/2
                   ; Count Value = 1000 = 8
                   ; Interrupt will occur every
                     16 clock cycles
```

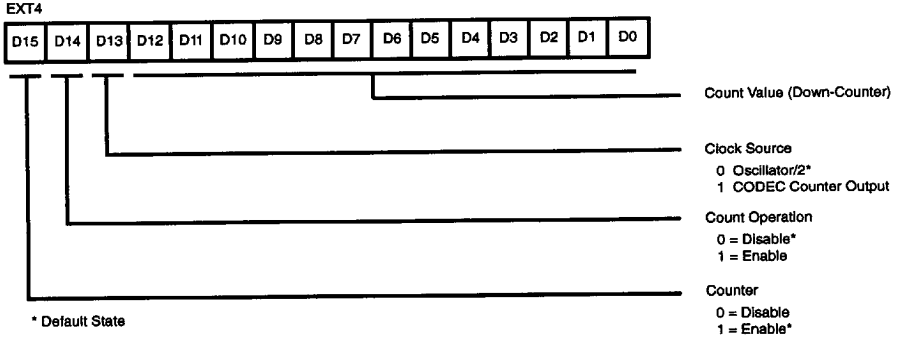


Figure 23. CODEC Timer Register

ADDRESSING MODES

This section discusses the syntax of the addressing modes supported by the DSP assembler.

Table 8. Addressing Modes

Symbolic Name	Syntax	Description
<pregs>	Pn:b	Pointer Register
<dregs> (Points to RAM)	Dn:b	Data Register
<hwregs>	X,Y,PC,SR,P EXTn,A,BUS	Hardware Registers
<accind> (Points to Program Memory)	@A	Accumulator Memory Indirect
<direct>	<expression>	Direct Address Expression
<limm>	#<const exp>	Long (16-bit) Immediate Value
<simm>	#<const exp>	Short (8-bit) Immediate Value
<regind> (Points to RAM)	@Pn:b @Pn:b+ @Pn:b–LOOP @Pn:b+LOOP	Pointer Register Indirect Pointer Register Indirect with Increment Pointer Register Indirect with Loop Decrement Pointer register Indirect with Loop Increment
<memind> (Points to Program Memory)	@@Pn:b @Dn:b @@Pn:b–LOOP @@Pn:b+LOOP @@Pn:b+	Pointer Register Memory Indirect Data Register Memory Indirect Pointer Register Memory Indirect with Loop Decrement Pointer Register Memory Indirect with Loop Increment Pointer Register Memory Indirect with Increment

ADDRESSING MODES (Continued)

There are eight distinct addressing modes for data transfer.

<pregs>, <hwregs> These two modes are used for simple loads to and from registers within the chip, such as loading to the Accumulator, or loading from a pointer register. The names of the registers need only be specified in the operand field (destination first, then source).

<regind> This mode is used for indirect accesses to the data RAM. The address of the RAM location is stored in the pointer. The "@" symbol indicates "indirect" and precedes the pointer, therefore @P1:1 instructs the processor to read or write to a location in RAM1, which is specified by the value in the pointer.

<dregs> This mode is also used for accesses to the data RAM, but only the lower 16 addresses in either bank. The 4-bit address comes from the status register and the operand field of the data pointer. Note that data registers are typically used not for addressing RAM, but loading data from program memory space.

<memind> This mode is used for indirect accesses to the program memory. The address of the memory is located in a RAM location, which is specified by the value in a pointer. Therefore, @@P1:1 instructs the processor to read (write is not possible) from a location in memory, which is specified by a value in RAM, and the location of the RAM is in turn specified by the value in the pointer. Note that the data pointer can also be used for a memory access in this manner, but only one "@" precedes the pointer. In both cases, the memory address stored in RAM is incremented by one, each time the addressing mode is used, to allow easy transfer of sequential data from program memory.

<accind> Similar to the previous mode, the address for the program memory read is stored in the Accumulator. @A in the second operand field loads the number in memory specified by the address in A.

<direct> The direct mode allows read or write to data RAM from the Accumulator by specifying the absolute address of the RAM in the operand of the instruction. A number between 0 and 255 indicates a location in RAM0, and a number between 256 and 511 indicates a location in RAM1.

<limm> This address mode indicates a long immediate load. A 16-bit word can be copied directly from the operand into the specified register or memory.

<simm> This address mode can only be used for immediate transfer of 8-bit data in the operand to the specified RAM pointer.

CONDITION CODES

The following Instruction Description defines the condition codes supported by the DSP assembler. If the instruction description refers to the <cc> (condition code) symbol in one of its addressing modes, the instruction will only execute if the condition is true.

Code	Description
C	Carry
EQ	Equal (same as Z)
F	False
IE	Interrupts Enabled
MI	Minus
NC	No Carry
NE	Not Equal (same as NZ)
NIE	Not Interrupts Enabled
NOV	Not Overflow
NU0	Not User Zero

Code	Description
NU1	Not User One
NZ	Not zero
OV	Overflow
PL	Plus (Positive)
U0	User Zero
U1	User One
UGE	Unsigned Greater Than or Equal (Same as NC)
ULT	Unsigned Less Than (Same as C)
Z	Zero

INSTRUCTION DESCRIPTIONS

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
ABS	Absolute Value	ABS[<cc>,]<src>	<cc>,A	1	1	ABS NC,A
			A	1	1	ABS A
ADD	Addition	ADD<dest>,<src>	A,<pregs>	1	1	ADD A,P0:0
			A,<dregs>	1	1	ADD A,D0:0
			A,<limm>	2	2	ADD A,#%1234
			A,<memind>	1	3	ADD A,@@P0:0
			A,<direct>	1	1	ADD A,%F2
			A,<regind>	1	1	ADD A,@P1:1
			A,<hwregs>	1	1	ADD A,X
			A, <simm>			ADD A, #%12
AND	Bitwise AND	AND<dest>,<src>	A,<pregs>	1	1	AND A,P2:0
			A,<dregs>	1	1	AND A,D0:1
			A,<limm>	2	2	AND A,#%1234
			A,<memind>	1	3	AND A,@@P1:0
			A,<direct>	1	1	AND A,%2C
			A,<regind>	1	1	AND A,@P1:2+LOOP
			A,<hwregs>	1	1	AND A,EXT3
			A, <simm>			AND A, #%12
CALL	Subroutine call	CALL [<cc>,]<address>	<cc>,<direct>	2	2	CALL Z,sub2
			<direct>	2	2	CALL sub1
CCF	Clear carry flag	CCF	None	1	1	CCF
CIEF	Clear Carry Flag	CIEF	None	1	1	CIEF
COPF	Clear OP flag	COPF	None	1	1	COPF
CP	Comparison	CP<src1>,<src2>	A,<pregs>	1	1	CP A,P0:0
			A,<dregs>	1	1	CP A,D3:1
			A,<memind>	1	3	CP A,@@P0:1
			A,<direct>	1	1	CP A,%FF
			A,<regind>	1	1	CP A,@P2:1+
			A,<hwregs>	1	1	CP A,STACK
			A<limm>	2	2	CP A,#%FFCF
			A, <simm>			CP A, #%12
DEC	Decrement	DEC [<cc>,]<dest>	<cc>A,	1	1	DEC NZ,A
			A	1	1	DEC A
INC	Increment	INC [<cc>,] <dest>	<cc>,A	1	1	INC PL,A
			A	1	1	INC A
JP	Jump	JP [<cc>,]<address>	<cc>,<direct>	2	2	JP NIE,Label
			<direct>	2	2	JP Label

INSTRUCTION DESCRIPTIONS (Continued)

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
LD	Load destination with source	LD<dest>,<src>	A,<hwregs>	1	1	LD A,X
			A,<dregs>	1	1	LD A,D0:0
			A,<pregs>	1	1	LD A,P0:1
			A,<regind>	1	1	LD A,@P1:1
			A,<memind>	1	3	LD A,@D0:0
			A,<direct>	1	1	LD A,124
			<direct>,A	1	1	LD 124,A
			<dregs>,<hwregs>	1	1	LD D0:0,EXT7
			<pregs>,<simm>	1	1	LD P1:1,#%FA
			<pregs>,<hwregs>	1	1	LD P1:1,EXT1
			<regind>,<limm>	1	1	LD@P1:1,#1234
			<regind>,<hwregs>	1	1	LD @P1:1+,X
			<hwregs>,<pregs>	1	1	LD Y,P0:0
			<hwregs>,<dregs>	1	1	LD SR,D0:0
			<hwregs>,<limm>	2	2	LD PC,#%1234
			<hwregs>,<accind>	1	3	LD X,@A
			<hwregs>,<memind>	1	3	LD Y,@D0:0
			<hwregs>,<regind>	1	1	LD A,@P0:0–LOOP
			<hwregs>,<hwregs>	1	1	LD X,EXT6
			Note: When <dest> is <hwregs>, <dest> cannot be P.			
			Note: When <dest> is <hwregs> and <src> is <hwregs>, <dest> cannot be EXTn if <src> is EXTn, <dest> cannot be X if <src> is X, <dest> cannot be SR if <src> is SR.			
			Note: When <src> is <accind> <dest> cannot be A.			
MLD	Multiply	MLD<srcl>,<srcl>[,<bank switch>]	<hwregs>,<regind>	1	1	MLD A,@P0:0+LOOP
			<hwregs>,<regind>,<bank switch>	1	1	MLD A,@P1:0,OFF
			<regind>,<regind>	1	1	MLD @P1:1,@P2:0
			<regind>,<regind>,<bank switch>	1	1	MLD @P0:1,@P1:0,ON
			Note: If src1 is <regind> it must be a bank 1 register. Src2's <regind must be a bank 0 register.			
			Note: <hwregs> for src1 cannot be X.			
			Note: For the operands <hwregs>, <regind> the <band switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.			
MPYA	Multiply and add	MPYA <srcl>,<src2>[,<bank switch>]	<hwregs>,<regind>	1	1	MPYA A,@P0:0
			<hwregs>,<regind>,<bank switch>	1	1	MPYA A,@P1:0,OFF
			<regind>,<regind>	1	1	MPYA @P1:1,@P2:0
			<regind>,<regind>,<bank switch>	1	1	MPYA@P0:1,@P1:0,ON
			Note: If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register.			
			Note: <hwregs> for src1 cannot be X.			
			Note: For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.			

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
MPYS	Multiply and subtract	MPYS<src1>,<src2>[,<bank switch>]	<hwregs>,<regind>	1	1	MPYS A,@P0:0
			<hwregs>,<regind>,<bank switch>	1	1	MPYS A,@P1:0,0FF
			<regind>,<regind>	1	1	MPYS @P1:1,@P2:0
			<regind>,<regind>,<bank switch>	1	1	MPYS@P0:1,@P1:0,ON
			Note: If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register.			
			Note: <hwregs> for src1 cannot be X.			
			Note: For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, <regind> the <bank switch> defaults to ON.			
NEG	Negate	NEG <cc>,A	<cc>, A	1	1	NEG MI,A
			A	1	1	NEG A
NOP	No operation	NOP	None	1	1	NOP
OR	Bitwise OR	OR <dest>,<src>	A, <pregs>	1	1	OR A,P0:1
			A, <dregs>	1	1	OR A, D0:1
			A, <limm>	2	2	OR A,#%2C21
			A, <memind>	1	3	OR A,@@P2:1+
			A, <direct>	1	1	OR A, %2C
			A, <regind>	1	1	OR A,@P1:0–LOOP
			A, <hwregs>	1	1	OR A,EXT6
			A, <simm>			OR A,#%12
POP	Pop value from stack	POP <dest>	<pregs>	1	1	POP P0:0
			<dregs>	1	1	POP D0:1
			<regind>	1	1	POP @P0:0
			<hwregs>	1	1	POP A
PUSH	Push value onto stack	PUSH <src>	<pregs>	1	1	PUSH P0:0
			<dregs>	1	1	PUSH D0:1
			<regind>	1	1	PUSH @P0:0
			<hwregs>	1	1	PUSH BUS
			<limm>	2	2	PUSH #12345
			<accind>	1	3	PUSH @A
			<memind>	1	3	PUSH @@P0:0
RET	Return from subroutine	RET	None	1	2	RET
RL	Rotate Left	RL <cc>,A	<cc>,A	1	1	RL NZ,A
			A	1	1	RL A
RR	Rotate Right	RR <cc>,A	<cc>,A	1	1	RR C,A
			A	1	1	RR A

INSTRUCTION DESCRIPTIONS (Continued)

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
SCF	Set C flag	SCF	None	1	1	SCF
SIEF	Set IE flag	SIEF	None	1	1	SIEF
SLL	Shift left logical	SLL	[<cc>,]A	1	1	SLL NZ,A
			A	1	1	SLL A
SOPF	Set OP flag	SOPF	None	1	1	SOPF
SRA	Shift right arithmetic	SRA<cc>,A	<cc>,A	1	1	SRA NZ,A
			A	1	1	SRA A
SUB	Subtract	SUB<dest>,<src>	A,<pregs>	1	1	SUB A,P1:1
			A,<dregs>	1	1	SUB A,D0:1
			A,<limm>	2	2	SUB A,#%2C2C
			A, <memind>	1	3	SUB A,@D0:1
			A, <direct>	1	1	SUB A,%15
			A, <regind>	1	1	SUB A,@P2:0–LOOP
			A, <hwregs>	1	1	SUB A,STACK
			A, <simm>			SUB A, #%12
XOR	Bitwise exclusive OR	XOR <dest>,<src>	A, <pregs>	1	1	XOR A,P2:0
			A, <dregs>	1	1	XOR A,D0:1
			A, <limm>	2	2	XOR A,#13933
			A, <memind>	1	3	XOR A,@@P2:1+
			A, <direct>	1	1	XOR A,%2F
			A, <regind>	1	1	XOR A,@P2:0
			A, <hwregs>	1	1	XOR A,BUS
			A, <simm>			XOR A, #%12

Bank Switch Enumerations. The third (optional) operand of the MLD, MPYA and MPYS instructions represents whether a bank switch is set ON or OFF. To more clearly represent this, the keywords ON and OFF are used to state the direction of the switch. These keywords are referenced in the instruction descriptions through the <bank switch> symbol. The most notable capability this provides is that a source operand can be multiplied by itself (squared).

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min.	Max.	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp	–65°	+150	°C
T_A	Oper Ambient Temp		†	°C

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

1

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 24).

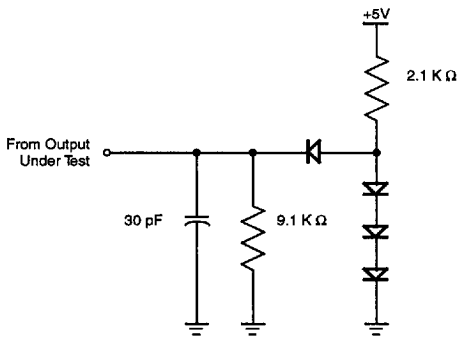


Figure 24. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±10%, T_A = 0°C to +70°C, unless otherwise noted.)

Sym.	Parameter	Condition	fclock = 20 MHz[1] Min.	Typ.	Max.	fclock = 16 MHz[2] Min.	Typ.	Max.	fclock = 10 MHz Min.	Typ.	Max.	Units
I_{DD}	Supply Current	V_{DD} = 5.5V		70			55			35		mA
I_{DC}	DC Power Consumption			5			5			5		mA
V_{IH}	Input High Level		2.7			2.7			2.7			V
V_{IL}	Input Low Level				.8			.8			.8	V
IL	Input Leakage				10			10			10	µA
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{DD}-0.2			V_{DD}-02			V_{DD}-02			V
V_{OL}	Input Low Voltage	I_{OL} = 2.0 mA			.5			.5			.5	V
I_{FL}	Output Floating Leakage Current				10			10			10	µA

Notes:
[1] Z89321 and Z89391 only.
[2] Z89371 only (V_{DD} = 5V ±5%)
[3] V_{DD} = 5V, ±5% for 16 MHz Z89371
[4] V_{DD} = 5V, ±10% for 10 MHz Z89371

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V 10%, T_A = 0°C to +70°C, unless otherwise specified)

Symbol	Parameter	fclock = 20 MHz[1] Min.	fclock = 20 MHz[1] Max.	fclock = 16 MHz[2] Min.	fclock = 16 MHz[2] Max.	fclock = 10 MHz Min.	fclock = 10 MHz Max.	Units
Clock								
TCY	Clock Cycle Time	50		62.5		100		ns
Tr	Clock Rise Time		2		2		2	ns
Tf	Clock Fall Time		2		2		2	ns
CPW	Clock Pulse Width	23		29		48		ns
I/O								
DSVALID	/DS Valid Time from CLOCK Fall	0	15	0	18	0	25	ns
DSHOLD	/DS Hold Time from CLOCK Rise	4	15	5	18	5	25	ns
EASET	EA Setup Time to /DS Fall	12		15		18		ns
EAHOLD	EA Hold Time from /DS Rise	4		5		6		ns
RDSET	Data Read Setup Time to /DS Rise	14		17		21		ns
RDHOLD	Data Read Hold Time from /DS Rise	6		6		6		ns
WRVALID	Data Write Valid Time from /DS Fall		18		22		30	ns
WRHOLD	Data Write Hold Time from /DS Rise	5		5		5		ns
Interrupt								
INTSET	Interrupt Setup Time to CLOCK Fall	7		9		11		ns
INTWIDTH	Interrupt Low Pulse Width	1 TCY		1 TCY		1 TCY		ns
Codec Interface								
SSET	SCLK Setup Time from Clock Rise		15		18		22	ns
FSSET	FSYNC Setup Time from SCLK Rise		6		7		9	ns
TXSET	TXD Setup Time from SCLK Rise		7		9		11	ns
RXSET	RXD Setup Time to SCLK Fall	7		9		11		ns
RXHOLD	RXD Hold Time from SCLK Fall	0		0		0		
Reset								
RRISE	Reset Rise Time		1000		1200		1500	ns
RSET	Reset Setup Time to CLOCK Rise	15		18		22		ns
RWIDTH	Reset Low Pulse Width	2 TCY		2 TCY		2 TCY		ns
External Program Memory								
PAVALID	PA Valid Time from CLOCK Rise		20		25		35	ns
PDSET	PD Setup Time to CLOCK Rise	10		12		15		ns
PDHOLD	PD Hold Time from CLOCK Rise	10		10		10		ns
Wait State								
WSET	WAIT Setup Time to CLOCK Rise	23		29		35		ns
WHOLD	WAIT Hold Time from CLOCK Rise	1		1		2		ns
Halt								
HSET	Halt Setup Time to CLOCK Rise	3		4		5		ns
HHOLD	Halt Hold Time from CLOCK Rise	10		12		15		ns

Notes:
[1] Z89321 and Z89391 only.
[2] Z89371 only (V_{DD} = 5V ±5%)

TIMING DIAGRAMS

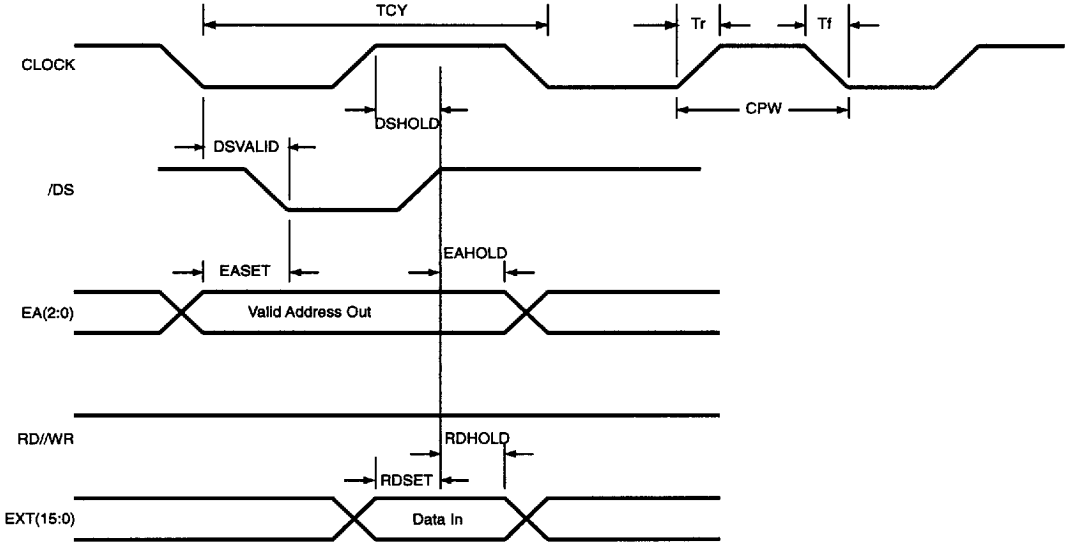


Figure 25. Read Timing

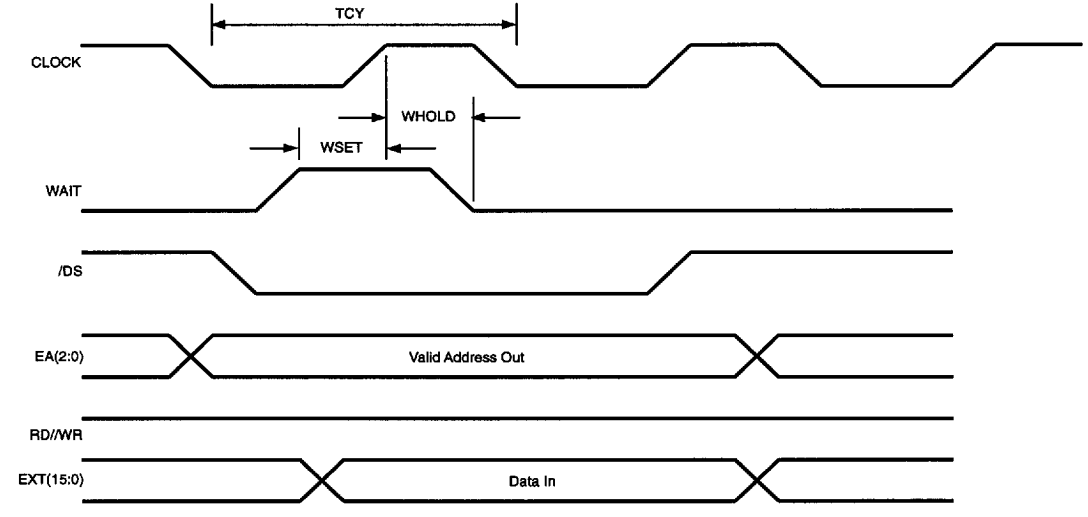


Figure 26. External (EXT) Bus Read Timing Using WAIT Pin

TIMING DIAGRAMS (Continued)

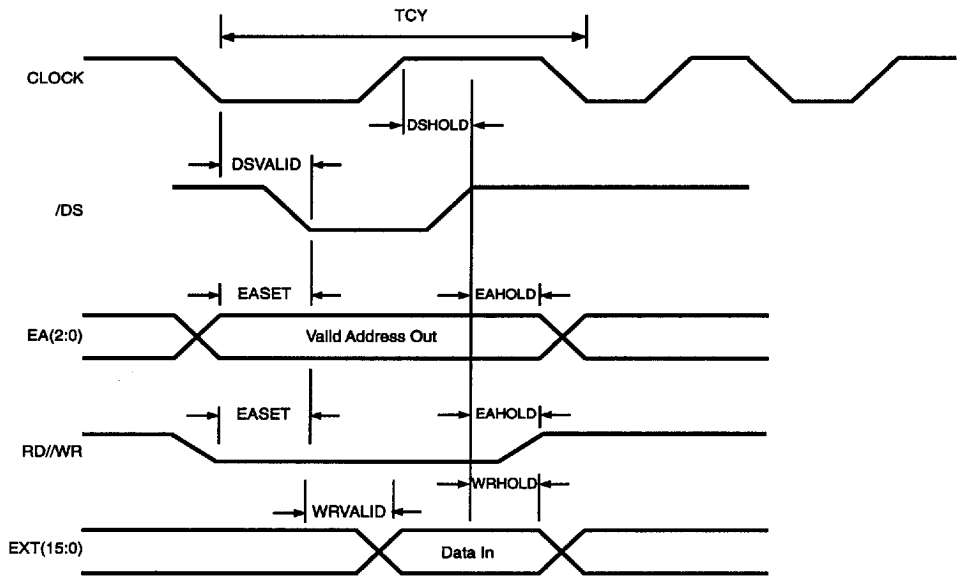


Figure 27. Write Timing

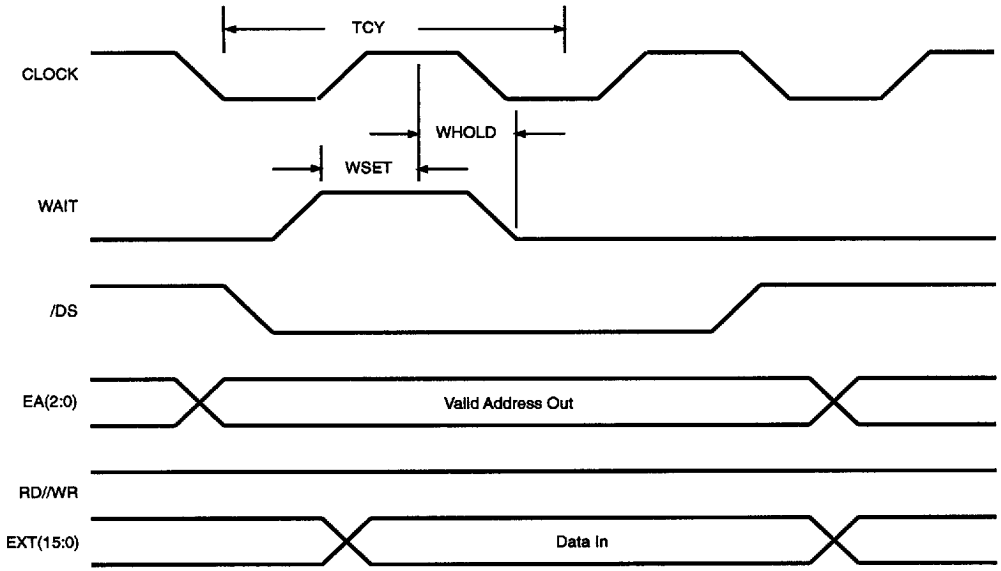


Figure 28. Write Timing Using WAIT Pin

TIMING DIAGRAMS (Continued)

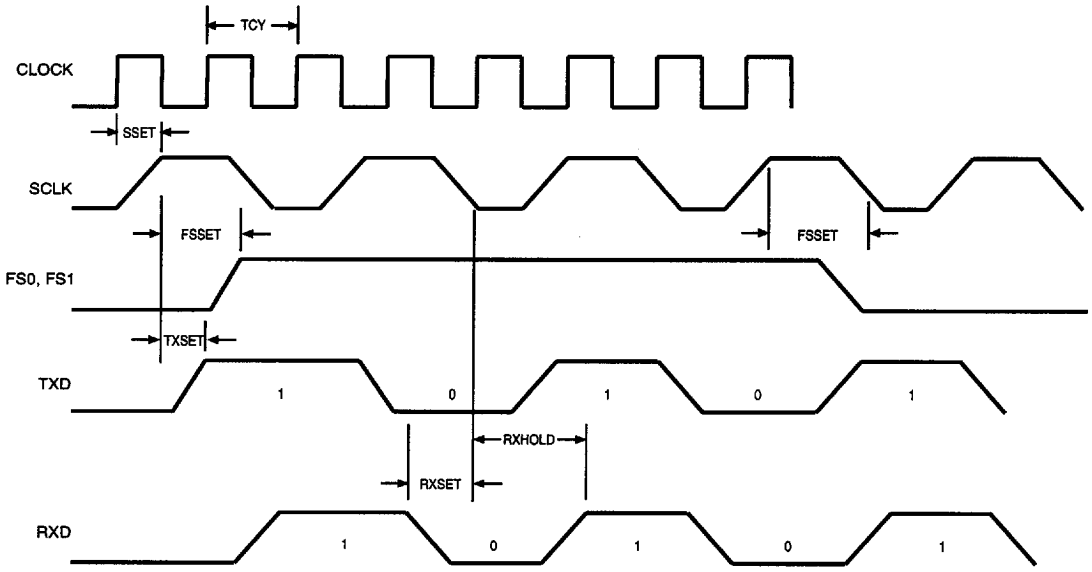


Figure 29. CODEC Interface Timing

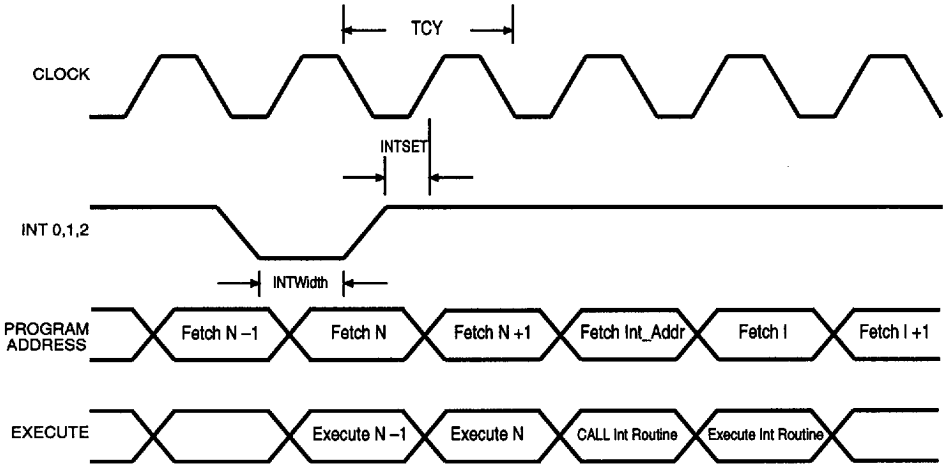


Figure 30. Interrupt Timing

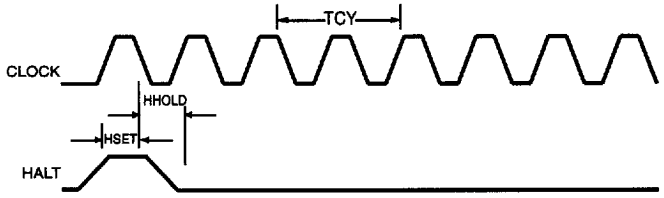
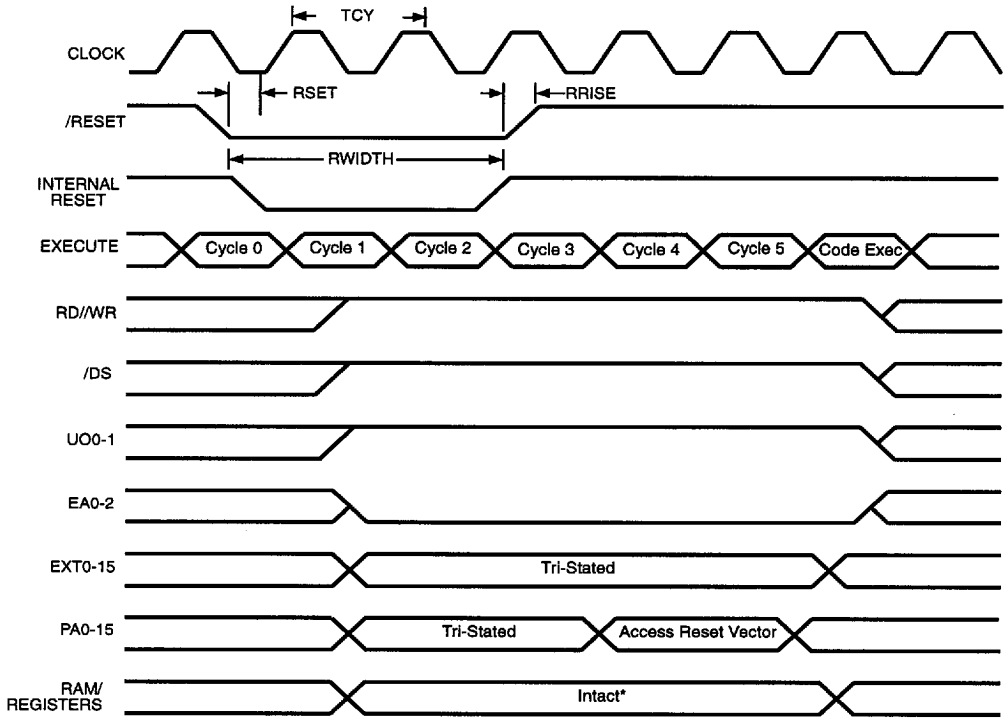


Figure 31. HALT Timing

TIMING DIAGRAMS (Continued)



* The RAM and hardware registers are left intact during a warm reset. A cold reset will produce random data in these locations. The status register is set to zeroes in both cases.

Figure 32. RESET Timing

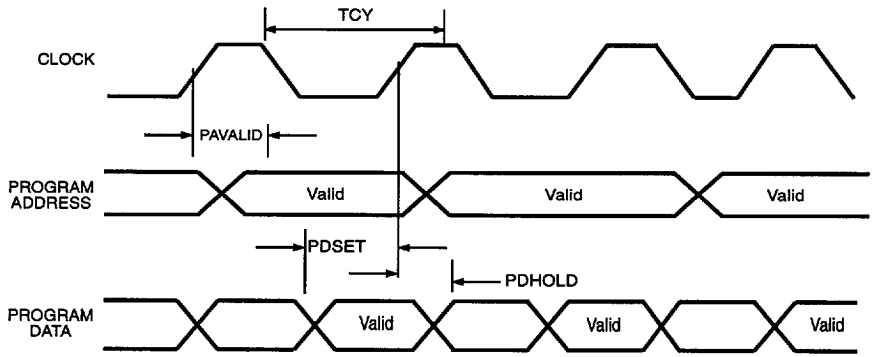
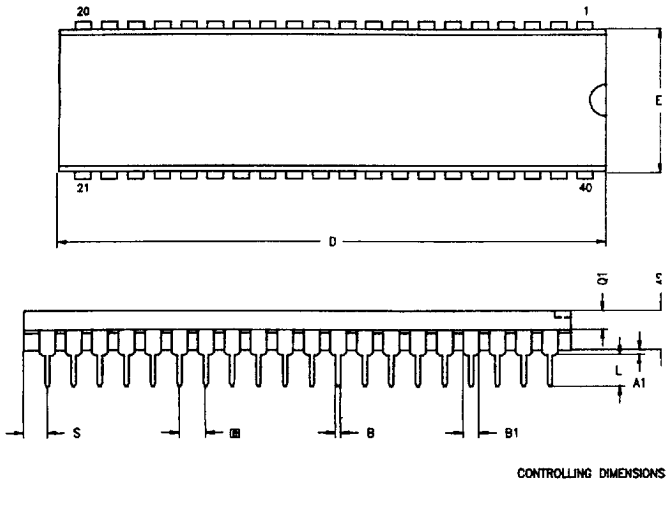


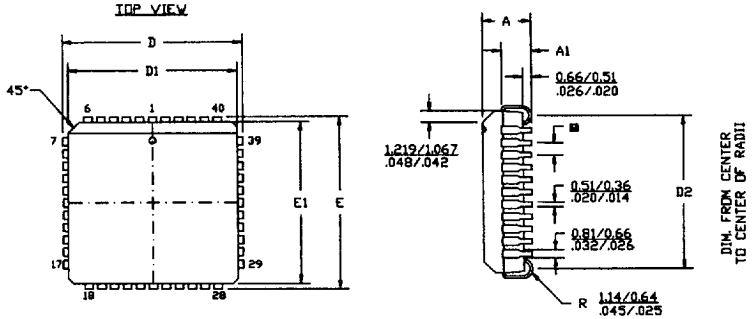
Figure 33. External Program Memory Port Timing

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

40-Pin DIP Package Diagram

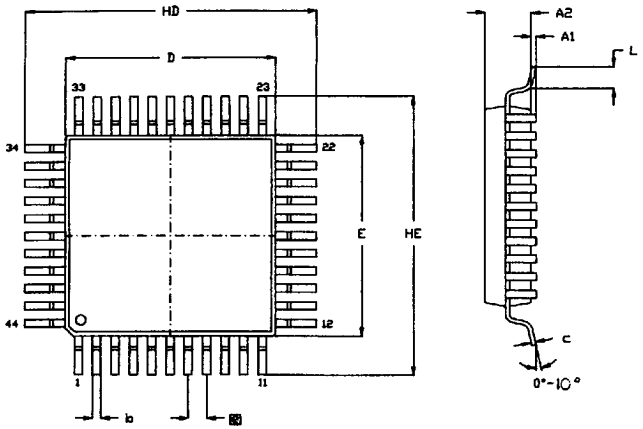


NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.41	2.92	.095	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

44-Pin PLCC Package Diagram

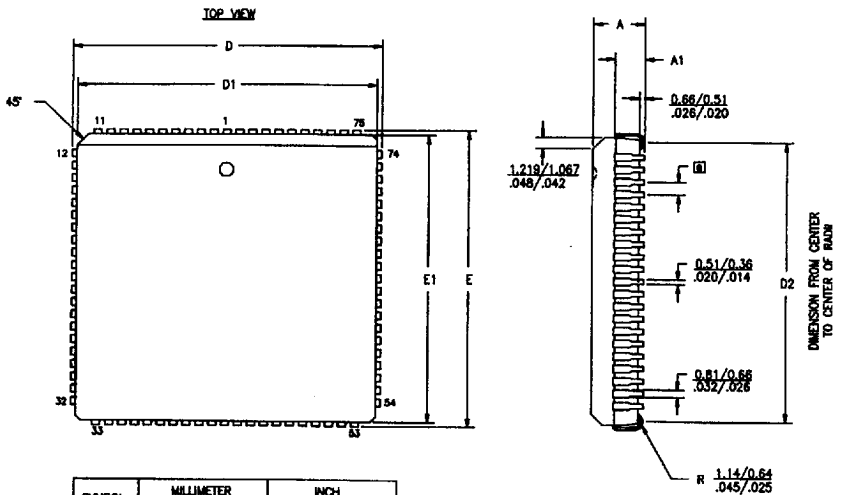
PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.076	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
e	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 (.004")

44-Pin QFP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.43	2.92	.095	.115
D/E	30.10	30.35	1.185	1.195
D1/E1	29.21	29.41	1.150	1.158
D2	27.94	28.58	1.100	1.125
e	1.27 TYP		.050 TYP	

NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN RANGE.
3. DIMENSION : MM / INCH

84-Pin PLCC Package Diagram

ORDERING INFORMATION

Z89321	Z89371	Z89391
20 MHz 44-Pin PLCC Z8932120VSC	**16 MHz** 44-pin PLCC Z8937116VSC	**20 MHz** 84-Pin PLCC Z8939120VSC
20 MHz 40-Pin DIP Z8932120PSC	**16 MHz** 40-pin DIP Z8937116PSC	
20 MHz 44-Pin QFP Z8932120FSC	**16 MHz** 44-pin QFP Z8937116FSC	
10 MHz 40-Pin PLCC Z8932110VSC	**10 MHz** 40-pin PLCC Z8937110VSC	**10 MHz** 84-Pin PLCC Z8939110VSC
10 MHz 40-Pin DIP Z8932110PSC	**10 MHz** 40-pin DIP Z8937110PSC	
10 MHz 44-Pin QFP Z8932110FSC	**10 MHz** 44-pin QFP Z8937110FSC	

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
P= Plastic DIP
V = Plastic PLCC
F = Plastic QFP

Temperature
S = 0°C to +70°C

Speed
20 = 20 MHz
16 = 16 MHz

Environmental
C = Plastic Standard

Example:

Z 89321 20 V S C is a Z89321, 20 MHz, PLCC, 0°C to +70°C, Plastic Standard Flow