Z89332/36
DIGITAL TELEVISION CONTROLLER

FEATURES

Part Number	ROM (Kbyte)	RAM* (Bytes)	Speed (MHz)
Z89332	24	640	12
Z89336	12	640	12

  *General-Purpose
- 42-Pin SDIP and 48-Pin Ceramic Packages with 42- to 48-Pin Adapter Socket
- 4.75- to 5.25-Volt Operating Range
- 0°C to +70°C Temperature Range
- Fully-Customized Character Set
- Character Control and Closed Caption Modes
- Keypad User Control
- TV Tuner Serial Interface
- Direct Video Signals

GENERAL DESCRIPTION

The Z89332/36 Digital Television Controllers are designed to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities. The Television Controllers feature a Z89C00 RISC processor core that controls the on-board peripheral functions and registers using the standard processor instruction set.

Character attributes can be controlled through two modes: the on-screen display Character Control Mode and the Closed Caption Mode. The Character Control Mode provides access to the full set of attribute controls, allowing the modification of attributes on a character-by-character basis. The insertion of control characters permits direction of other character attributes. Closed caption text can be decoded directly from the composite video signal and displayed on-screen with the assistance of the processor's digital signal processing (DSP) capabilities.

The fully customized 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes that include underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency.

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices, such as digital channel tunning adjustments, may be accessed through the industry-standard I^2C port.

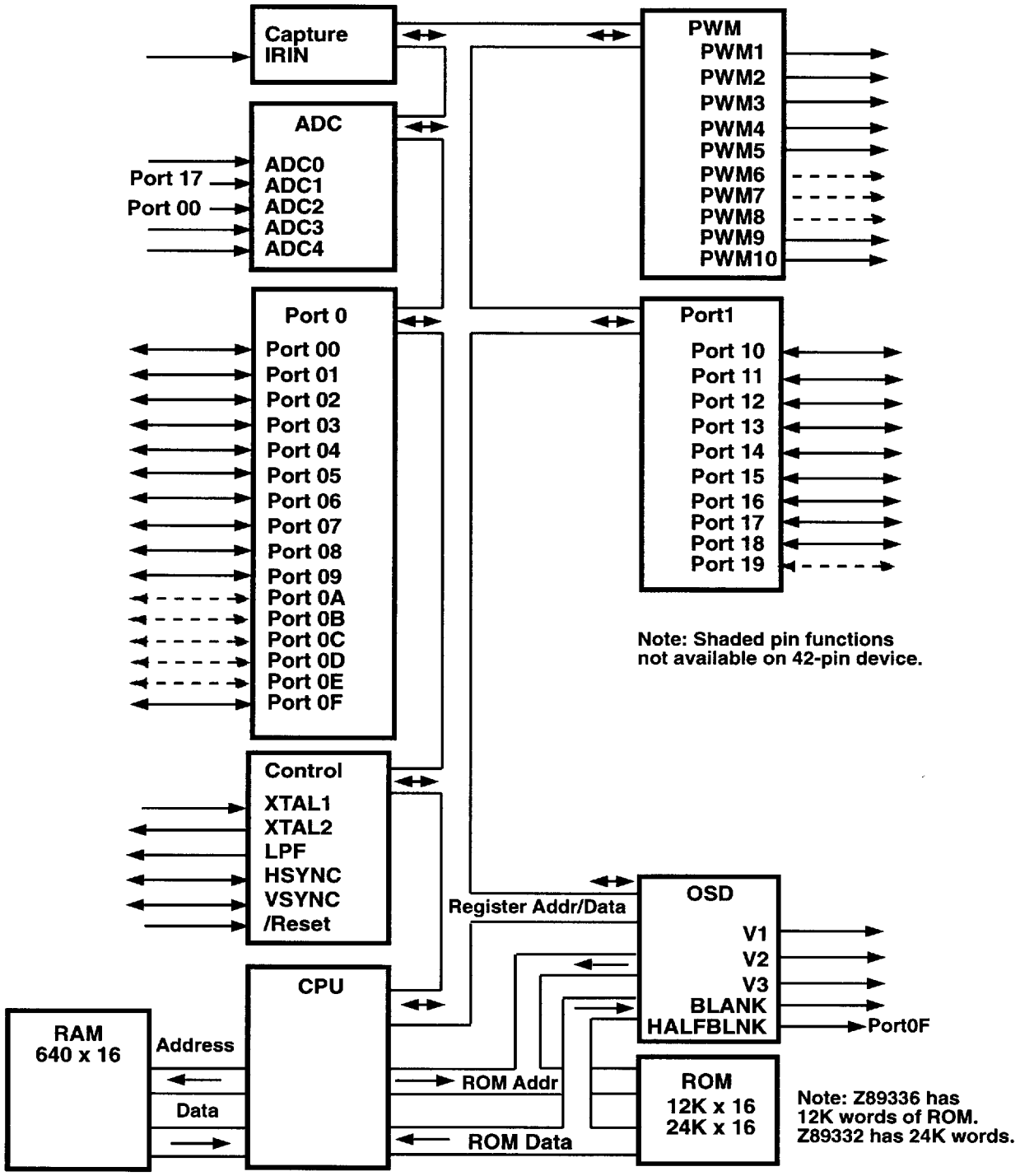
User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register. Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

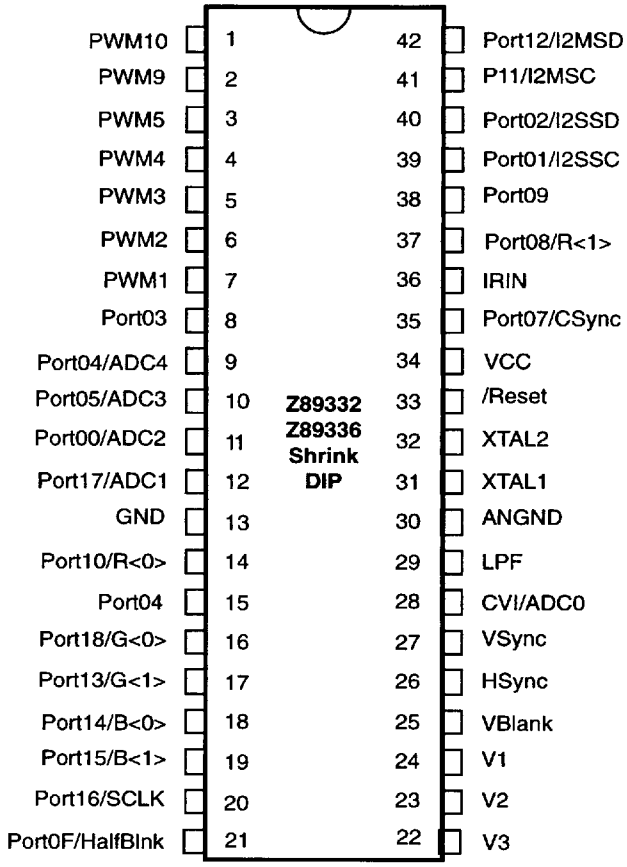
Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)



Functional Block Diagram



42-Pin Shrink DIP and
48-Pin Ceramic Pin Configurations
with 42- to 48-Pin Adapter Footprint

PIN IDENTIFICATION

42-Pin SDIP

Name	Function	Z89331/6	Direction	Reset
V_{CC}	+ 5 Volts	34	PWR	–
GND	0 Volts	13,30	PWR	–
IRIN	Infrared Remote Capture Input	36	I	I
ADC[5:0]	4-Bit A/D Converter Input	–,9,10,11,12,28	AI	I
PWM10, PWM9	14-Bit Pulse Width Modulator Output	1,2	O	O
PWM[8:1][a]	8-Bit Pulse Width Modulator Output	–,–,–,3,4,5,6,7	OD	O
Port0[F:0][b]	Bit Programmable Input/Output Ports	21,–,–,–,–,–,38,37, 35,–,–,15,8,40,39,11	B	I
Port1[9:0][c]	Bit Programmable Input/Output Ports	–,16,12,20,19,18,17, 42,41,14	B	I
SCL[d]	I²C Clock I/O	39 or 41	BOD	
SCD[e]	1²C Data I/O	40 or 42	BOD	
XTAL1	Crystal Oscillator Input	31	AI	I
XTAL2	Crystal Oscillator Output	32	AO	O
LPF	Loop Filter	29	AB	O
HSYNC	H_SYNC	26	B	I
VSYNC	V_SYNC	27	B	I
/Reset	Device Reset	33	I	I
V[3:1]	OSD Video Output Typically Drive B, G, and R Outputs	22,23,24	O	O
Blank	OSD Blank Output	25	O	O
HalfBlank[f]	OSD Half-Blank Output	21	O	
RGB Digital Outputs[g]	R[1:0], G[1:0], and B[1:0] Outputs of the RGB Matrix	37,14,17,16,19,18	O	
SCLK[h]	Internal Processor SCLK	20	O	

Notes:

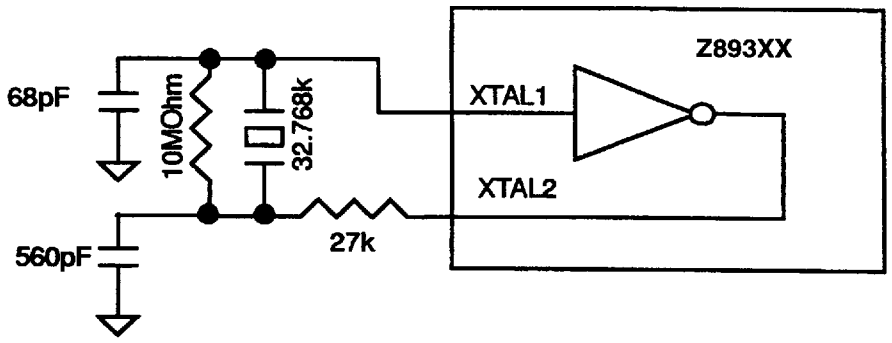
a) PWM[8,7] is not available on the 42-pin SDIP version.
b) Port0[F:A] is not available on the 42-pin SDIP version.
c) Port19 is not available on the 42-pin SDIP version.
d) SCL I/O pin is shared with Port0 or Port11.
e) SCD I/O pin is shared with Port02 or Port12.
f) Half Blank output is a function shared with Port0F.
Half Blank output is not available on the 42-pin SDIP version.
g) Digital RGB outputs and the internal SCLK are shared with Port1[5:0].
h) Internal processor SCLK is shared with Port16.

V1, V2, V3 ANALOG OUTPUT
Specifications V_{CC} = 5.25 V

V_{CC} = 5.25 V	Condition	Limit
Output Voltage	Bit = 11 Bit = 10	4.55 V +/– 0.25 V 3.205V +/– 0.2 V
	Bit = 01 Bit = 00	1.95 V +/– 0.15 V 0.65 V +/– 0.1 V
Settling Time	70% of DC Level, 10pf Load	< 50 nsec

V1, V2, V3 ANALOG OUTPUT
Specifications V_{CC} = 4.75V

V_{CC} = 4.75V	Condition	Limit
Output Voltage	Bit = 11 Bit = 10	3.90 V +/– 0.25 V 2.90 V +/– 0.2 V
	Bit = 01 Bit = 00	1.90 V +/– 0.15 V 0.1 V +/– 0.1 V
Settling Time	70% of DC Level, 10pf Load	< 50 nsec



32K Oscillator Recommended Circuit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	Conditions
V_{CC}	Power Supply Voltage	0	7	V	
V_{ID}	Input Voltage	–0.3	V_{CC} +0.3	V	Digital Inputs
V_{IA}	Input Voltage	–0.3	V_{CC} +0.3	V	Analog Inputs (A/D0...A/D4)
V_O	Output Voltage	–0.3	V_{CC} +0.3	V	All Push-Pull Digital Output
V_O	Output Voltage	–0.3	V_{CC} +8.0	V	Open-Drain PWM Outputs (PWM1...PWM8)
V_O	Output Voltage	–0.3	V_{CC} +0.3	V	Open-Drain PWM Outputs (PWM1...PWM8) - Z89332BA
I_{OH}	Output Current High		–10	mA	One Pin
I_{OH}	Output Current High		–100	mA	All Pins
I_{OL}	Output Current Low		20	mA	One Pin
I_{OL}	Output Current Low		200	mA	All Pins
T_A	Operating Temperature	0	70	°C	
T_A	Storage Temperature	–65	150	°C	

DC CHARACTERISTICS

T_A = 0°C to + 70°C; V_{CC} = 4.5 V to + 5.5 V; F_{OSC} = 32.768 KHz

Symbol	Parameter	Min	Max	Typical	Units	Conditions
V_{IL}	Input Voltage Low	0	0.2 V_{CC}	0.4	V	
V_{IH}	Input Voltage High	0.6 V_{CC}	V_{CC}	3.6	V	
V_{PU}	Max. Pull-Up Voltage		12		V	PWM0...PWM8 Only
V_{OL}	Output Voltage Low		0.4	0.16	V	@ I_{OL} = 1 mA
V_{OL}	Output Voltage High	V_{CC} –0.9		4.75	V	@ I_{OL} = 0.75 mA
V_{XL}	Input Voltage XTAL1 Low		0.3 V_{CC}	1.0	V	External Clock
V_{XH}	Input Voltage XTAL1 High	V_{CC} –2.0		3.5	V	Generator Driven
V_{HY}	Schmitt Hysteresis	3.0	0.75	0.5	V	On XTAL1 Input Pin
I_{IR}	Reset Input Current		150	90	µA	V_{RL} = 0 V
I_{IL}	Input Leakage	–3.0	3.0	0.01	µA	@ 0 V and V_{CC}
I_{CC}	Supply Current		100	60	mA	
I_{CC1E}	Supply Current of the OTP		700	300	µA	Sleep Mode @ 32 KHz
I_{CC1}	Supply Current		300	100	µA	Sleep Mode @ 32 KHz
I_{CC2}	Supply Current		10	5	µA	Sleep Mode

AC CHARACTERISTICS

T_A = 0°C to + 70°C; V_{CC} = 4.5 V to 5.5 V; F_{OSC} = 32.768 KHz

Symbol	Parameter	Min	Max	Typical	Units
T_PC	Input Clock Period	16	100	32	µS
T_RC, T_FC	Clock Input Rise and Fall			12	µS
T_DPOR	Power On Reset Delay	0.8		1.2	s

AC CHARACTERISTICS

T_A = 0°C to + 70°C; V_{CC} = 4.5 V to 5.5 V; F_{OSC} = 32.768 KHz

Symbol	Parameter	Min	Max	Typical	Units
T_WRES	Power-On Reset Min. Width		5TPC		µS
T_DH_S	H_Sync Incoming Signal Width	5.5	12.5	11	µS
T_DV_S	V_Sync Incoming Signal Width	0.15	1.5	1.0	mS
T_DE_S	Time Delay Between Leading Edge of V_Sync and H_Sync in Even Field	–12	+12	0	µS
T_DO_S	Time Delay Between Leading Edge of H_Sync in Odd Field	20	44	32	µS
T_WHV_S	H_Sync/V_Sync Edge Width		2.0	0.5	µS

Notes:
All timing of the I²C bus interface are defined by related specifications of the I²C bus interface.

Development Projects:
Customer is cautioned that while reasonable efforts will be employed to meet performance objectives and milestone dates, development is subject to unanticipated problems and delays. No production release is authorized or committed until the Customer and Zilog have agreed upon a Customer Procurement Specification for this project.

Pre-Characterization Product:
The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
Telex 910-338-7621
FAX 408 370-8056
Internet: http://www.zilog.com