PRODUCT SPECIFICATION

Z80180/Z8S180*

Z180® MICROPROCESSOR (*Z8S180 - PRELIMINARY)

FEATURES

- Z80180 Supports Operating Frequency to 10 MHz
- Z8S180 Supports Operating Frequency to 20 MHz
- On-Chip MMU Supports Extended Address Space
- Two DMA Channels
- On-Chip Wait State Generators
- Two UART Channels
- Two 16-Bit Timer Channels
- On-Chip Interrupt Controller
- On-Chip Clock Oscillator/Generator
- Clocked Serial I/O Port
- CPU Control Register (Z8S180 only) provides:
  - Programmable execution speed (to 20 MHz)
  - Programmable EMI noise reduction
  - Reduced operating current (to 20% of Z80180)
  - Fully static operation - low STANDBY current (10 µA max.)
- Code Compatible with Zilog Z80 CPU Extended Instructions
- 6 MHz Version Supports 6.144 MHz CPU Clock Operation.

GENERAL DESCRIPTION

Based on a microcoded execution unit and an advanced CMOS manufacturing technology, the Z80180 is an 8-bit MPU which provides the benefits of reduced system costs and low power operation while offering higher performance and maintaining compatibility with a large base of industry standard software written around the Zilog Z80® CPU.

The Z8S180 is a fully static version of Z80180 which provides complete software and hardware compatibility to the Z80180 as well as enhancements for doubling execution speeds, power savings and EMI noise reduction.

Higher performance is obtained by virtue of higher operating frequencies, reduced instruction execution times, an enhanced instruction set, and an on-chip memory management unit (MMU) with the capability of addressing up to 1 Mbyte of memory.

Reduced system costs are obtained by incorporating several key system functions on-chip with the CPU. These key functions include I/O devices such as DMA, UART, and timer channels. Also included on-chip are several "glue" functions such as dynamic RAM refresh control, wait state generators, clock oscillator, and interrupt controller.

Not only does the Z80180 consume a low amount of power during normal operation, but it also provides two operating modes that are designed to drastically reduce the power consumption even further. The SLEEP mode reduces power by placing the CPU into a "stopped" state, thereby consuming less current, while the on-chip I/O device is still operating. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a "stopped" mode, thereby reducing power consumption even further.

In addition to the two operating modes offered by the Z80180, the Z8S180 provides a STANDBY mode. The STANDBY mode consumes less than 10 µA by stopping the external oscillators and internal clock.

When combined with other CMOS VLSI devices and memories, the Z80180 provides an excellent solution to system applications requiring high performance, and low power operation.

For the rest of this document, descriptions of Z180 operation applies to both Z80180 and Z8S180.

GENERAL DESCRIPTION (Continued)

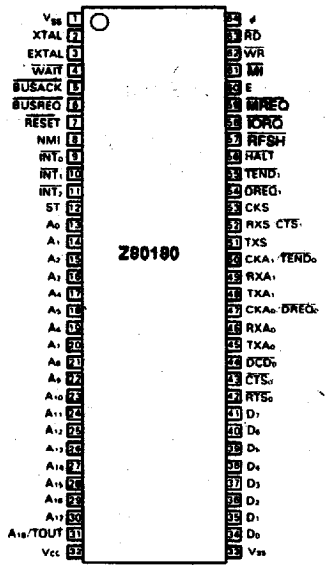


Figure 1a. Z80180 64-Pin DIP

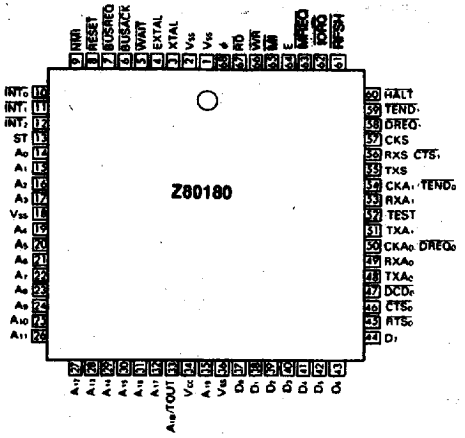


Figure 1b. Z80180 68-Pin PLCC

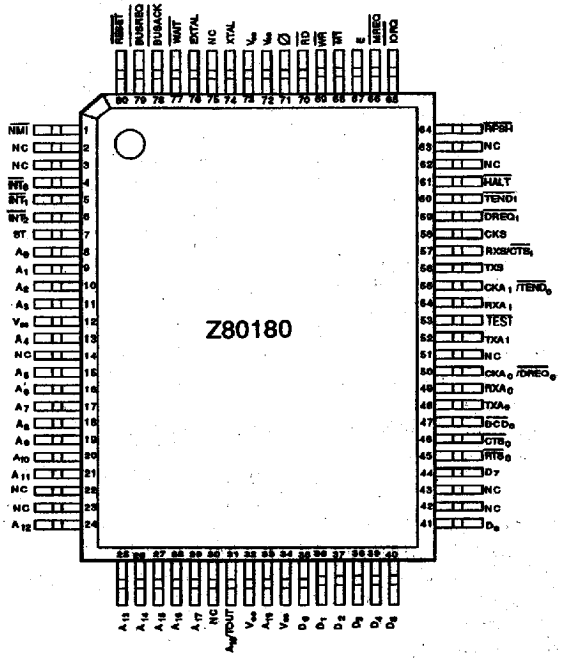


Figure 1c. Z80180 80-Pin QFP

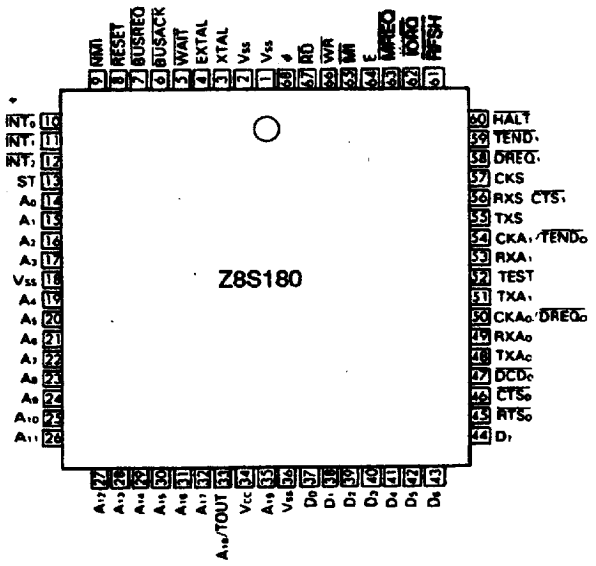


Figure 2a. Z8S180 68-Pin PLCC

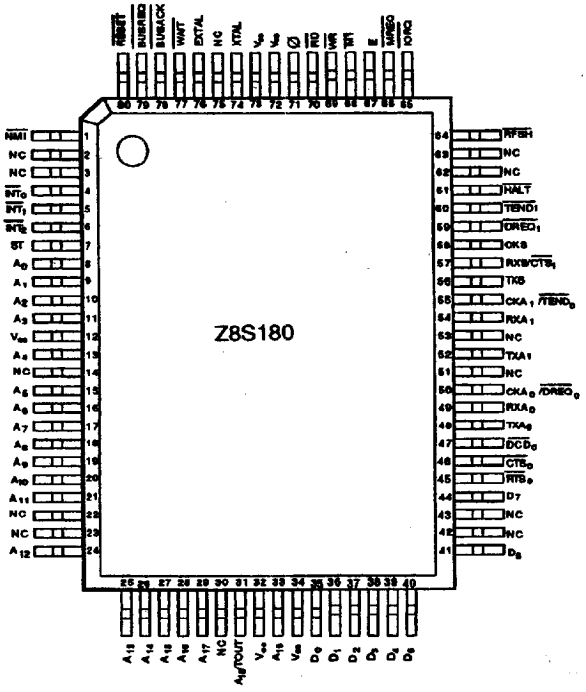


Figure 2b. Z8S180 80-Pin QFP

GENERAL DESCRIPTION (Continued)

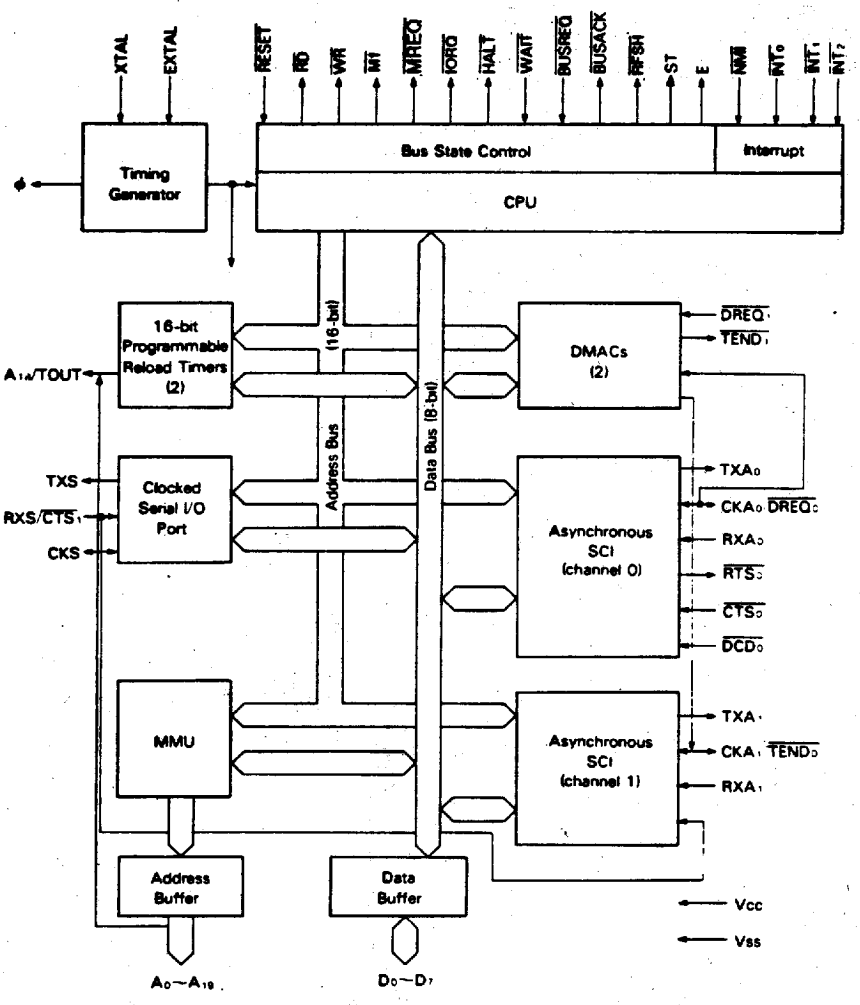


Figure 3. Z80180 Block Diagram

Note:
The Z8S180 contains an additional control register. For details see I/O Register Section.

PIN DESCRIPTION:

A_0-A_{19}. *Address Bus (Output, active High, 3-state).* A_0-A_{19} form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges, up to 1 Mbyte, and I/O data bus exchanges, up to 64K. The address bus enters a high impedance state during reset and external bus acknowledge cycles. Address line A_{18} is multiplexed with the output of PRT channel 1 (TOUT, selected as address output on reset) and address line A_{19} is not available in DIP versions of the Z80180.

$\overline{BUSACK}$. *Bus Acknowledge (Output, active Low).* $\overline{BUSACK}$ indicates the requesting device, the MPU address and data bus, and some control signals, have entered their high impedance state.

$\overline{BUSREQ}$. *Bus Request (Input, active Low).* This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle. This signal will stop the CPU from executing further instructions and places the address and data buses, and other control signals, into the high impedance state.

CKA_0, CKA_1. *Asynchronous Clock 0 and 1 (Bidirectional, active High).* These pins are the transmit and receive clocks for the synchronous channels. CKA_0 is multiplexed with $\overline{DREQ_0}$ and CKA_1 is multiplexed with $\overline{TEND_0}$.

CKS. *Serial Clock (Bidirectional, active High).* This line is clock for the CSIO channel.

CLOCK. *System Clock (Output, active High).* The output is used as a reference clock for the MPU and the external system. The frequency of this output is equal to one-half that of the crystal or input clock frequency.

$\overline{CTS_0}$-$\overline{CTS_1}$. *Clear to Send 0 and 1 (Inputs, active Low).* These lines are modem control signals for the ASCI channels. $\overline{CTS1}$ is multiplexed with RXS.

D_0-D_7. *Data Bus (Bidirectional, active High, 3-state).* D_0-D_7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during reset and external bus acknowledge cycles.

$\overline{DCD_0}$. *Data Carrier Detect 0 (Input, active Low).* This is a programmable modem control signal for ASCI channel 0.

$\overline{DREQ_0}$, $\overline{DREQ_1}$. DMA Request 0 and 1 (Input, active Low). $\overline{DREQ}$ is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a read or write operation. These inputs can be programmed to be either level or edge sensed. $\overline{DREQ_0}$ is multiplexed with CKA_0.

E. *Enable Clock (Output, active High).* Synchronous machine cycle clock output during bus transactions.

EXTAL. *External Clock/Crystal (Input, active High).* Crystal oscillator connection. An external clock can be input to the Z80180 on this pin when a crystal is not used. This input is Schmitt triggered.

$\overline{HALT}$. *Halt/Sleep Status (Output, active Low).* This output is asserted after the CPU has executed either the HALT or SLP instruction, and is waiting for either non-maskable or maskable interrupt before operation can resume. It is also used with the $\overline{M1}$ and ST signals to decode status of the CPU machine cycle.

$\overline{INT_0}$. *Maskable Interrupt Request 0 (Input, active Low).* This signal is generated by external I/O devices. The CPU will honor this request at the end of the current instruction cycle as long as the $\overline{NMI}$ and $\overline{BUSREQ}$ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the $\overline{M1}$ and $\overline{IORQ}$ signals will become active.

$\overline{INT_1}$, $\overline{INT_2}$. *Maskable Interrupt Requests 1 and 2 (Inputs, active Low).* This signal is generated by external I/O devices. The CPU will honor these requests at the end of the current instruction cycle as long as the $\overline{NMI}$, $\overline{BUSREQ}$, and $\overline{INT_0}$ signals are inactive. The CPU will acknowledge these interrupt requests with an interrupt acknowledge cycle. Unlike the acknowledgement for $\overline{INT_0}$, during this cycle neither the $\overline{M1}$ or $\overline{IORQ}$ signals will become active.

$\overline{IORQ}$. *I/O Request (Output, active Low, 3-state).* $\overline{IORQ}$ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. $\overline{IORQ}$ is also generated, along with $\overline{M1}$, during the acknowledgement of the $\overline{INT_0}$ input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the $\overline{IOE}$ signal of the Z64180.

$\overline{M1}$. *Machine Cycle 1 (Output, active Low).* Together with $\overline{MREQ}$, $\overline{M1}$ indicates that the current cycle is the opcode fetch cycle of an instruction execution. Together with $\overline{IORQ}$, $\overline{M1}$ indicates that the current cycle is for an interrupt acknowledge. It is also used with the $\overline{HALT}$ and ST signal to decode status of the CPU machine cycle. This signal is analogous to the $\overline{LIR}$ signal of the Z64180.

$\overline{MREQ}$. *Memory Request (Output, active Low, 3-state).* $\overline{MREQ}$ indicates that the address bus holds a valid address for a memory read or memory write operation. This signal is analogous to the $\overline{ME}$ signal of the Z64180.

$\overline{NMI}$. *Non-maskable Interrupt (Input, negative edge triggered).* $\overline{NMI}$ has a higher priority than $\overline{INT}$ and is always recognized at the end of an instruction, regardless of the state of the interrupt enable flip-flops. This signal forces CPU execution to continue at location 0066H.

$\overline{RD}$. *Read (Output, active Low, 3-state).* $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

$\overline{RFSH}$. *Refresh (Output, active Low).* Together with $\overline{MREQ}$, $\overline{RFSH}$ indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low order 8 bits of the address bus (A_7-A_0) contain the refresh address.

This signal is analogous to the $\overline{REF}$ signal of the Z64180.

$\overline{RTS_0}$. *Request to Send 0 (Output, active Low).* This is a programmable modem control signal for ASCI channel 0.

RXA_0, RXA_1. *Receive Data 0 and 1 (Inputs, active High).* These signals are the receive data to the ASCI channels.

RXS. *Clocked Serial Receive Data (Input, active High).* This line is the receiver data for the CSIO channel. RXS is multiplexed with the $\overline{CTS1}$ signal for ASCI channel 1.

ST. *Status (Output, active High).* This signal is used with the $\overline{M1}$ and $\overline{HALT}$ output to decode the status of the CPU machine cycle.

Note that the output from M1 is affected by the status of the M1E bit in OMCR register. Table 1 shows the status while M1E = 1.

ST	$\overline{HALT}$	$\overline{M1}$	Operation
0	1	0	CPU operation (1st op-code fetch)
1	1	0	CPU operation (2nd op-code and 3rd op-code fetch)
1	1	1	CPU operation (MC except for op-code fetch)
0	X	1	DMA operation
0	0	0	HALT mode
1	0	1	SLEEP mode (including SYSTEM STOP mode)

NOTE X: Don't care
MC: Machine cycle

Table 1. Status Summary

$\overline{TEND_0}$, $\overline{TEND_1}$. *Transfer End 0 and 1 (Outputs, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{TEND_0}$ in multiplexed with CKA_1.

TEST (Output): This pin is for test and is left open.

TOUT. *Timer Out (Output, active High).* TOUT is the pulse output from PRT channel 1. This line is multiplexed with A_{18} of the address bus.

TXA_0, TXA_1. *Transmit Data 0 and 1 (Outputs, active High).* These signals are the transmitted data from the ASCI channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS. *Clocked Serial Transmit Data (Output, active High).* This line is the transmitted data from the CSIO channel.

$\overline{WAIT}$. *Wait (Input, active Low).* $\overline{WAIT}$ indicates to the MPU that the addressed memory or I/O devices are not ready for a data transfer. This input is used to induce additional clock cycles into the current machine cycle. The $\overline{WAIT}$ input is sampled on the falling edge of T_2 (and subsequent wait states). If the input is sampled low, then additional wait states are inserted until the $\overline{WAIT}$ input is sampled high, at which time execution will continue.

$\overline{WR}$. *Write (Output, active Low, 3-state).* $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL. *Crystal (Input, active High).* Crystal oscillator connection. This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (reference DC characteristics).

Multiplexed pin descriptions

$A_{18}/\overline{TOUT}$ — During RESET, this pin is initialized as A_{18} pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, TOUT function is selected. If TOC1 and TOC0 bits are cleared to 0, A_{18} function is selected.

$CKA_0/\overline{DREQ_0}$ — During RESET, this pin is initialized as CKA_0 pin. If either DM1 or SM1 in DMA Mode Register (DMODE) is set to 1, $\overline{DREQ_0}$ function is always selected.

$CKA_1/\overline{TEND_0}$ — During RESET, this pin is initialized as CKA_1 pin. If CKA1D bit in ASCI control register ch 1 (CNTLA1) is set to 1, $\overline{TEND_0}$ function is selected. If CKA1D bit is set to 0, CKA_1 function is selected.

$RXS/\overline{CTS_1}$ — During RESET, this pin is initialized as RXS pin. If CTS1E bit in ASCI status register ch1 (STAT1) is set to 1, $\overline{CTS_1}$ function is selected. If CTS1E bit is set to 0, RXS function is selected.

ARCHITECTURE:

The Z180 combines a high performance CPU core with a variety of system and I/O resources useful in a broad range of applications. The CPU core consists of five functional blocks: clock generator, bus state controller (including dynamic memory refresh), interrupt controller, memory management unit (MMU), and the central processing unit (CPU). The integrated I/O resources make up the remaining four functional blocks: direct memory access (DMA) control (2 channels), asynchronous serial communications interface (ASCI, 2 channels), programmable reload timers (PRT, 2 channels), and a clock serial I/O (CSIO) channel.

Clock Generator. This logic generates the system clock from either an external crystal or clock input. The external clock is divided by two and provided to both internal and external devices.

Bus State Controller. This logic performs all of the status and bus control activity associated with both the CPU and some on-chip peripherals. This includes wait state timing, reset cycles, DRAM refresh, and DMA bus exchanges.

Interrupt Controller. This block monitors and prioritizes the variety of internal and external interrupts and traps to provide the correct responses from the CPU. To remain compatible with the Z80 CPU, three different interrupt modes are supported.

Memory Management Unit. The MMU allows the user to "map" the memory used by the CPU (logically only 64K) into the 1M Byte addressing range supported by the Z180. The organization of the MMU object code compatibility with the Z80 CPU while offerring access to an extended memory space. This is accomplished by using an effective "common area - banked area" scheme.

Central Processing Unit. The CPU is microcoded to provide a core that is object code compatible with the Z80 CPU. It also provides a superset of the Z80 instruction set, including 8-bit multiply and divide. This core has been enhanced to allow many of the instructions to execute in fewer clock cycles.

DMA Controller. The DMA controller provides high speed transfers between memory and I/O devices. Transfer operations supported are memory to memory, memory to/from I/O, and I/O to I/O. Transfer modes supported are request, burst, and cycle steal. DMA transfers can access the full 1 Mbyte addressing range with a block length up to 64K bytes, and can cross over 64K boundaries.

Asynchronous Serial Communications Interface (ASCI). The ASCI logic provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels can also support a multiprocessor communications format.

Programmable Reload Timer (PRT). This logic consists of two separate channels, each containig a 16-bit counter (timer) and count reload register. The time base for the counters is derived from the system clock (divided by 20) before reaching the counter. PRT channel 1 provides an optional output to allow for waveform generation.

Clocked Serial I/O (CSIO). The CSIO channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer.

OPERATION MODES:

The Z180 can be configured to operate like the 64180. This is accomplished by allowing the user to have control over the $\overline{M1}$, $\overline{IORQ}$, $\overline{WR}$, and $\overline{RD}$ signals. The Operation Mode Control Register (OMCR) determines the $\overline{M1}$ options; the timing of the $\overline{IORQ}$, RD, and $\overline{WR}$ signals; and the RETI operation.

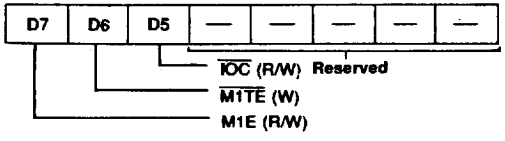


Figure 4. Operation Mode Control Register (I/O Address = 3 EH)

M1E ($\overline{M1}$ Enable): This bit controls the M1 output and is set to a 1 during reset.

When M1E=1, the $\overline{M1}$ output is asserted LOW during the opcode fetch cycle, the $\overline{INT0}$ acknowledge cycle, and the first machine cycle of the $\overline{NMI}$ acknowledge. This will also cause the $\overline{M1}$ signal to be active during both fetches of the RETI instruction sequence, which may cause corruption of the external interrupt daisy chain. Hence, this bit should be set to 0 for the Z180. When M1E=0, the $\overline{M1}$ output is normally inactive and asserted LOW only during the refetch of the RETI instruction sequence and during the $\overline{INT0}$ acknowledge cycle.

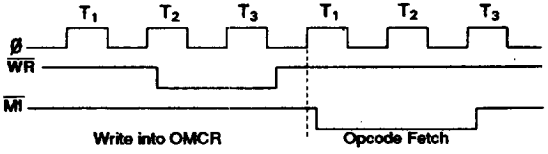


Figure 5. M1 Temporary Enable Timing

M1TE ($\overline{M1}$ Temporary Enable): This bit controls the temporary assertion of the $\overline{M1}$ signal. It is always read back as

a '1' and is set to 1 during reset. This function is used to "arm" the internal interrupt structure of the Z80PIO. When a control word is written to the Z80PIO to enable interrupts, no enable actually takes place until the PIO sees an active $\overline{M1}$ signal. When $\overline{M1TE}$=1, there is no change in the operation of the $\overline{M1}$ signal and M1E controls its function. When $\overline{M1TE}$=0, the $\overline{M1}$ output will be asserted during the next opcode fetch cycle regardless of the state programmed into the M1E bit. This is only momentary (one time) and the user need not reprogram a 1 to disable the function (See Figure 5).

$\overline{IOC}$: this bit controls the timing of the $\overline{IORQ}$ and $\overline{RD}$ signals. It is set to 1 by reset.

When $\overline{IOC}$=1, the $\overline{IORQ}$ and $\overline{RD}$ signals function the same as the Z64180.

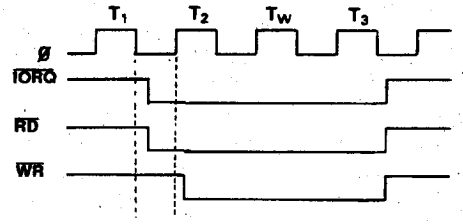


Figure 6. I/O Read and Write Cycles with $\overline{IOC}$ =1

When $\overline{IOC}$=0, the timing of the $\overline{IORQ}$ and $\overline{RD}$ signals match the timing required by the Z80 family of peripherals. The $\overline{IORQ}$ and $\overline{RD}$ signals will go active as a result of the rising edge of T2. This allows the Z180 to satisfy the setup times required by the Z80 peripherals on those two signals.

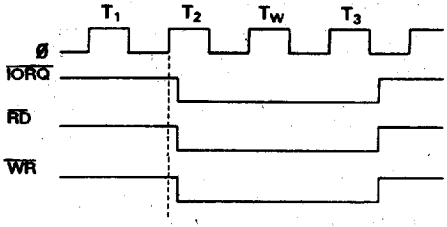


Figure 7. I/O Read and Write Cycles with $\overline{IOC}$ = 0

For the rest of this manual, it is assumed that M1E=0 and $\overline{IOC}$=0. The user must program the Operation Mode Control Register before the first I/O instruction is executed.

TIMING:

This section explains the Z180 CPU timing for the following operations:

- Instruction (op-code) fetch timing.
- Operand and data read/write timing.
- I/O read/write timing.
- Basic instruction (fetch and execute) timing.
- RESET timing.
- BUSREQ/BUSACK bus exchange timing.

The basic CPU operation consists of one or more "Machine Cycles" (MC). A machine cycle consists of three system clocks, T1, T2, and T3 while accessing memory or I/O, or it consists of one system clock (T1) during CPU internal operations. The system clock is half the frequency of the Crystal oscillator (e.g., an 8 MHz crystal produces 4 MHz or 250 nsec). For interfacing to slow memory or peripherals, optional wait states (Tw) may be inserted between T2 and T3.

Instruction (op-code) Fetch Timing. Fig. 8 shows the instruction (op-code) fetch timing with no wait states. An op-code fetch cycle is externally indicated when the $\overline{M1}$ output pin is LOW.

In the first half of T_1, the address bus (A_0-A_{19}) is driven from the contents of the Program Counter (PC). Note that this is the translated address output of the Z180 on-chip MMU.

In the second half of T_1, the $\overline{MREQ}$ (Memory Request) and $\overline{RD}$ (Read) signals are asserted LOW, enabling the memory.

The op-code on the data bus is latched at the rising edge of T_3 and the bus cycle terminates at the end of T_3.

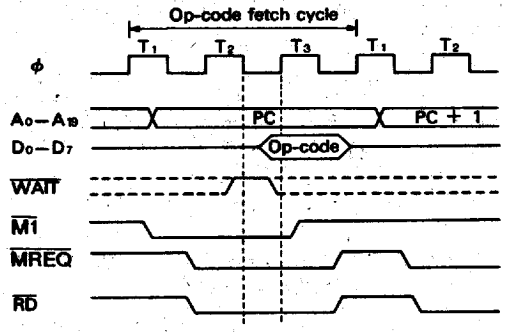


Figure 8. Opcode Fetch timing (Without Wait State)

Fig. 9 illustrates the insertion of wait states (Tw) into the op-code fetch cycle. Wait states (Tw) are controlled by the external $\overline{WAIT}$ input combined with an on-chip programmable wait state generator.

At the falling edge of T_2 the combined $\overline{WAIT}$ input is sampled. If $\overline{WAIT}$ input is asserted LOW, a wait state (Tw) is inserted. The address bus, $\overline{MREQ}$, $\overline{RD}$ and $\overline{MI}$ are held stable during wait states. When the WAIT is sampled inactive HIGH at the falling edge of Tw, the bus cycle enters T_3 and completes at the end of T_3.

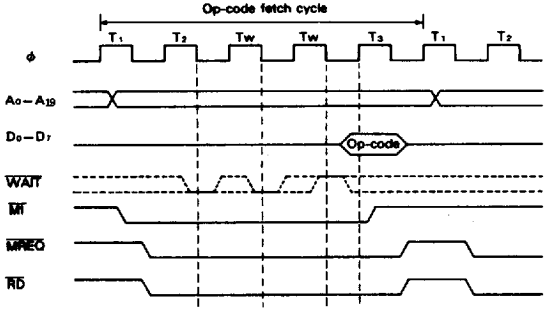


Figure 9. Opcode Fetch Timing (With Wait State)

Operand and Data Read/Write Timing. The instruction operand and data read/write timing differs from op-code fetch timing in two ways. First, the $\overline{MI}$ output is held inactive. Second, the read cycle timing is relaxed by one-half clock cycle since data is latched at the falling edge of T_3.

Instruction operands include immediate data, displacement, and extended addresses, and have the same timing as memory data reads.

During memory write cycles the $\overline{MREQ}$ signal goes active in the second half of T_1. At the end of T_1, the data bus is driven with the write data.

At the start of T_2, the $\overline{WR}$ signal is asserted LOW enabling the memory. $\overline{MREQ}$ and $\overline{WR}$ go inactive in the second half of T3 followed by disabling of the write data on the data bus.

Wait states (Tw) are inserted as previously described for op-code fetch cycles. Fig. 10 illustrates the read/write timing without wait states (Tw), while Fig. 11 illustrates read/write timing with wait states (Tw).

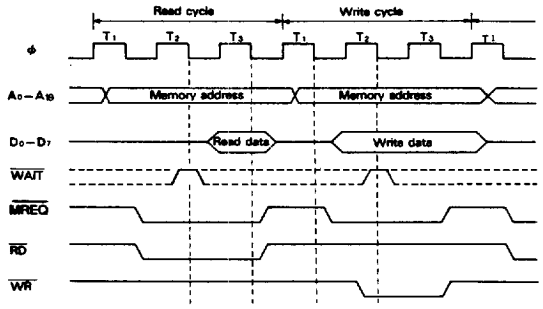


Figure 10. Memory Read/Write Timing (Without Wait State)

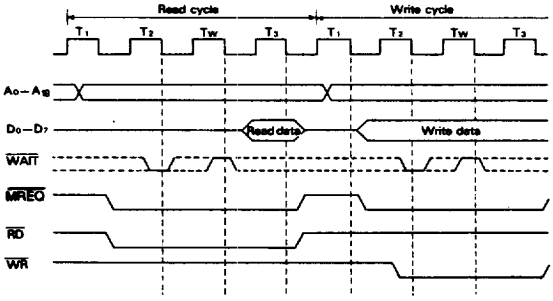


Figure 11. Memory Read/Write Timing (With Wait State)

I/O Read/Write Timing. I/O instructions cause data read/write transfers which differ from memory data transfers in the following three ways:

1. The $\overline{IORQ}$ (I/O Reguest) signal is asserted LOW instead of the $\overline{MREQ}$ signal.
2. The 16-bit I/O address is not translated by the MMU.
3. A_{16}-A_{19} are held LOW.

At least one wait state (Tw) is always inserted for I/O read and write cycles (except internal I/O cycles).

Fig. 12 shows I/O read/write timing with the automatically inserted wait state (Tw).

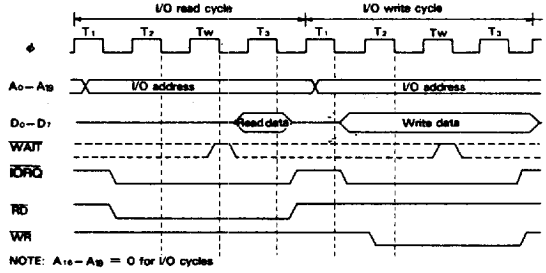


Figure 12. I/O Read/Write Timing

Basic Instruction Timing. An instruction may consist of a number of machine cycles including op-code fetch, operand fetch, and data read/write cycles. An instruction may also include cycles for internal processes which make the bus idle.

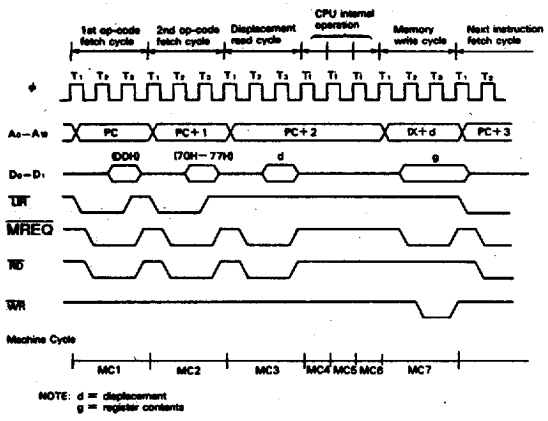


Figure 13. Instruction Timing

The example in Fig. 13 illustrates the bus timing for the data transfer instruction LD (IX+d),g. This instruction moves the contents of a CPU register (g) to the memory location with address computed by adding a signed 8-bit displacement (d) to the contents of an index register (IX).

The instruction cycle starts with the two machine cycles to read the two byte instruction op-code as indicated by $\overline{M1}$ LOW. Next, the instruction operand (d) is fetched.

The external bus is idle while the CPU computes the effective address. Finally, the computed memory location is written with the contents of the CPU register (g).

RESET Timing. Fig. 14 shows the Z180 hardware RESET timing. If the $\overline{RESET}$ pin is LOW for six or more than six clock cycles, processing is terminated and the Z180 restarts execution from (logical and physical) address 00000H.

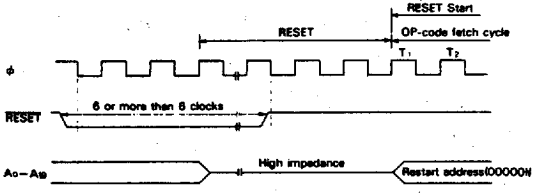


Figure 14. Reset Timing

$\overline{BUSREQ}$/$\overline{BUSACK}$ Bus Exchange Timing. The Z180 can coordinate the exchange of control, address and data bus ownership with another bus master. The alternate bus master can request the bus release by asserting the $\overline{BUSREQ}$ (Bus Request) input LOW. After the Z180 releases the bus, it relinquishes control to the alternate bus master by asserting the $\overline{BUSACK}$ (Bus Acknowledge) output LOW.

The bus may be released by the Z180 at the end of each machine cycle. In this context, a machine cycle consists of a minimum of 3 clock cycles (more if wait states are inserted) for op-code fetch, memory read/write, and I/O read/write cycles. Except for these cases, a machine cycle corresponds to one clock cycle.

When the bus is released, the address (A_0-A_{19}), data (D_0-D_7), and control ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$) signals are placed in the high impedance state.

Note that dynamic RAM refresh is not performed when the Z180 has released the bus. The alternate bus master must provide dynamic memory refreshing if the bus is released for long periods of time.

Fig. 15 illustrates $\overline{BUSREQ}$/$\overline{BUSACK}$ bus exchange during a memory read cycle. Fig. 16 illustrates bus exchange when the bus release is requested during a Z180 CPU internal operation. $\overline{BUSREQ}$ is sampled at the falling edge of the system clock prior to T_3, T_i and Tx (BUS RELEASE state). If $\overline{BUSREQ}$ is asserted LOW at the falling edge of the clock state prior to Tx, another Tx is executed.

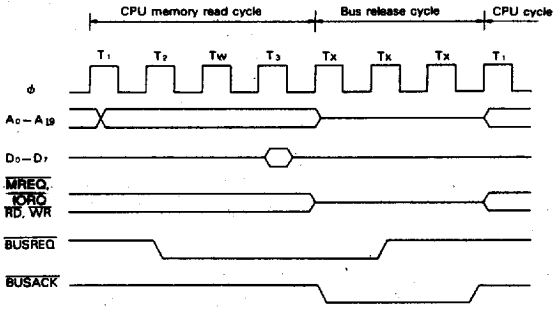


Figure 15. Bus Exchange Timing

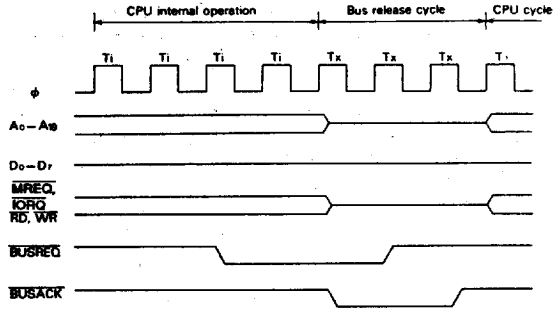


Figure 16. Bus Exchange Timing

WAIT State Generator

To ease interfacing with slow memory and I/O devices, the Z180 uses wait states (Tw) to extend bus cycle timing. A wait state(s) is inserted based on the combined (logical OR) state of the external $\overline{WAIT}$ input and an internal programmable wait state (Tw) generator. Wait states (Tw) can be inserted in both CPU execution and DMA transfer cycles.

When the external $\overline{WAIT}$ input is asserted LOW, wait state(s) (Tw) are inserted between T_2 and T_3 to extend the bus cycle duration. The $\overline{WAIT}$ input is sampled at the falling edge of the system clock in T_2 or Tw. If the $\overline{WAIT}$ input is asserted LOW at the falling edge of the system clock in Tw, another Tw is inserted into the bus cycle. Note that $\overline{WAIT}$ input transitions must meet specified set-up and hold times. This can easily be accomplished by externally synchronizing $\overline{WAIT}$ input transitions with the rising edge of the system clock.

Dynamic RAM refresh is not performed during wait states (Tw) and thus system designs which use the automatic refresh function must consider the affects of the occurrence and duration of wait states (Tw). Figure 17 shows WAIT timing.

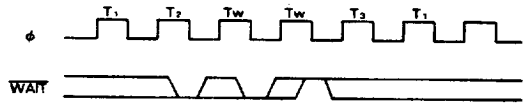


Figure 17. $\overline{WAIT}$ Timing

Programmable Wait State Insertion. In addition to the $\overline{WAIT}$ input, wait states (Tw) can also be inserted by program using the Z180 on-chip wait state generator. Wait state (Tw) timing applies for both CPU execution and on-chip DMAC cycles.

By programming the four significant bits of the DMA/WAIT Control Register (DCNTL) the number of wait states, (Tw) automatically inserted in memory and I/O cycles, can be separately specified.

HALT and Low Power Operation Modes

The Z180 can operate in 4 different modes. HALT mode, IOSTOP mode and 2 low power operation modes - SLEEP and SYSTEM STOP. Note that in all operating modes, the basic CPU clock (XTAL, EXTAL) must remain active.

HALT mode. HALT mode is entered by execution of the HALT instruction (op-code = 76H) and has the following characteristics.

(1) The internal CPU clock remains active.

(2) All internal and external interrupts can be received.

(3) Bus exchange ($\overline{BUSREQ}$ and $\overline{BUSACK}$) can occur.

(4) Dynamic RAM refresh cycle ($\overline{RFSH}$) insertion continues at the programmed interval.

(5) I/O operations (ASCI, CSI/O and PRT) continue.

(6) The DMAC can operate.

(7) The $\overline{HALT}$ output pin is asserted LOW.

(8) The external bus activity consists of repeated "dummy" fetches of the op-code following the HALT instruction.

Essentially, the Z180 operates normally in HALT mode, except that instruction execution is stopped.

HALT mode can be exited in the following two ways.

RESET Exit from HALT mode. If the $\overline{RESET}$ input is asserted LOW for at least 6 clock cycles, HALT mode is exited and the normal RESET sequence (restart at address 00000H) is initiated.

Interrupt Exit from HALT mode. When an internal or external interrupt is generated, HALT mode is exited and the normal interrupt response sequence is initiated.

If the interrupt source is masked (individually by enable bit, or globally by IEF1 state), the Z180 remains in HALT mode. However, $\overline{NMI}$ interrupt will initiate the normal $\overline{NMI}$ interrupt response sequence independent of the state of IEF_1.

HALT timing is shown in Fig 18.

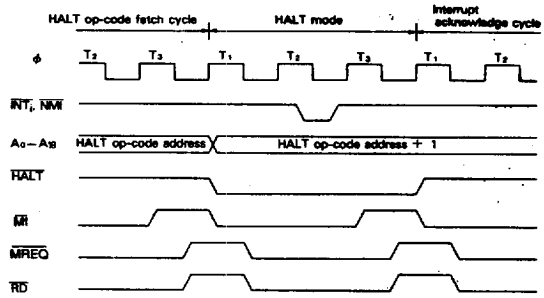


Figure 18. HALT Timing

SLEEP mode. SLEEP mode is entered by execution of the 2 byte SLP instruction. SLEEP mode has the following characteristics.

(1) The internal CPU clock stops, reducing power consumption.

(2) The internal crystal oscillator does not stop.

(3) Internal and external interrupt inputs can be received.

(4) DRAM refresh cycles stop.

(5) I/O operations using on-chip peripherals continue.

(6) The internal DMAC stop.

(7) $\overline{BUSREQ}$ can be received and acknowledged.

(8) Address outputs go HIGH and all other control signal output become inactive HIGH.

(9) Data Bus, 3-state.

SLEEP mode is exited in one of two ways as shown below.

RESET Exit from SLEEP mode. If the $\overline{RESET}$ input is held LOW for at least 6 clock cycles, it will exit SLEEP mode and begin the normal RESET sequence with execution starting at address (logical and physical) 00000H.

Interrupt Exit from SLEEP mode. The SLEEP mode is exited by detection of an external (NMI, INT_0-INT_2) or internal (ASCI, CSI/O, PRT) interrupt.

In case of $\overline{NMI}$, SLEEP Mode is exited and the CPU begins the normal $\overline{NMI}$ interrupt response sequence.

In the case of all other interrupts, the interrupt response depends on the state of the global interrupt enable flag (IEF_1) and the individual interrupt source enable bit.

If the individual interrupt condition is disabled by the corresponding enable bit, occurrence of that interrupt is ignored and the CPU remains in the SLEEP state.

Assuming the individual interrupt condition is enabled, the response to that interrupt depends on the global interrupt enable flag (IEF_1). If interrupts are globally enabled (IEF_1=1) and an individually enabled interrupt occurs, SLEEP mode is exited and the appropriate normal interrupt response sequence is executed.

If interrupts are globally disabled (IEF_1=0) and an individually enabled interrupt occurs, SLEEP mode is exited and instruction execution begins with the instruction following the SLP instruction. Note that this provides a technique for synchronization with high speed external events without incurring the latency imposed by an interrupt response sequence.

Figure 19 shows SLEEP timing.

IOSTOP mode. IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP mode. SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode, noting that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

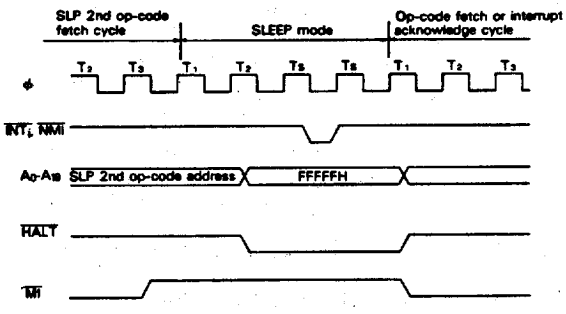


Figure 19. SLEEP Timing

Trap and Interrupts

The Z180 CPU has twelve interrupt sources, 4 external and 8 internal, with fixed priority. (Reference Figure 20).

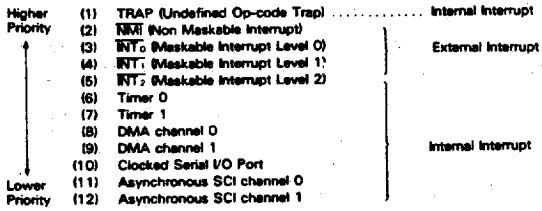


Figure 20. Interrupt Sources

TRAP Interrupt. The Z180 generates a non-maskaable TRAP interrupt when an undefined op-code fetch occurs. This feature can be used to increase software reliability, implement an "extended" instruction set, or both. TRAP may occur during op-code fetch cycles and also if an undefined op-code is fetched during the interrupt acknowledge cycle for INT_0 when Mode 0 is used.

When a TRAP interrupt occurs the Z180 operates as follows.

(1) The TRAP bit in the Interrupt TRAP/Control (ITC) register is set to 1.

(2) The current PC (Program Counter) value, reflecting location of the undefined op-code, is saved on the stack.

(3) The Z180 vectors to logical address 0. Note that if logical address 0000H is mapped to physical address 00000H, the vector is the same as for RESET. In this case, testing the TRAP bit in ITC will reveal whether the restart at physical address 00000H was caused by RESET or TRAP.

External Interrupts. The Z180 has four external hardware interrupt inputs.

(1) $\overline{NMI}$ - Non-maskable Interrupt
(2) $\overline{INT_0}$ - Maskable Interrupt Level 0
(3) $\overline{INT_1}$ - Maskable Interrupt Level 1
(4) $\overline{INT_2}$ - Maskable Interrupt Level 2

$\overline{NMI}$, $\overline{INT_1}$ and $\overline{INT_2}$ have fixed interrupt response modes. $\overline{INT_0}$ has 3 different software programmable interrupt response modes - Mode 0, Mode 1 and Mode 2.

$\overline{NMI}$ - Non-Maskable Interrupt. The $\overline{NMI}$ interrupt input is edge sensitive and cannot be masked by software. When $\overline{NMI}$ is detected, the Z180 operates as follows.

(1) DMAC operation is suspended by the clearing of the DME (DMA Main Enable) bit in DCNTL.

(2) The PC is pushed onto the stack.

(3) The contents of IEF_1 are copied to IEF_2. This saves the interrupt reception state that existed prior to $\overline{NMI}$.

(4) IEF_1 is cleared to 0. This disables all external and internal maskable interrupts (i.e. all interrupts except $\overline{NMI}$ and TRAP).

(5) Execution commences at logical address 0066H.

The last instruction of an $\overline{NMI}$ service routine should be RETN (Return from Non-maskable Interrupt). This restores the stacked PC, allowing the interrupted program to continue.

$\overline{INT_0}$ - Maskable Interrupt Level 0
The next highest priority external interrupt after $\overline{NMI}$ is $\overline{INT_0}$. $\overline{INT_0}$ is sampled at the falling edge of the clock state prior to T_3 or T1 in the last machine cycle. If $\overline{INT_0}$ is asserted LOW at the falling edge of the clock state prior to T_3 or T_1 in the last machine cycle, $\overline{INT_0}$ is accepted. The interrupt is masked if either the IEF1 flag or the ITE0 (Interrupt Enable 0) bit in ITC are reset to 0.

The $\overline{INT_0}$ interrupt is unique in that 3 programmable interrupt response modes are available - Mode 0, Mode 1 and Mode 2. The specific mode is selected with the IM 0, IM 1 and IM 2 (Set Interrupt Mode) instructions. During RESET, the Z180 is initialized to use Mode 0 for INT0. The 3 interrupt response modes for INT_0 are:

(1) Mode 0 - Instruction fetch from data bus.

(2) Mode 1 - Restart at logical address 0038H.

(3) Mode 2 - Low byte vector table address fetch from data bus.

$\overline{INT_0}$ Mode 0
During the interrupt acknowledge cycle, an instruction is fetched from the data bus (D0-D7) at the rising edge of T3. Often, this instruction is one of the eight single byte RST (RESTART) instructions which stack the PC and restart execution at a fixed logical address. However, multibyte instructions can be processed if the interrupt acknowledging device can provide a multibyte response. Unlike all other interrupts, the PC is not automatically stacked.

Note that TRAP interrupt will occur if an invalid instruction is fetched during Mode 0 interrupt acknowledge.

$\overline{INT_0}$ Mode 1
When $\overline{INT_0}$ is received, the PC is stacked and instruction execution restarts at logical address 0038H. Both IEF1 and IEF2 flags are reset to 0, disabling all maskable interrupts. The interrupt service routine should normally terminate with the EI (Enable Interrupts) instruction followed by the RETI (Return from Interrupt) instruction, to reenable the interrupts.

$\overline{INT_0}$ Mode 2
This method determines the restart address by reading the contents of a table residing in memory. The vector table consists of up to 128 two-byte restart addresses stored in low byte, high byte order.

The vector table address is located on 256 byte boundaries in the 64K byte logical address space programmed in the 8-bit Interrupt Vector Register (I).

During the $\overline{INT_0}$ Mode 2 acknowledge cycle, the low-order 8 bits of the vector is fetched from the data bus at the rising edge of T3 and the CPU acquires the 16-bit vector.

Next, the PC is stacked. Finally, the 16-bit restart address is fetched from the vector table and execution begins at that address.

Note that external vector acquisition is indicated by both $\overline{M1}$ and $\overline{IORQ}$ LOW. Two wait states (Tw) are automatically inserted for external vector fetch cycles.

$\overline{INT_1}$, $\overline{INT_2}$
The operation of external interrupts $\overline{INT_1}$ and $\overline{INT_2}$ is a vector mode similar to $\overline{INT_0}$ Mode 2. The difference is that $\overline{INT_1}$ and $\overline{INT_2}$ generate the low-order byte of vector table address using the IL (Interrupt Vector Low) register rather than fetching it from the data bus. This is also the interrupt response sequence used for all internal interrupts (except TRAP).

Internal Interrupts. Internal interrupts (except TRAP) ise the same vectored response mode as INT1 and INT2. Internal interrupts are globally masked by IEF1 = 0. Individual internal interrupts are enabled/disabled by programming each individual I/O (PRT, DMAC, CSI/O, ASCI) control register. The lower vector of INT_1, INT_2 and internal interrupt are summarized in Table 2.

Interrupt Source	Priority	IL			Fixed Code				
		b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
$\overline{INT_1}$	Highest	•	•	•	0	0	0	0	0
$\overline{INT_2}$		•	•	•	0	0	0	1	0
PRT channel 0		•	•	•	0	0	1	0	0
PRT channel 1		•	•	•	0	0	1	1	0
DMA channel 0		•	•	•	0	1	0	0	0
DMA channel 1		•	•	•	0	1	0	1	0
CSI/O		•	•	•	0	1	1	0	0
ASCI channel 0		•	•	•	0	1	1	1	0
ASCI channel 1	Lowest	•	•	•	1	0	0	0	0

* Programmable

Table 2. Vector Table

RETI Instruction Sequence:
When the EDH/4DH sequence is fetched by the Z180, it is recognized as the RETI instruction sequence. The Z180 will then refetch the RETI instruction with 4 T-states in the EDH cycle to allow the Z80 peripherals time to decode that cycle (See Figure 21). This allows the internal interrupt structure of the peripheral to properly decode the instruction and behave accordingly.

The M1E bit of the Operation Mode Control Register (OMCR) should be set to 0 so that $\overline{M1}$ signal is active only during the refetch of the RETI instruction sequence. This is the desired operation when Z80 peripherals are connected to the Z180.

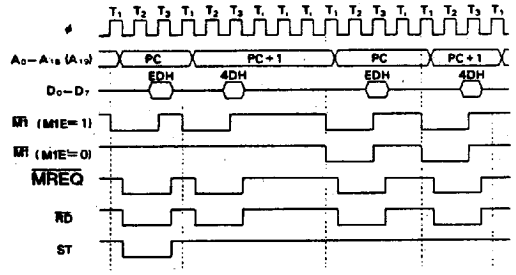


Figure 21. RETI Instruction Sequence

The RETI instruction takes 22 T-states and 10 machine cycles.

Interrupt Control Registers and Flags. The Z180 has three registers and two flags which are associated with interrupt processing.

Function	Name	Access Method
(1) Interrupt Vector High	I	LD A,I and LD I, A instructions
(2) Interrupt Vector Low	IL	I/O instruction (addr=33H)
(3) Interrupt/Trap Control	ITC	I/O instruction (addr=34H)
(4) Interrupt Enable Flag 1,2	IEF_1,IEF_2	EI and DI

Interrupt Enable/Disable Operation
Two flags, IEF_1 and IEF_2, are used to signal the Z180 CPU interrupt status. IEF_1 controls the overall enabling and disabling of all internal and external maskable interrupts (i.e. all interrupts except NMI and TRAP).

If $IEF_1 = 0$, all maskable interrupts are disabled. IEF_1 can be reset to 0 by the DI (Disable Interrupts) instruction and set to 1 by the EI (Enable Interrupts) instruction.

The purpose of IEF_2 is to correctly manage the occurrence of $\overline{NMI}$. During $\overline{NMI}$, the prior interrupt reception state is saved and all maskable interrupts are automatically disabled (IEF_1 copied to IEF_2 and then IEF_1 cleared to 0). At the end of the $\overline{NMI}$ interrupt service routine, execution of the RETN (Return from Non-maskable Interrupt) will automatically restore the interrupt receiving state (by copying IEF2 to IEF1) prior to the occurrence of $\overline{NMI}$.

IEF_2 state can be reflected in the P/V bit of the CPU Status Register by executing LD A, I or LD A, R instructions.

CPU Operation	IEF_1	IEF_2	REMARKS
RESET	0	0	Inhibits the interrupt except $\overline{NMI}$ and TRAP
$\overline{NMI}$	0	IEF_1	Copies the contents of IEF_1 to IEF_2.
RETN	IEF_2	not affected	Returns from the $\overline{NMI}$ service routine
Interrupt except $\overline{NMI}$ and TRAP	0	0	Inhibits the interrupt except $\overline{NMI}$ and TRAP
RETI	not affected	not affected	
TRAP	not affected	not affected	
EI	1	1	
DI	0	0	
LD A, I	not affected	not affected	Transfers the contents of IEF_2 to P/V flag
LD A, R	not affected	not affected	Transfers the contents of IEF_2 to P/V flag

Table 3. State of IEF_1 and IEF_2

Internal I/O Registers

The Z180 internal I/O Registers occupy 64 I/O addresses (including reserved addresses). These registers access the internal I/O modules (ASCI, CSI/O, PRT) and control functions (DMAC, DRAM refresh, interrupts, wait state generator, MMU and I/O relocation).

To avoid address conflicts with external I/O, the Z180 internal I/O addresses can be relocated on 64 byte boundaries within the bottom 256 bytes of the 64K byte I/O address space.

ADDITIONAL FEATURES ON Z8S180™

STANDBY Mode

The Z8S180 MPU has been designed to be fully static. A very low power programmable standby mode has been added. To enter STANDBY mode:

1. Set the standby enable bit (D6 of the CPU Control Register, I/O Address = 1FH)

2. Execute the SLP instruction

When the part is in STANDBY mode, it behaves similar to the SYSTEM STOP mode which currently exists on the Z180 MPU, except the STANDBY mode stops the external oscillator, internal clocks and reduce power consumption to less than 10 μA.

Since the external oscillator has been stopped, a restart of the oscillator requires a period of time for stabilization. A 20-bit counter has been added in the Z8S180 to allow for oscillator stabilization. When the part receives an external IRQ or BUSREQ during STANDBY mode, the oscillator is restarted and the timer counts down 2^{19} counts before acknowledgement is sent to the interrupt source.

The following is a description of how the part exits STANDBY for different interrupts and modes of operation.

STANDBY Mode Exit With RESET

The /RESET input is to be asserted for a duration long enough for the crystal oscillator to stabilize (10 ms MAX) to exit from the STANDBY mode. When /RESET is de-asserted, it goes through the normal reset timing to start instruction execution at address (logical and physical) 0000H.

The clocking is resumed within the Z8S180 and at the system clock output after /RESET is asserted, when the crystal oscillator is restarted but not yet stabilized.

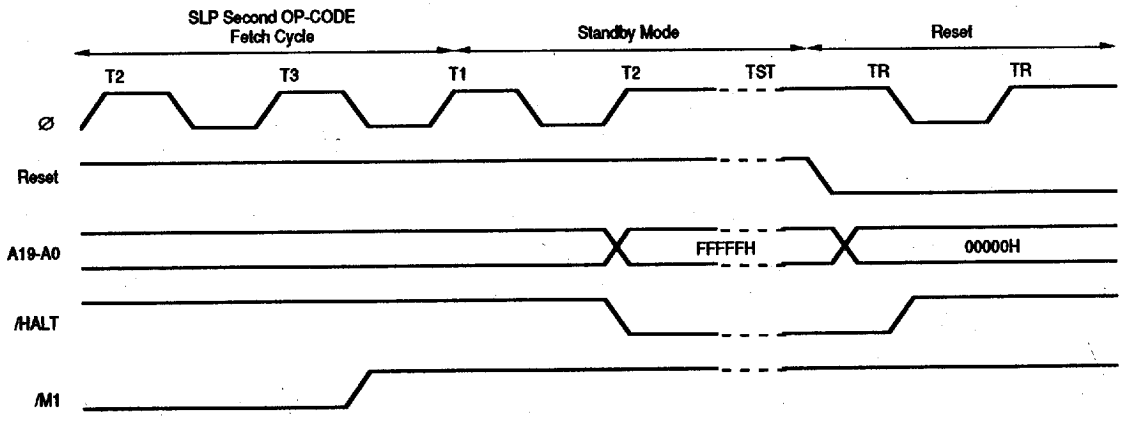


Figure A. Z8S180 Standby Mode Timing With Reset Exit

STANDBY Mode Exit With BUS REQUEST

Optionally, if the BREXT bit (D5 of CPU Control Register) is set to 1, the Z8S180 exits STANDBY mode when the /BUSREQ input is asserted. The crystal oscillator is then restarted. An internal counter automatically provides time for the oscillator to stabilize, before the internal clocking and the system clock output of the Z8S180 are resumed.

The Z8S180 relinquishes the system bus after the clocking is resumed by:

- Tri-Stating the address outputs A19 through A0
- Tri-Stating the bus Control outputs /MREQ, /IORQ, /RD and /WR
- Asserting /BUSACK

The Z8S180 will regain the system bus when /BUSREQ is deactivated. The address outputs and the bus control outputs will then be driven High. The STANDBY mode is then resumed.

If the BREXT bit of the CPU Control Register (CCR) is cleared, asserting the /BUSREQ would not cause the Z8S180 to exit STANDBY mode.

If STANDBY mode is exited, due to a reset or an external interrupt, the Z8S180 will keep relinquished from the system bus as long as the /BUSREQ is active.

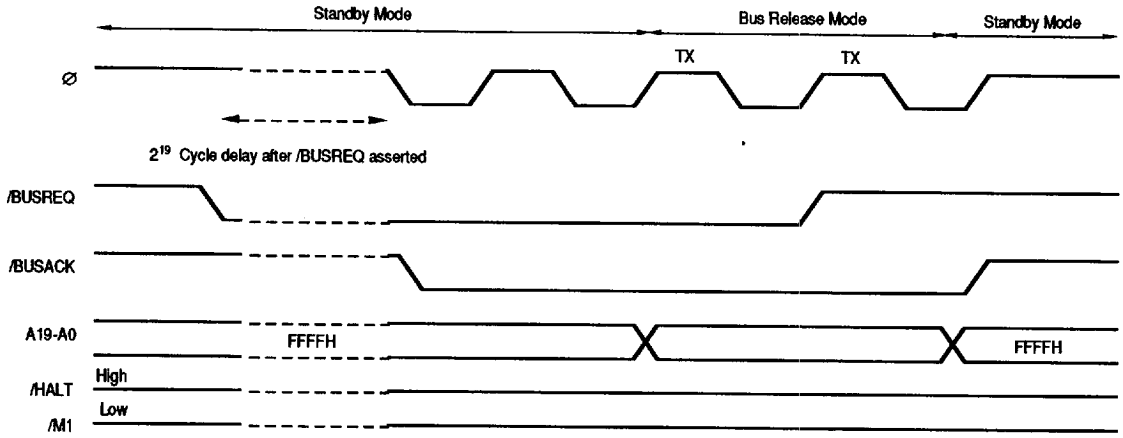


Figure B. Z8S180 Standby Mode Exit With Bus Request

STANDBY Mode Exit With EXTERNAL INTERRUPTS

STANDBY mode can be exited by asserting input /NMI. The STANDBY mode may also exit by asserting /INT0, /INT1 or /INT2, depending on the conditions specified in the following paragraphs. If exit conditions are met, the internal counter provides time for the crystal oscillator to stabilize, before the internal clocking and the system clock output within the Z8S180 are resumed.

a. Exit with Non-Maskable Interrupts

If /NMI is asserted, the CPU begins a normal NMI interrupt acknowledge sequence after clocking resumes.

b. Exit with External Maskable Interrupts

If an external maskable interrupt input is asserted, the CPU responds according to the status of the Global Interrupt Enable Flag IEF1 (determined by the ITE1 bit) and the settings of the corresponding interrupt enable bit in the Interrupt/Trap Control Register (ITC: I/O Address = 34H):

1. If an interrupt source is disabled in the ITC, asserting the corresponding interrupt input would not cause the Z8S180 to exit STANDBY mode. This is true regardless of the state of the Global Interrupt Enable Flag IEF1.

2. If the Global Interrupt Flag IEF1 is set to 1, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input causes the Z8S180 to exit STANDBY mode.

   The CPU will perform an interrupt acknowledge sequence appropriate to the input being asserted when clocking is resumed if:

   - the interrupt input follows the normal interrupt daisy-chain protocol
   - the interrupt source is active until the acknowledge cycle is completed

3. If the Global Interrupt Flag IEF1 is disabled, i.e., reset to 0, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input still causes the Z8S180 to exit STANDBY mode.

   The CPU proceeds to fetch and execute instructions that follows the SLP instruction when clocking is resumed.

If the external maskable interrupt input is not active until clocking resumes, the Z8S180 will not exit STANDBY mode.

If the Non-Maskable Interrupt (/NMI) is not active until clocking resumes, the Z8S180 still exits the STANDBY mode even if the interrupt sources go away before the timer times out. It is because /NMI is edge-triggered. The condition is latched internally once /NMI is asserted Low.

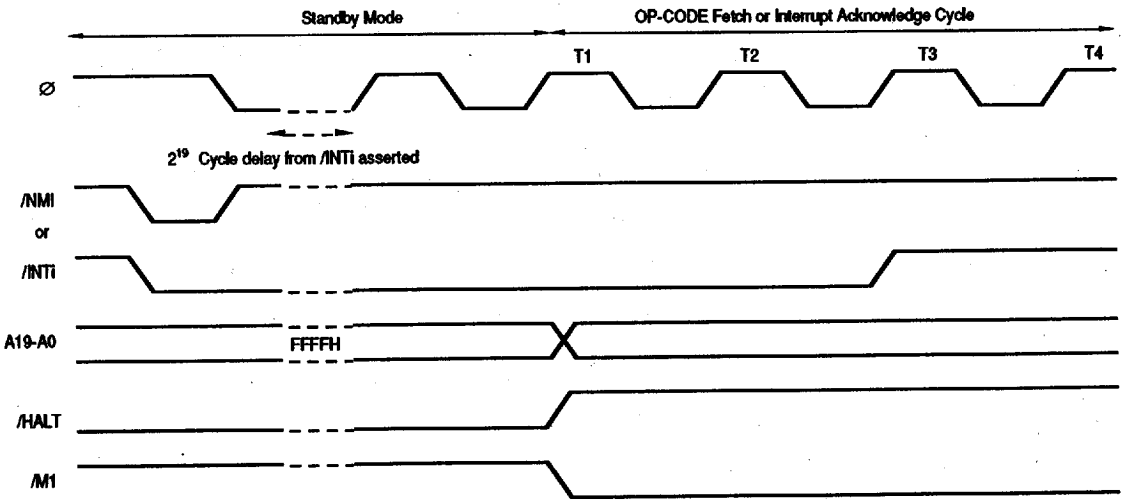


Figure C. Z8S180 Standby Mode Exit With External Interrupts

CPU Control Register

The Z8S180 has an additional register that allows the programmer to select options. This directly affects the CPU performance as well as controlling the STANDBY operating mode of the chip. The CPU CONTROL REGISTER (CCR) allows the programmer to change the divide-by-two internal clocks to divide-by-one. In addition, applications where EMI noise is a problem, the Z8S180 can reduce the output drivers on selected groups of pins to 20% of normal pad driver capability which reduces the EMI noise generated by the part to minimal.

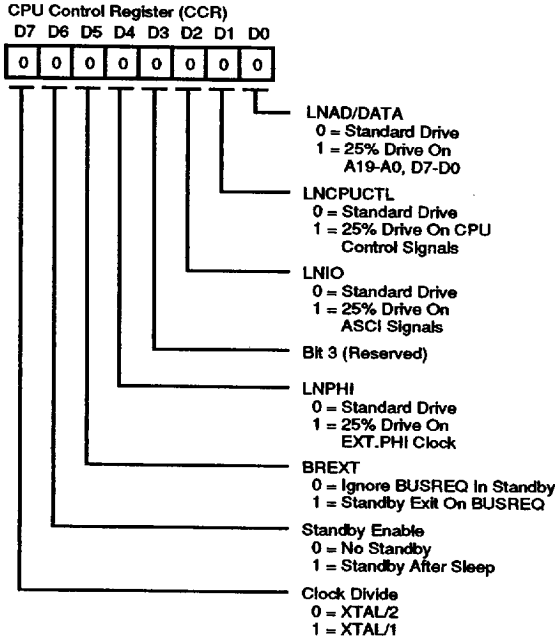


Figure D. Z8S180 Only CPU Control Register (CCR) Address $1F (Reset Values Shown)

Bit 7. *Clock Divide Select.* Bit 7 of the CCR allows the programmer to set the internal clock to divide the external clock by 2 if the bit is 0, and divide by 1 if the bit is 1.

Upon reset this bit is set to 0 and the part is in divide-by-2 mode. Since the on-board oscillator is not guaranteed to operate above 20 MHz, an external source must be used to achieve the maximum 20 MHz operation of the part, i.e., an external clock at 40 MHz with 50% duty cycle.

If the external oscillator is used in divide-by-1 mode, the duty cycle of the external oscillator should be as close to 50% as possible. A maximum 60%/40% or 40%/60% duty cycle is permissible at 10 MHz.

Bit 6. *STANDBY Enable.* This bit is used for enabling/disabling the STANDBY mode. Setting this bit to 1 enables the STANDBY mode. The Z8S180 will enter STANDBY after fetching the second opcode of a SLP instruction if the IOSTOP bit is set.

Bit 5. *BREXT.* This bit controls the ability of the Z8S180 to honor a bus request during STANDBY mode. If this bit is set to 1 and the part is in STANDBY mode, a BUSREQ is honored after the clock stabilization timer is timed out.

Bit 4. *LNPHI.* This bit controls the drive capability on the PHI Clock output. If this bit is set to 1, the PHI Clock output is reduced to 25% of its drive capability.

Bit 3. *Reserved.*

CPU Control Register (Continued)

Bit 2. *LNIO.* This bit controls the drive capability of the external I/O pins of the Z8S180. When this bit is set to 1, the output driving capability of the following pins is reduced to 25% of the original drive capability:

- CKS
- RXS/CTS1
- TXS
- CKA1/TEND0
- TXA1
- CKA0/DREQ0
- TXA0

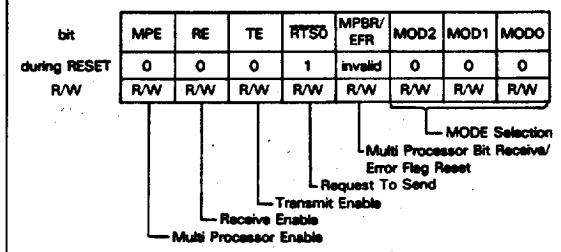
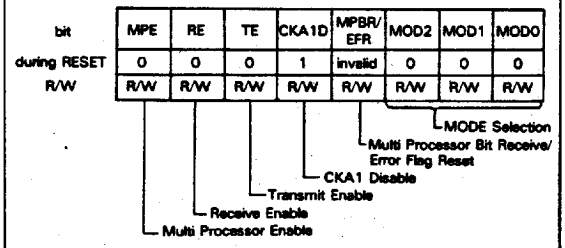
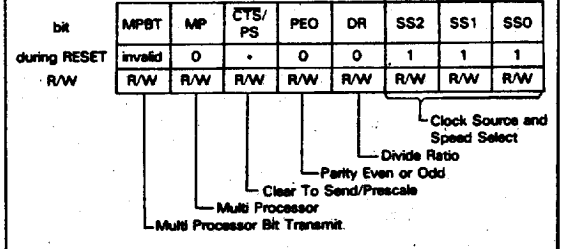
Bit 1. *LNCPUCTL.* This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output driving capability of the following pins is reduced to 25% of the original drive capability:

- /BUSACK
- /RD
- /WR
- /M1
- E
- /MREQ
- /IORQ
- /RFSH
- /HALT
- /TEND1

Bit 0. *LNAD/DATA.* This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output driving capability of the Address and Data bus output is reduced to 25% of its original drive capability.

Internal I/O Registers

By programming IOA7 and IOA6 in the I/O control register, internal I/O register addresses are relocatable within ranges from 0000H to 00FFH in the I/O address space.

REGISTER	MNEMONICS	ADDRESS	REMARKS
ASCI Control Register A Channel 0	CNTLA0	0 0	
ASCI Control Register A Channel 1	CNTLA1	0 1	
ASCI Control Register B Channel 0	CNTLB0	0 2	

MOD2, 1, 0

0 0 0	Start + 7 bit Data + 1 Stop
0 0 1	Start + 7 bit Data + 2 Stop
0 1 0	Start + 7 bit Data + Parity + 1 Stop
0 1 1	Start + 7 bit Data + Parity + 2 Stop
1 0 0	Start + 8 bit Data + 1 Stop
1 0 1	Start + 8 bit Data + 2 Stop
1 1 0	Start + 8 bit Data + Parity + 1 Stop
1 1 1	Start + 8 bit Data + Parity + 2 Stop

• $\overline{CTS}$: Depending on the condition of $\overline{CTS}$ Pin.
PS : Cleared to 0.

(to be continued)

REGISTER	MNEMONICS	ADDRESS	REMARKS

ASCI Control Register B Channel 1 : CNTLB1 — 0 3

bit	MPBT	MP	$\overline{CTS}$/PS	PEO	DR	SS2	SS1	SS0
during RESET	invalid	0	0	0	0	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- SS2, SS1, SS0: Clock Source and Speed Select
- DR: Divide Ratio
- PEO: Parity Even or Odd
- $\overline{CTS}$/PS: Clear To Send/Prescale
- MP: Multi Processor
- MPBT: Multi Processor Bit Transmit

General divide ratio	PS=0 (divide ratio=10)		PS=1 (divide ratio=30)	
SS2,1,0	DR=0 (×16)	DR=1 (×64)	DR=0 (×16)	DR=1 (×64)
000	$\phi \div$ 160	$\phi \div$ 640	$\phi \div$ 480	$\phi \div$ 1920
001	$\div$ 320	$\div$ 1280	$\div$ 960	$\div$ 3840
010	$\div$ 640	$\div$ 2560	$\div$ 1920	$\div$ 7680
011	$\div$ 1280	$\div$ 5120	$\div$ 3840	$\div$ 15360
100	$\div$ 2560	$\div$ 10240	$\div$ 7680	$\div$ 30720
101	$\div$ 5120	$\div$ 20480	$\div$ 15360	$\div$ 61440
110	$\div$ 10240	$\div$ 40960	$\div$ 30720	$\div$ 122880
111	External clock (frequency < $\phi \div 40$)			

ASCI Status Register Channel 0 : STAT0 — 0 4

bit	RDRF	OVRN	PE	FE	RIE	$\overline{DCD0}$	TDRE	TIE
during RESET	0	0	0	0	0	*	**	0
R/W	R	R	R	R	R/W	R	R	R/W

- TIE: Transmit Interrupt Enable
- TDRE: Transmit Data Register Empty
- $\overline{DCD0}$: Data Carrier Detect
- RIE: Receive Interrupt Enable
- FE: Framing Error
- PE: Parity Error
- OVRN: Over Run Error
- RDRF: Receive Data Register Full

** $\overline{CTS_0}$ Pin: L → TDRE: 1; H → TDRE: 0

* $\overline{DCD_0}$: Depending on the condition of $\overline{DCD_0}$ Pin.

ASCI Status Register Channel 1 : STAT1 — 0 5

bit	RDRF	OVRN	PE	FE	RIE	CTS1E	TDRE	TIE
during RESET	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R/W	R/W	R	R/W

- TIE: Transmit Interrupt Enable
- TDRE: Transmit Data Register Empty
- CTS1E: $\overline{CTS1}$ Enable
- RIE: Receive Interrupt Enable
- FE: Framing Error
- PE: Parity Error
- OVRN: Over Run Error
- RDRF: Receive Data Register Full

(to be continued)

REGISTER	MNEMONICS	ADDRESS	REMARKS
ASCI Transmit Data Register Channel 0	: TDR0	0 6	
ASCI Transmit Data Register Channel 1	: TDR1	0 7	
ASCI Receive Data Register Channel 0	: TSR0	0 8	
ASCI Receive Data Register Channel 1	: TSR1	0 9	
CSI/O Control Register	: CNTR	0 A	
CSI/O Transmit/Receive Data Register	: TRDR	0 B	
Timer Data Register Channel 0L	: TMDR0L	0 C	
Timer Data Register Channel 0H	: TMDR0H	0 D	
Timer Reload Register Channel 0L	: RLDR0L	0 E	
Timer Reload Register Channel 0H	: RLDR0H	0 F	
Timer Control Register	: TCR	1 0	

bit

	EF	EIE	RE	TE	–	SS2	SS1	SS0
during RESET	0	0	0	0	1	1	1	1
R/W	R	R/W	R/W	R/W		R/W	R/W	R/W

- SS2, SS1, SS0: Speed Select
- TE: Transmit Enable
- RE: Receive Enable
- EIE: End Interrupt Enable
- EF: End Flag

SS2,1,0	Baud Rate	SS2,1,0	Baud Rate
000	φ÷ 20	100	φ÷ 320
001	÷ 40	101	÷ 640
010	÷ 80	110	÷1280
011	÷160	111	External (frequency < ÷ 20)

bit

	TIF1	TIF0	TIE1	TIE0	TOC1	TOC0	TDE1	TDE0
during RESET	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

- TDE1, TDE0: Timer Down Count Enable 1,0
- TOC1, TOC0: Timer Output Control 1,0
- TIE1, TIE0: Timer Interrupt Enable 1,0
- TIF1, TIF0: Timer Interrupt Flag 1,0

TOC1,0	Ath/TOUT
00	Inhibited
01	Toggle
10	0
11	1

(to be continued)

REGISTER	MNEMONICS	ADDRESS	REMARKS
Timer Data Register Channel 1L	: TMDR1L	1 4	
Timer Data Register Channel 1H	: TMDR1H	1 5	
Timer Relosd Register Channel 1L	: RLDR1L	1 6	
Timer Reload Register Channel 1H	: RLDR1H	1 7	
Free Running Counter	: FRC	1 8	read only
DMA Source Address Register Channel 0L	: SAR0L	2 0	
DMA Source Address Register Channel 0H	: SAR0H	2 1	
DMA Source Address Register Channel 0B	: SAR0B	2 2	Bits 0-2 (3) are used for SAR0B. A_{19}*, A_{18}, A_{17}, A_{16} | DMA Transfer Request X X 0 0 | $\overline{DREQ_0}$ (external) X X 0 1 | RDR0 (ASCI0) X X 1 0 | RDR1 (ASCI1) X X 1 1 | Not Used
DMA Destination Address Register Channel 0L	: DAR0L	2 3	
DMA Destination Address Register Channel 0H	: DAR0H	2 4	
DMA Destination Address Register Channel 0B	: DAR0B	2 5	Bits 0-2 (3) are used for DAR0B. A_{19}*, A_{18}, A_{17}, A_{16} | DMA Transfer Request X X 0 0 | $\overline{DREQ_0}$ (external) X X 0 1 | TDR0 (ASCI0) X X 1 0 | TDR1 (ASCI1) X X 1 1 | Not Used
DMA Byte Count Register Channel 0L	: BCR0L	2 6	
DMA Byte Count Register Channel 0H	: BCR0H	2 7	
DMA Memory Address Register Channel 1L	: MAR1L	2 8	
DMA Memory Address Register Channel 1H	: MAR1H	2 9	
DMA Memory Address Register Channel 1B	: MAR1B	2 A	Bits 0-2 (3) are used for MAR1B.
DMA I/O Address Register Channel 1L	: IAR1L	2 B	
DMA I/O Address Register Channel 1H	: IAR1H	2 C	

(to be continued)

* In the R1 and Z Mask, these DMAC registers are expanded from 4 bits to 3 bits in the package version of CP-68 and FP-80.

REGISTER	MNEMONICS	ADDRESS	REMARKS
DMA Byte Count Register Channel 1L	: BCR1L	2 E	
DMA Byte Count Register Channel 1H	: BCR1H	2 F	
DMA Status Register	: DSTAT	3 0	
DMA Mode Register	: DMODE	3 1	

bit	DE1	DE0	DWE1	DWE0	DIE1	DIE0	–	DME
during RESET	0	0	1	1	0	0	1	0
R/W	R/W	R/W	W	W	R/W	R/W		R

DMA Master Enable
DMA Interrupt Enable 1,0
DMA Enable Bit Write Enable 1,0
DMA Enable ch 1,0

bit	–	–	DM1	DM0	SM1	SM0	MMOD	–
during RESET	1	1	0	0	0	0	0	1
R/W			R/W	R/W	R/W	R/W	R/W	

Memory MODE Select
Ch 0 Source Mode 1,0
Ch 0 Destination Mode 1, 0

DM1, 0	Destination	Address
0 0	M	DAR0+1
0 1	M	DAR0−1
1 0	M	DAR0 fixed
1 1	I/O	DAR0 fixed

SM1, 0	Source	Address
0 0	M	SAR0+1
0 1	M	SAR0−1
1 0	M	SAR0 fixed
1 1	I/O	SAR0 fixed

MMOD	Mode
0	Cycle Steal Mode
1	Burst Mode

(to be continued)

REGISTER	MNEMONICS	ADDRESS	REMARKS
DMA/WAIT Control Register	: DCNTL	3 2	

bit	MWI1	MWI0	IWI1	IWI0	DMS1	DMS0	DIM1	DIM0
during RESET	1	1	1	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

DMA Ch 1 I/O Memory Mode Select

$\overline{DREQi}$ Select, i = 1,0

I/O Wait Insertion

Memory Wait Insertion

MWI1,0	The number of wait states
0 0	0
0 1	1
1 0	2
1 1	3

IWI1,0	The number of wait states
0 0	0
0 1	2
1 0	3
1 1	4

DMSi	Sense
1	Edge sense
0	Level sense

DIM1,0	Transfer Mode	Address Increment/Decrement	
0 0	M→I/O	MAR1 + 1	IAR1 fixed
0 1	M→I/O	MAR1 − 1	IAR1 fixed
1 0	I/O→M	IAR1 fixed	MAR1 + 1
1 1	I/O→M	IAR1 fixed	MAR1 − 1

Interrupt Vector Low Register	: IL	3 3

bit	IL7	IL6	IL5	–	–	–	–	–
during RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W					

Interrupt Vector Low

INT/TRAP Control Register	: ITC	3 4

bit	TRAP	UFO	–	–	–	ITE2	ITE1	ITE0
during RESET	0	0	1	1	1	0	0	1
R/W	R/W	R				R/W	R/W	R/W

$\overline{INT}$ Enable 2,1,0

Undefined Fetch Object

TRAP

Refresh Control Register	: RCR	3 6

bit	REFE	REFW	–	–	–	–	CYC1	CYC0
during RESET	1	1	1	1	1	1	0	0
R/W	R/W	R/W					R/W	R/W

Cycle Select

Refresh Wait State

Refresh Enable

CYC1,0	Interval of Refresh Cycle
0 0	10 States
0 1	20
1 0	40
1 1	80

(to be continued)

REGISTER	MNEMONICS	ADDRESS	REMARKS
MMU Common Base Register	: CBR	3 8	
MMU Bank Base Register	: BBR	3 9	
MMU Common/Bank Area Register	: CBAR	3 A	
Operation Mode Control Register	: OMCR	3 E	
I/O Control Register	: ICR	3 F	

MMU Common Base Register

bit	CB7*	CB6	CB5	CB4	CB3	CB2	CB1	CB0
during RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MMU Bank Base Register

bit	BB7*	BB6	BB5	BB4	BB3	BB2	BB1	BB0
during RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MMU Common/Bank Area Register

bit	CA3	CA2	CA1	CA0	BA3	BA2	BA1	BA0
during RESET	1	1	1	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Operation Mode Control Register

bit	M1E	$\overline{M1TE}$	$\overline{IOC}$	–	–	–	–	–
during RESET	1	1	1	1	1	1	1	1
R/W	R/W	W	R/W					

I/O Control Register

bit	IOA7	IOA6	IOSTP	–	–	–	–	–
during RESET	0	0	0	1	1	1	1	1
R/W	R/W	R/W	R/W					

These MMU registers are expanded from 7 bits to 8 bits in the PLCC package

Memory Management Unit (MMU)

The Z180 has an on-chip MMU which performs the translation of the CPU 64K byte (16-bit addresses 0000H to FFFFH) logical memory address space into a 1024K byte (20-bit addresses 00000H to FFFFFH) physical memory address space. Address translation occurs internally in parallel with other CPU operation.

Logical Address Spaces. The 64K byte CPU logical address space is interpreted by the MMU as consisting of up to three separate logical address areas, Common Area 0, Bank Area, and Common Area 1.

As shown in Fig.22, a variety of logical memory configurations are possible. The boundaries between the Common and Bank Areas can be programmed with 4K byte resolution.

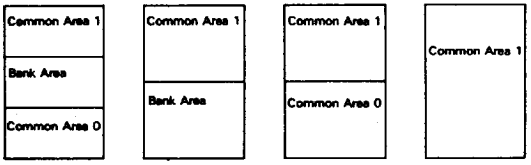


Figure 22. Logical Address Mapping Examples

Whether address translation takes place depends on the type of CPU cycle as follows.

(1) Memory Cycles
Address Translation occurs for all memory access cycles including instruction and operand fetches, memory data reads and writes, hardware interrupt vector fetch, and software interrupt restarts.

(2) I/O Cycles
The MMU is logically bypassed for I/O cycles. The 16-bit logical I/O address space corresponds directly with the 16-bit physical I/O address space. The four high-order bits (A16-A19) of the physical address are always 0 during I/O cycles.

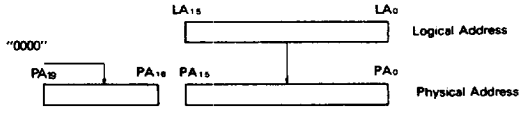


Figure 23. I/O Address Translation

(3) DMA Cycles
When the Z180 on-chip DMAC is using the external bus, the MMU is physically bypassed. The 20-bit source and destination registers in the DMAC are directly output on the physical address bus (A0-A19).

Physical address translation. Fig. 24 shows the way in which physical addresses are generated based on the contents of CBAR, CBR and BBR. MMU comparators classify an access by logical area as defined by CBAR. Depending on which of the three potential logical areas (Common Area 1, Bank Area, or Common Area 0) is being accessed, the appropriate 8-bit base address is added to the high-order 4 bits of the logical address, yielding a 20-bit physical address. CBR is associated with Common Area 1 accesses. Common Area 0, if defined, is always based at physical address 00000H.

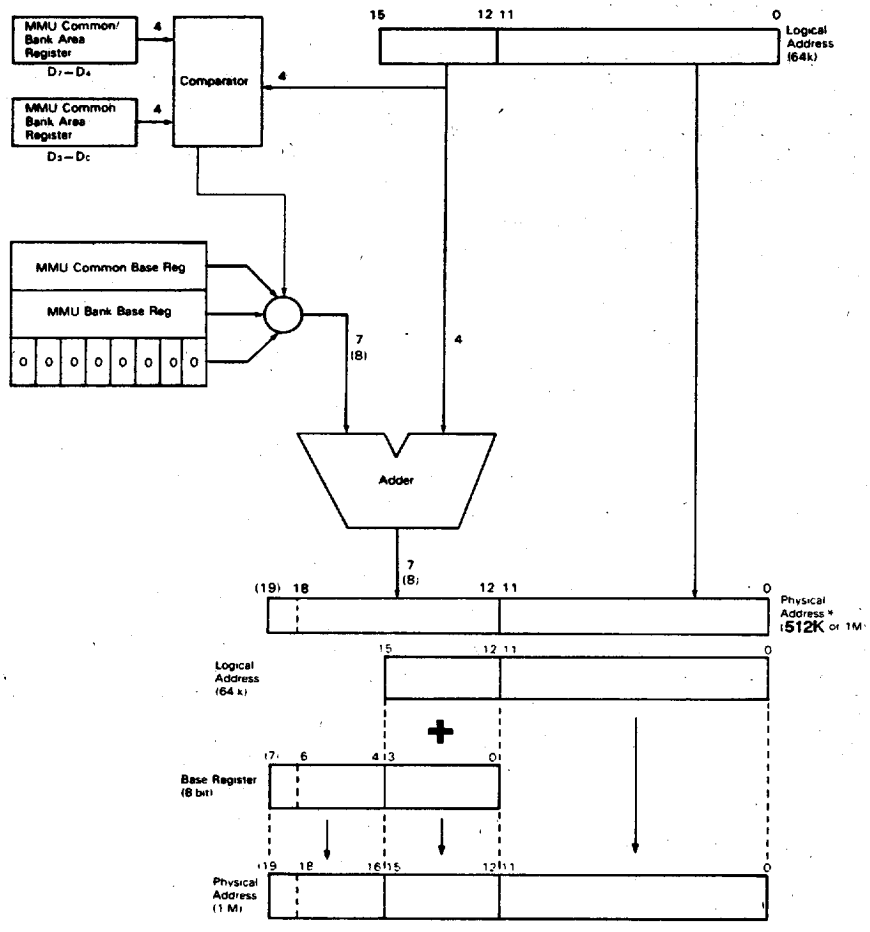


Figure 24. Physical Address Generation

(*Z80180 in DIP package is addressable to 512K. All other Z180 can address up to 1M.)

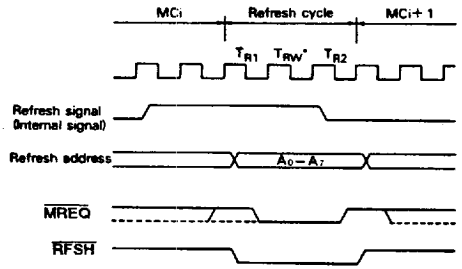
Dynamic RAM Refresh Control

The Z180 incorporates a dynamic RAM refresh control circuit including 8-bit refresh address generation and programmable refresh timing. This circuit generates asynchronous refresh cycles inserted at the programmable interval independent of CPU program execution. For systems which do not use dynamic RAM, the refresh function can be disabled.

When the internal refresh controller determines that a refresh cycle should occur, the current instruction is interrupted at the first breakpoint between machine cycles. The refresh cycle is inserted by placing the refresh address on A_0-A_7 and the $\overline{RFSH}$ output is driven LOW.

Refresh cycles may be programmed to be either 2 or 3 clock cycles in duration by programming the REFW (Refresh Wait) bit in the Refresh Control Register (RCR). Note that the external $\overline{WAIT}$ input and the internal wait state generator are not effective during refresh.

Fig. 25 shows the timing of a refresh cycle with a refresh wait (T_{RW}) cycle.



NOTE: * If three refresh cycles are specified, T_{RW} is inserted. Otherwise, T_{RW} is not inserted.
MC: Machine Cycle

Figure 25. Refresh Cycle Timing

DMA Controller (DMAC)

The Z180 contains a two-channel DMA (Direct Memory Access) controller which supports high speed data transfer. Both channels (channel 0 and channel 1) have the following capabilities.

Memory Address Space. Memory source and destination addresses can be directly specified anywhere within the 1024K byte physical address space using 20-bit source and destination memory addresses. In addition, memory transfers can arbitrarily cross 64K byte physical address boundaries without CPU intervention.

I/O Address Space. I/O source and destination addresses can be directly specified anywhere within the 64K byte I/O address space (16-bit source and destination I/O addresses).

Transfer Length. Up to 64K bytes are transferred based on a 16-bit byte count register.

$\overline{DREQ}$ Input. Level and edge sense DREQ input detection are selectable.

$\overline{TEND}$ Output. Used to indicate DMA completion to external devices.

Transfer Rate. Each byte transfer can occur every 6 clock cycles. Wait states can be inserted in DMA cycles for slow memory or I/O devices. At the system clock (ø) = 6 MHz, the DMA transfer rate is as high as 1.0 megabytes/second (no wait states).

There is an additional feature disc for DMA interrupt request by DMA END. Each channel has the following additional specific capabilities.

Channel 0
Memory ↔ memory, memory ↔ I/O, memory ↔ memory mapped I/O transfers.

-Memory address increment, decrement, no-change.
-Burst or cycle steal memory to/from memory transfers.
-DMA to/from both ASCI channels.
-Higher priority than DMAC channel 1.

Channel 1
Memory ↔ I/O transfer.
Memory address increment, decrement

DMAC Registers
Each channel of the DMAC (channel 0, 1) has three registers specifically associated with that channel.

Channel 0
SAR0 - Source Address Register
DAR0 - Destination Address Register
BCR0 - Byte Count Register

Channel 1
MAR1 - Memory Address Register
IAR1 - I/O Address Register
BCR1 - Byte Count Register

The two channels share the following three additional registers in common.

DSTAT - DMA Status Register
DMODE - DMA Mode Register
DCNTL - DMA Control Register

DMAC Block Diagram. Fig.26 shows the Z180 DMAC Block Diagram.

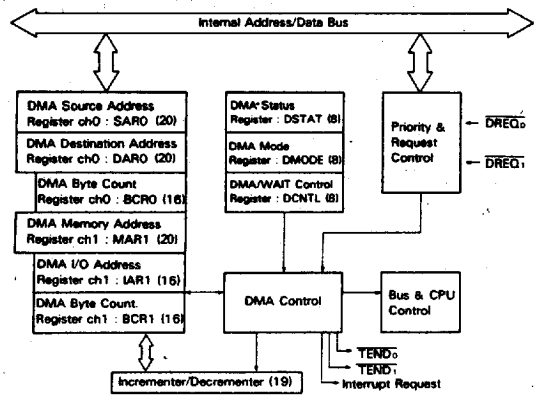


Figure 26. DMAC Block Diagram

Asynchronous Serial Communication Interface (ASCI)

The Z180 on-chip ASCI has two independent full-duplex channels. Based on full programmability of the following functions, the ASCI directly communicates with a wide variety of standard UARTs (Universal Asynchronous Receiver/Transmitter) including the Z8440 SIO, the Z8530 SCC and the Z85230 ESCC.

The key functions for ASCI are shown below. Each channel is independently programmable.

-Full-duplex communication.
-7- or 8-bit data length.
-Program controlled 9th data bit for multiprocessor communication.
-1 or 2 stop bits.
-Odd, even, no parity.
-Parity, overrun, framing error detection.
-Programmable baud rate generator, /16 and /64 modes.
-Speed to 38.4K bits per second (CPU fc = 6.144 MHz).
-Modem control signals - Channel 0 has $\overline{DCD0}$, $\overline{CTS0}$ and $\overline{RTS0}$ Channel 1 has $\overline{CTS1}$.
-Programmable interrupt condition enable and disable.
-Operation with on-chip DMAC.

ASCI Block Diagram. Fig. 27 shows the ASCI Block Diagram.

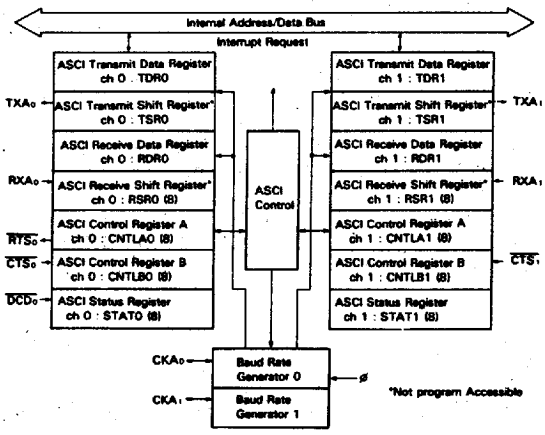


Figure 27. ASCI Block Diagram

Clocked Serial I/O Port (CSI/O)

The Z180 includes a simple, high speed clock, synchronous serial I/O port. The CSI/O includes transmit/receive (half-duplex), fixed 8-bit data, and internal or external data clock selection. High speed operation (baud rate 200K bits/second at fC = 4 MHz) is provided. The CSI/O is ideal for implementing a multiprocessor communication link between mulitple Z180s. These secondary devices may typically perform a portion of the system I/O processing, i.e. keyboard scan/decode, LDC interface, etc.

CSI/O Block Diagram. The CSI/O block diagram is shown in Fig. 28. The CSI/O consists of two registers - the Transmit/Receive Data Register (TRDR) and Control Register (CNTR).

CSI/O Transmit/Receive Data Register (TRDR: I/O Address = 0BH). TRDR is used for both CSI/O transmission and reception. Thus, the system design must insure that the constraints of half-duplex operation are met (Transmit and receive operation cannot occur simultaneously). For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, a CSI/O will not work. Also note that TRDR is not buffered. Therefore, attempting to perform a CSI/O transmit while the previous transmit data is still being shifted out causes the shift data to be immediately updated, thereby corrupting the transmit operation in progress. Similarly, reading TRDR while a transmit or receive is in progress should be avoided.

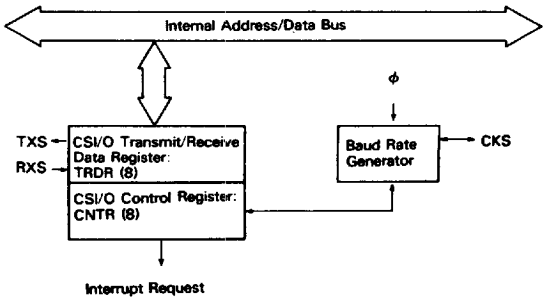


Figure 28. CSI/O Block Diagram

CSI/O Register Description

CSI/O Control/Status Register (CNTR: I/O Address = 0AH). CNTR is used to monitor CSI/O status, enable and disable the CSI/O, enable and disable interrupt generation, and select the data clock speed and source.

Programmable Reload Timer (PRT)

The Z180 contains a two channel 16-bit Programmable Reload Timer. Each PRT channel contains a 16-bit down counter and a 16-bit reload register. The down counter is directly read and written and a down counter overflow interrupt can be programmably enabled or disabled. Also, PRT channel 1 has a TOUT output pin (pin 31 - multiplexed with A18) which can be set HIGH, LOW, or toggled. Thus, PRT1 can perform programmable output waveform generation.

PRT block diagram. The PRT block diagram is shown in Fig. 29. The two channels have seperate timer data and reload registers and a common status/control register. The PRT input clock for both channels is equal to the system clock divided by 20.

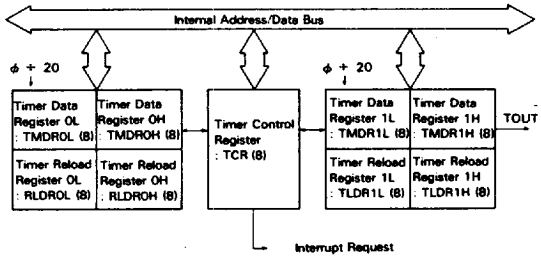


Figure 29. PRT Block Diagram

Secondary Bus Interface

E clock Output Timing. The Z180 also has a secondary bus interface that allows it to easily interface with other peripheral families.

These devices require connection with the Z180 synchronous E clock output. The speed (access time) required for the peripheral devices are determined by the Z180 clock rate. Table 19, and Figures 80-82 define E clock output timing.

On-Chip Clock Generator

The Z180 contains a crystal oscillator and system clock generator. A crystal can be directly connected or an external clock input can be provided. In either case, the system clock is equal to one-half the input clock. For example, a crystal or external clock input of 8 MHz corresponds with a system clock rate of 4 MHz.

The following table shows the AT cut crystal characteristics (Co, Rs) and the load capacitance (CL1, CL2) required for various frequencies of Z80180 operation.

Item \ Clock Frequency	4MHz	4MHz < f ≤ 12MHz	12MHz < f ≤ 18MHz
Co	< 7 pF	< 7 pF	< 7 pF
Rs	< 60Ω	< 80Ω	< 60Ω
CL_1, CL_2	10 to 22 pF ± 10%	10 to 22 pF ± 10%	10 to 22 pF ± 10%

Table 4.

If an external clock input is used instead of a crystal, the waveform (twice the clock rate) should exhibit a 50% ± 10% duty cycle. Note that the minimum clock input HIGH voltage level is Vcc-0.6V. The external clock input is connected to the EXTAL pin, while the XTAL pin is left open. Fig. 30 shows external clock interface.

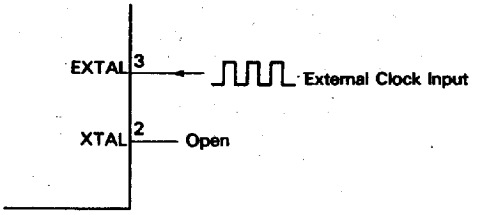


Figure 30. External Clock Interface

Miscellaneous

Free Running Counter (I/O Address = 18H)

Read only 8-bit free running counter without control registers and status registers. The contents of the 8-bit free running counter is counted down by one with an interval of 10 clock cycles. The free running counter continues counting down without being affected by the read operation.

If data is written into the free running counter, the interval of DRAM refresh cycle and baud rates for the ASCI and CSI/O are not guaranteed.

In IOSTOP mode, the free running counter continues counting down. It is initialized to FFH during RESET.

SOFTWARE ARCHITECTURE

Instruction Set. The Z180 is object code compatible with the Z80 CPU, refer to the Z80 CPU Technical Manual or the Z80 Assembly Language Programming Manual for further details.

New Instructions	Operation
SLP	Enter SLEEP mode
MLT	8-bit multiply with 16-bit result
INO g, (m)	Input contents of immediate I/O address
OUT0 (m), g	Output register contents to immediate I/O address
OTIM	Block output - increment
OTIMR	Block output - increment and repeat
OTDM	Block output - decrement
OTDMR	Block output - decrement and repeat
TSTIO m	Non-destructive AND, I/O port, and accumulator
TST g	Non-destructive AND, register, and accumulator
TST m	Non-destructive AND, immediate data and accumulator.
TST (HL)	Non-destructive AND, memory data, and accumulator.

SLP - Sleep. The SLP instruction causes the Z180 to enter the SLEEP low power consumption mode. See section 2.4 for a complete description of the SLEEP state.

MLT - Multiply. The MLT performs unsigned multiplication on two 8-bit numbers yielding a 16-bit result. MLT may specify BC, DE, HL or SP registers. In all cases, the 8-bit operands are loaded into each half of the 16-bit register and the 16-bit result is returned in that register.

OTIM, OTIMR, OTDM, OTDMR - Block I/O. The contents of memory pointed to by HL is output to the I/O address in (C). The memory address (HL) and I/O address (C) are incremented in OTIM and OTIMR and decremented in OTDM and OTDMR, respectively. The B register is decremented. The OTIMR and OTDMR variants repeat the above sequence until register B is decremented to 0. Since the I/O address (C) is automatically incremented or decremented, these instructions are useful for block I/O (such as Z180 on-chip I/O) initialization. When I/O is accessed, 00H is output in high-order bits of address automatically.

TSTIO m - Test I/O Port. The contents of the I/O port addressed by C are ANDed with immediately specified 8-bit data and the status flags are updated. The I/O port contents are not written (non-destructive AND). When I/O is accessed, 00H is output in higher bits of address automatically.

TST g - Test Register. The contents of the specified register are ANDed with the accumulator (A) and the status flags are updated. The accumulator and specified register are not changed (non-destructive AND).

TST m - Test Immediate. The contents of the immediately specified 8-bit data are ANDed with the accumulator (A) and the status flags are updated. The accumulator is not changed (non-destructive AND).

TST (HL) - Test Memory. The contents of memory pointed to by HL are ANDed with the accumulator (A) and the status flags are updated. The memory contents and accumulator are not changed (non-destructive AND).

INO g, (m) - Input, Immediate I/O address. The contents of immediately specified 8-bit I/O address are input into the specified register. When I/O is accessed, 00H is output in high-order bits of the address automatically.

OUTO (m), g - Output, Immediate I/O address. The contents of the specified register are output to the immediately specified 8-bit I/O address. When I/O is accessed, 00H is output in high-order bits of the address automatically.

CPU Registers

The Z180 CPU registers consist of Register Set GR, Register Set GR' and Special Registers.

The Register Set GR consists of 8-bit Accumulator (A), 8-bit Flag Register (F), and three General Purpose Registers (BC, DE, and HL) which may be treated as 16-bit registers (BC, DE, and HL) or as individual 8-bit registers (B, C, D, E, H, and L) depending on the instruction to be executed. The Register Set GR' is alternate register set of Register Set GR and also contains Accumulator (A'), Flag Register (F') and three General Purpose Registers (BC', DE', and HL'). While the alternate Register Set GR' contents are not directly accessible, the contents can be programmably exchanged at high speed with those of Register Set GR.

The Special Registers consist of 8-bit Interrupt Vector Register (I), 8-bit R Counter (R), two 16-bit Index Registers (IX and IY), 16-bit Stack Pointer (SP), and 16-bit Program Counter (PC).

Fig. 31 shows CPU registers configuration.

Register Set GR

Accumulator A	Flag Register F
B Register	C Register
D Register	E Register
H Register	L Register

General Purpose Registers

Register Set GR'

Accumulator A'	Flag Register F'
B' Register	C' Register
D' Register	E' Register
H' Register	L' Register

General Purpose Registers

Special Registers

Interrupt Vector Register I	R Counter R
Index Register IX	
Index Register IY	
Stack Pointer SP	
Program Counter PC	

Figure 31. CPU Registers

Z80180 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

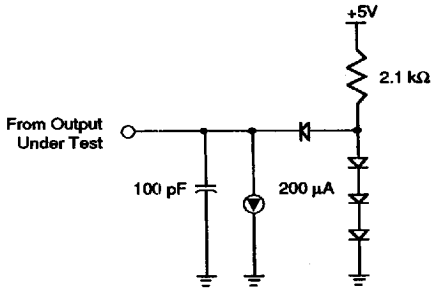
Item	Symbol		Value	Unit
Supply Voltage	V_{CC}		−0.3 ~ +7.0	V
Input Voltage	V_{in}		−0.3 ~ V_{CC}+0.3	V
Operating Temperature	Standard	Topr	0 - 70	°C
	Extended	Topr	-40 - 85	°C
Storage Temperature	T_{stg}		−55 ~ +150	°C

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

STANDARD TEST CONDITIONS

The DC Characteristics and Capacitance sections below apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin (Test Load Configuration).

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points).



Test Load Configuration

Z80180 DC CHARACTERISTICS

V_{CC}=5V ±10%, V_{SS}=0V, over specified temperature range unless otherwise noted.

Sym	Item	Condition	Min	Typ	Max	Unit
V_{IH1}	Input "H" Voltage /RESET, EXTAL /NMI		V_{CC} -0.6	-	V_{CC} +0.3	V
V_{IH2}	Input "H" Voltage except /RESET, EXTAL /NMI	2.0	-	V_{CC} +0.3	V	
V_{IL1}	Input "L" Voltage /RESET, EXTAL /NMI		-0.3	-	0.6	V
V_{IL2}	Input "L" Voltqge except /RESET, EXTAL /NMI	-0.3	-	0.8	V	
V_{OH}	Output "H" Voltage All outputs	I_{OH} = -200 µA	2.4	-	-	V
		I_{OH} = -20 µA	V_{CC} -1.2	-	-	V
V_{OL}	Output "L" Voltage All outputs	I_{OL} = 2.2 mA	-	-	0.45	V
V_{IL}	Input Leakage Current All inputs except XTAL, ETAL	V_{IN} = 0.5, V_{CC} -0.5	-	-	1.0	µA
I_{TL}	Tri-state Leakage Current	V_{IN} = 0.5, V_{CC} -0.5	-	-	1.0	µA
I_{CC}*	Power Dissipation* (Normal Operation)	f = 6 MHz	-	15	40	mA
		f = 8 MHz	-	20	50	mA
		f = 10 MHz	-	25	60	mA
	Power Dissipation* (SYSTEM STOP mode)	f = 6 MHz	-	3.8	12.5	mA
		f = 8 MHz	-	5	15.0	mA
		f = 10 MHz	-	6.3	17.5	mA
Cp	Pin Capacitance	V_{IN} = 0V, f = 1 MHz T_A = 25°C	-	-	12	pF

Notes:
*V_{IH}min = V_{CC} -1.0V, V_{IL}max = 0.8V (All output terminals are at no load.)
V_{CC} = 5.0V

Z80180 AC CHARACTERISTICS

(V_{CC}=5V ± 10%, V_{SS}=0V, over specified temperature range, unless otherwise noted.)

No	Sym	Parameter	Z8018006 Min	Z8018006 Max	Z8018008 Min	Z8018008 Max	Z8018010 Min	Z8018010 Max	Unit	Note
1	tcyc	Clock Cycle Time	162	2000	125	2000	100	2000	ns	[1]
2	tCHW	Clock Pulse Width (High)	65		55		40		ns	[1]
3	tCLW	Clock Pulse Width (Low)	65		55		40		ns	[1]
4	tcf	Clock Fall Time		15		15		10	ns	[1]
5	tcr	Clock Rise Time		15		15		10	ns	[1]
6	tAD	Address Vaild From Clock Rise		90		80		70	ns	
7	tAS	Address Valid To /MREQ, /IORQ Fall	30		20		10		ns	
8	tMED1	Clock Fall To /MREQ Fall Delay		60		50		50	ns	
9	tRDD1	Clock Fall To /RD Fall (/IOC=1)		60		50		50	ns	
		Clock Rise To /RD Fall (/IOC=0)		65		60		55	ns	
10	tM1D1	Clock Rise To /M1 Fall Delay		80		70		60	ns	
11	tAH	Address Hold Time (/MREQ, /IORQ, /RD, /WR)	35		20		10		ns	
12	tMED2	Clock Fall To /MREQ Rise Delay		60		50		50	ns	
13	tRDD2	Clock Fall To /RD Rise Delay		60		50		50	ns	
14	tM1D2	Clock Rise To /M1 Rise Delay		80		70		60	ns	
15	tDRS	Data Read Setup Time	40		30		25		ns	
16	tDRH	Data Read Hold time	0		0		0		ns	
17	tSTD1	Clock Edge To ST Fall		90		70		60	ns	
18	tSTD2	Clock Edge To ST Rise		90		70		60	ns	
19	tWS	/WAIT Setup Time To Clock Fall	40		40		30		ns	
20	tWH	/WAIT Hold Time From Clock Fall	40		40		30		ns	
21	tWDZ	Clock Rise To Data Float Delay		95		70		60	ns	
22	tWRD1	Clock Rise To /WR Fall Delay		65		60		50	ns	
23	tWDD	Clock Fall To Write Data Delay		90		80		60	ns	
24	tWDS	Write Data Setup Time To /WR	40		20		15		ns	
25	tWRD2	Clock Fall To /WR Rise		80		60		50	ns	
26	tWRP	/WR Pulse Width (Memory Write Cycles)	170		130		110		ns	
26a		/WR Pulse Width (I/O Write Cycles)	332		225		210		ns	
27	tWDH	Write Data Hold Time From /WR Rise	40		15		10		ns	
28	tIOD1	Clock Fall To /IORQ Fall Delay (/IOC=1)		60		50		50	ns	
		Clock Rise To /IORQ Fall Delay (/IOC=0)		65		60		55	ns	
29	tIOD2	Clock Fall /IOQR Rise Delay		60		50		50	ns	
30	tIOD3	/M1 Fall To /IORQ Fall Delay	340		250		200		ns	
31	tINTS	/INT Setup Time To Clock Fall	40		40		30		ns	
32	tINTH	/INT Hold Time From Clock Fall	40		40		30		ns	
33	tNMIW	/NMI Pulse Width	120		100		80		ns	
34	tBRS	/BUSREQ Setup Time To Clock Fall	40		40		30		ns	
35	tBRH	/BUSREQ Hold Time From Clock Fall	40		40		30		ns	
36	tBAD1	Clock Rise To /BUSACK Fall Delay		95		70		60	ns	
37	tBAD2	Clock Fall To /BUSACK Rise Delay		95		70		60	ns	
38	tBZD	Clock Rise To Bus Floating Delay Time		125		90		80	ns	
39	tMEWH	/MREQ Pulse Width (High)	110		90		70		ns	
40	tMEWL	/MREQ Pulse Width (Low)	125		100		80		ns	

Z80180 AC CHARACTERISTICS (Continued)

(V_{CC}=5V ± 10%, V_{SS}=0V, over specified temperature range, unless otherwise noted.)

No	Sym	Parameter	Z8018006 Min	Z8018006 Max	Z8018008 Min	Z8018008 Max	Z8018010 Min	Z8018010 Max	Unit	Note
41	tRFD1	Clock Rise To /RFSH Fall Delay		90		80		60	ns	
42	tRFD2	Clock Rise To /RFSH Rise Delay		90		80		60	ns	
43	tHAD1	Clock Rise To /HALT Fall Delay		90		80		50	ns	
44	tHAD2	Clock Rise To /HALT Rise Delay		90		80		50	ns	
45	tDRQS	/DREQi Setup Time To Clock Rise	40		40		30		ns	
46	tDRQH	/DREQi Hold Time From Clock Rise	40		40		30		ns	
47	tTED1	Clock Fall To /TENDi Fall Delay		70		60		50	ns	
48	tTED2	Clock Fall To /TENDi Rise Delay		70		60		50	ns	
49	tED1	Clock Rise To E Rise Delay		95		70		60	ns	
50	tED2	Clock Edge To E Fall Delay		95		70		60	ns	
51	PWEH	E Pulse Width (High)	75		65		55		ns	
52	PWEL	E Pulse Width (Low)	180		130		110		ns	
53	tEr	Enable Rise Time		20		20		20	ns	
54	tEf	Enable Fall Time		20		20		20	ns	
55	tTOD	Clock Fall To Timer Output Delay		300		200		150	ns	
56	tSTDI	CSI/O Tx Data Delay Time (Internal Clock Operation)		200		200		150	ns	
57	tSTDE	CSI/O Tx Data Delay Time (External Clock Operation)		7.5tcyc+300		7.5tcyc+200		7.5tcyc+150	ns	
58	tSRSI	CSI/O Rx Data Setup Time (Internal Clock Operation)	1		1		1		tcyc	
59	tSRHI	CSI/O Rx Data Hold Time (Internal Clock Operation)	1		1		1		tcyc	
60	tSRSE	CSI/O Rx Data Setup Time (External Clock Operation)	1		1		1		tcyc	
61	tSRHE	CSI/O Rx Data Hold Time (External Clock Operation)	1		1		1		tcyc	
62	tRES	/RESET Setup Time To Clock Fall	120		100		80		ns	
63	tREH	/RESET Hold Time From Clock Fall	80		70		50		ns	
64	tOSC	Oscillator Stabilization Time		20		20		20	ms	
65	tEXr	External Clock Rise Time (EXTAL)		25		25		15	ns	
66	tEXf	External Clock Fall Time (EXTAL)		25		25		15	ns	
67	tRr	/RESET Rise Time		50		50		50	ms	[2]
68	tRf	/RESET Fall Time		50		50		50	ms	[2]
69	tIr	Input Rise Time (Except EXTAL, /RESET)		100		100		100	ns	[2]
70	tIf	Input Fall Time (Except EXTAL, /RESET)		100		100		100	ns	[2]

Notes:

[1] tcyc=tCHW+tCLW+tcf+tcr

[2] This parameter has to be modified if other specification(s) cannot be met.

Z8S180 ELECTRICAL CHARACTERISTICS ABSOLUTE MAXIMUM RATINGS

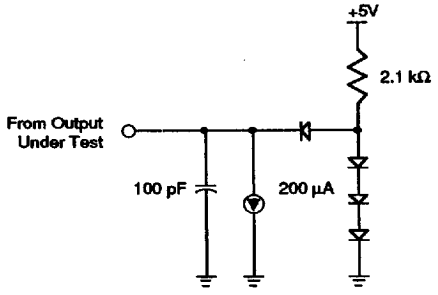
Symbol	Description	Min	Max	Unit
V_{CC}	Supply Voltage *	-0.3	+7.0	V
V_{IN}	Input Voltage	-0.3	V_{CC}+0.3	V
T_{OPR}	Operating Temp	-40	+100	C
T_{STG}	Storage Temp	-55	+150	C

Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

STANDARD TEST CONDITIONS

The DC Characteristics and Capacitance sections below apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin (Test Load Configuration).

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points).



Test Load Configuration

Z8S180 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, V_{SS}=0V, over specificied temperature range, unless otherwise noted.)

Symbol	Item	Condition	Min	Typ	Max	Unit
V_{IH1}	Input "H" Voltage Reset, EXTAL, NMI		V_{CC}-0.6		V_{CC}+0.3	V
V_{IH2}	Input "H" Voltage Except Reset, EXTAL, NMI		2.0		V_{CC}+0.3	V
V_{IL1}	Input "L" Voltage Reset, EXTAL, NMI		-0.3		0.6	V
V_{IL2}	Input "L" Voltage Except Reset, EXTAL, NMI		-0.3		0.8	V
V_{OH1}	Output "H" Voltage All Outputs	I_{OH} = -200 µA I_{OH} = -20 µA	2.4 V_{CC}-1.2			V V
V_{OH2}	Output "H" PHI	I_{OH} = -200 µA	V_{CC}-0.6			V
V_{OL1}	Output "L" Voltage All Outputs	I_{OL}= 2.2 mA			0.45	V
V_{OL2}	Output "L" PHI	I_{OL}=2.2 mA			0.45	V
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL	V_{IN}=0.5 to V_{CC}-0.5			1.0	µA
ITL	Tri-state Leakage Current	V_{IN}=0.5 to V_{CC}-0.5			1.0	µA
I_{CC}*	Power Dissipation (Normal Operation)	f = 16 MHz f = 20 MHz		45 50	100 120	mA mA
	Power Dissipation (System STOP mode)	f = 16 MHz f = 20 MHz		10 15	30 40	mA mA
	Power Dissipation (STANDBY Mode)	External Oscillator, Internal Clock Stops			10	µA
Cp	Pin Capacitance	V_{IN}=0V, f = 1 MHz T_A = 25°C			12	pF

Notes:

* V_{IH}min = V_{CC}-1.0V, V_{IL}max = 0.8V (all output termianls are at no load).
V_{CC}=5.0V

Z8S180 AC CHARACTERISTICS

(V_{CC}=5V ± 10%, V_{SS}=0V, over specified temperature range, unless otherwise noted.)

No	Sym	Parameter	Z8S18016 Min	Z8S18016 Max	Z8S18020 Min	Z8S18020 Max	Unit	Note
1	tcyc	Clock Cycle time	62	2000	50	2000	ns	[1]
2	tCHW	Clock Pulse width (high)	25		20		ns	[1]
3	tCLW	Clock Pulse width (low)	25		20		ns	[1]
4	tcf	Clock Fall time		6		5	ns	[1]
5	tcr	Clock Rise time		6		5	ns	[1]
6	tAD	Address vaild from Clock Rise		35		30	ns	
7	tAS	Address valid to /MREQ, /IORQ Fall	5		5		ns	
8	tMED1	Clock Fall to /MREQ Fall delay		25		25	ns	
9	tRDD1	Clock Fall to /RD Fall (/IOC=1)		25		25	ns	
		Clock Rise to /RD Fall (/IOC=0)		25		25	ns	
10	tM1D1	Clock Rise to /M1 Fall delay		45		35	ns	
11	tAH	Address Hold time (/MREQ, /IORQ, /RD, /WR)	5		5		ns	
12	tMED2	Clock Fall to /MREQ Rise Delay		30		25	ns	
13	tRDD2	Clock Fall to /RD Rise delay		30		25	ns	
14	tM1D2	Clock Rise to /M1 Rise delay		45		40	ns	
15	tDRS	Data Read Setup Time	15		10		ns	
16	tDRH	Data Read Hold time	0		0		ns	
17	tSTD1	Clock Edge to ST Fall		35		30	ns	
18	tSTD2	Clock Edge to ST Rise		35		30	ns	
19	tWS	/WAIT setup time to Clock Fall	15		15		ns	[2]
20	tWH	/WAIT Hold time from Clock Fall	10		10		ns	
21	tWDZ	Clock Rise to Data Float Delay		40		35	ns	
22	tWRD1	Clock Rise to /WR Fall delay		25		25	ns	
23	tWDD	Clock Fall to Write Data Delay		30		25	ns	
24	tWDS	Write Data Setup time to /WR	10		10		ns	
25	tWRD2	Clock Fall to /WR Rise		30		25	ns	
26	tWRP	/WR Pulse Width (Memory Write Cycles)	80		80		ns	
26a		/WR Pulse Width (I/O Write Cycles)	150		150		ns	
27	tWDH	Write Data Hold time from /WR Rise	10		10		ns	
28	tIOD1	Clock Fall to /IORQ Fall delay (/IOC=1)		30		25	ns	
		Clock Rise to /IORQ Fall delay (/IOC=0)		30		25	ns	
29	tIOD2	Clock Fall /IOQR Rise Delay		30		25	ns	
30	tIOD3	/M1 Fall to /IORQ Fall delay	120		100		ns	
31	tINTS	/INT Setup Time to Clock Fall	20		20		ns	
32	tINTH	/INT Hold Time from Clock Fall	10		10		ns	
33	tNMIW	/NMI Pulse width	40		35		ns	
34	tBRS	/BUSREQ Setup Time to Clock Fall	10		10		ns	
35	tBRH	/BUSREQ Hold Time from Clock Fall	10		10		ns	
36	tBAD1	Clock Rise to /BUSACK Fall delay		30		25	ns	
37	tBAD2	Clock Fall to /BUSACK Rise delay		30		25	ns	
38	tBZD	Clock Rise to Bus Floating Delay Time		45		40	ns	
39	tMEWH	/MREQ Pulse Width (High)	45		35		ns	
40	tMEWL	/MREQ Pulse Width (LOW)	45		35		ns	

Z8S180 AC CHARACTERISTICS (Continued)

(V_{cc}=5V ± 10%, V_{ss}=0V, over specified temperature range, unless otherwise noted.)

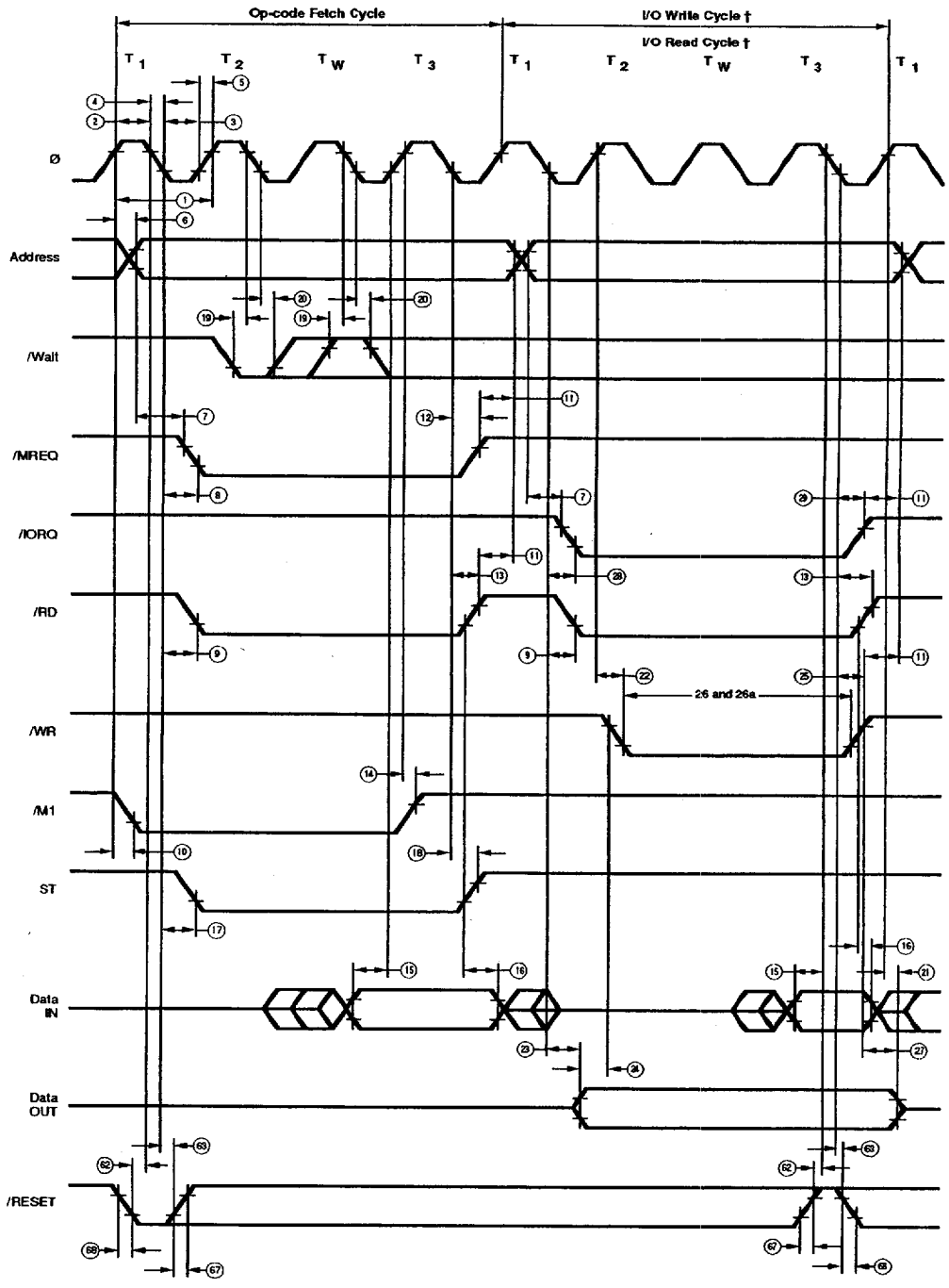
No	Sym	Parameter	Z8S18016 Min	Z8S18016 Max	Z8S18020 Min	Z8S18020 Max	Unit	Note
41	tRFD1	Clock Rise to /RFSH Fall Delay		25		20	ns	
42	tRFD2	Clock Rise to /RFSH Rise Delay		25		20	ns	
43	tHAD1	Clock Rise to /HALT Fall Delay		20		15	ns	
44	tHAD2	Clock Rise to /HALT Rise Delay		20		15	ns	
45	tDRQS	/DREQi Setup Time to Clock Rise	20		20		ns	
46	tDRQH	/DREQi Hold Time from Clock Rise	20		20		ns	
47	tTED1	Clock Fall to /TENDi Fall Delay		30		25	ns	
48	tTED2	Clock Fall to /TENDi Rise Delay		30		25	ns	
49	tED1	Clock Rise to E Rise Delay		35		30	ns	
50	tED2	Clock Edge to E Fall Delay		35		30	ns	
51	PWEH	E Pulse Width (High)	30		25		ns	
52	PWEL	E Pulse Width (Low)	60		50		ns	
53	tEr	Enable Rise Time		10		10	ns	
54	tEf	Enable Fall Time		10		10	ns	
55	tTOD	Clock Fall to Timer Output Delay		100		75	ns	
56	tSTDI	CSI/O Tx Data Delay Time (Internal Clock Operation)		100		75	ns	
57	tSTDE	CSI/O Tx Data Delay Time (External Clock Operation)		7.5 tcyc +100		7.5 tcyc+75	ns	
58	tSRSI	CSI/O Rx Data Setup Time (Internal Clock Operation)	1		1		tcyc	
59	tSRHI	CSI/O Rx Data Hold Time (Internal Clock Operation)	1		1		Tcyc	
60	tSRSE	CSI/O Rx Data Setup Time (External Clock Operation)	1		1		Tcyc	
61	tSRHE	CSI/O Rx Data Hold Time (External Clock Operation)	1		1		Tcyc	
62	tRES	/RESET Setup time to Clock Fall	45		40		ns	
63	tREH	/RESET Hold time from Clock Fall	30		25		ns	
64	tOSC	Oscillator Stabilization Time		20		20	ms	
65	tEXr	External Clock Rise Time (EXTAL)		6		5	ns	
66	tEXf	External Clock Fall Time (EXTAL)		6		5	ns	
67	tRr	/RESET Rise Time		50		50	ms	[2]
68	tRf	/RESET Fall Time		50		50	ms	[2]
69	tIr	Input Rise Time (Except EXTAL, /RESET)		50		50	ns	[2]
70	tIf	Input Fall Time (Except EXTAL, /RESET)		50		50	ns	[2]

Notes:

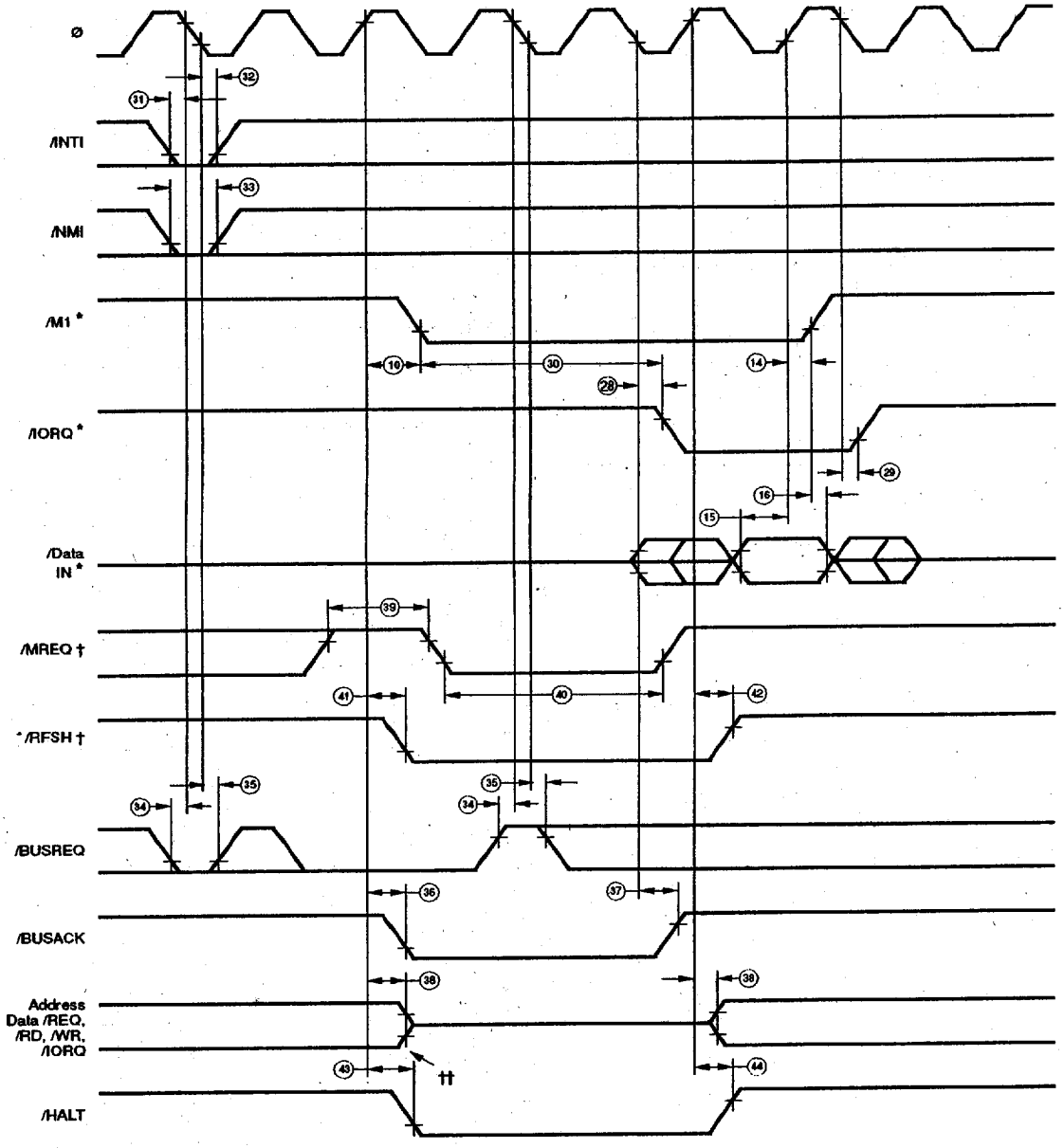
[1] tcyc=tCHW+tCLW+tcf+tcr

[2] This parameter has to be modified if other specification(s) can not be met.

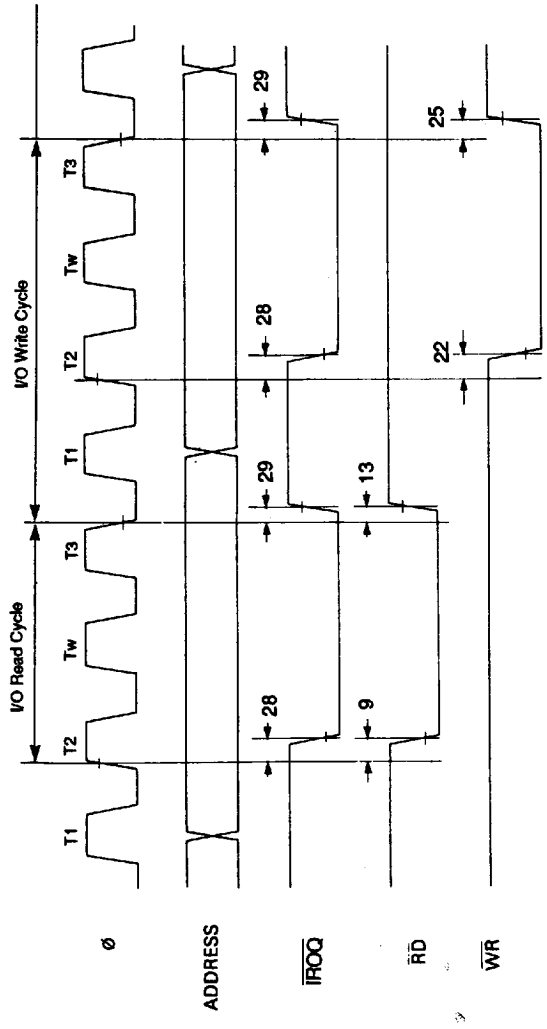
TIMING DIAGRAMS



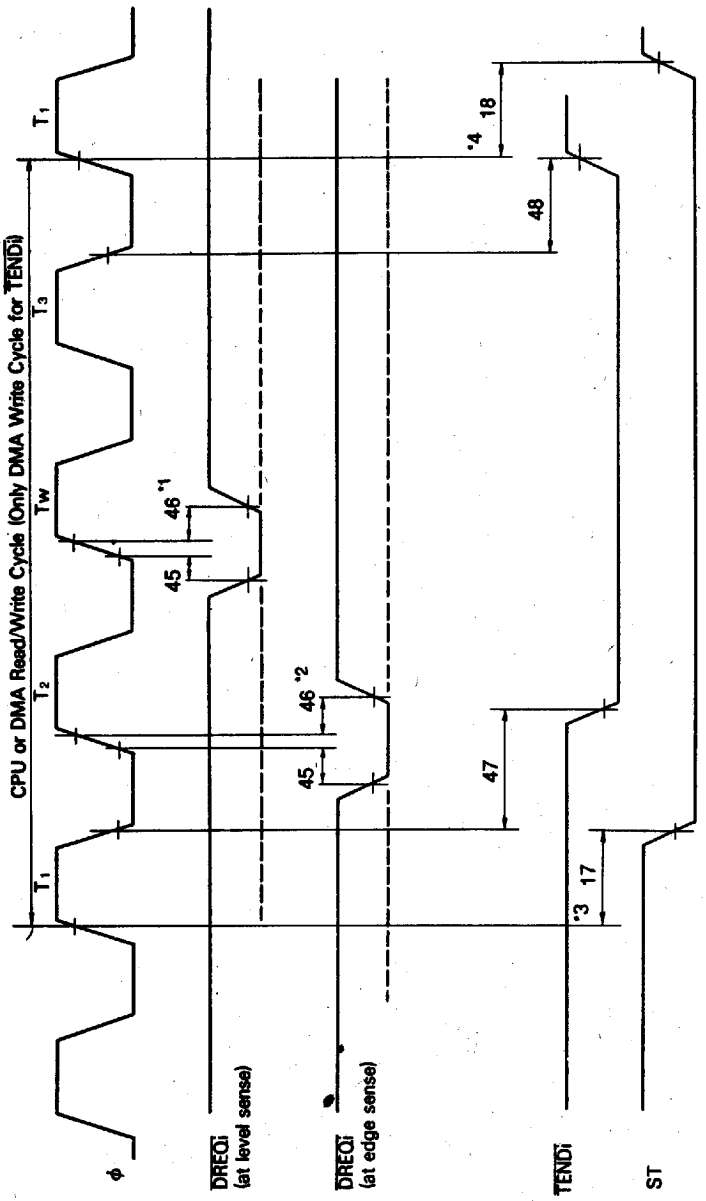
TIMING DIAGRAMS (Continued)



* During /INT Acknowledge Cycle
† During Refresh Cycle
†† Output Buffer Is Off At This Point

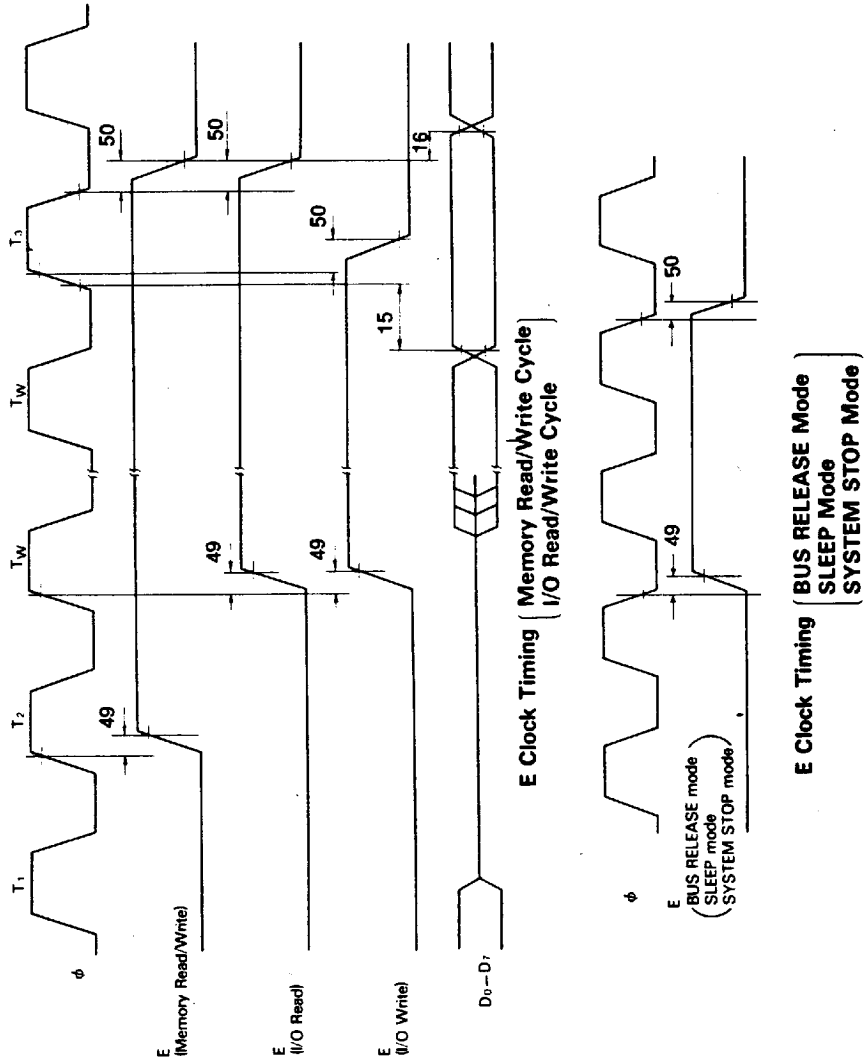


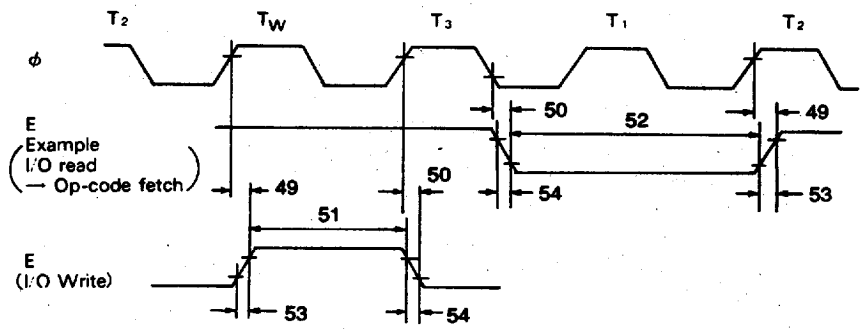
CPU Timing ($\overline{IOC}$=0)
- I/O Read Cycle
- I/O Write Cycle



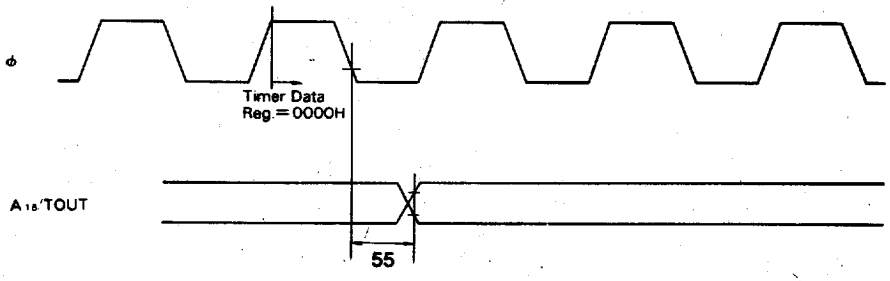
DMA Control Signals

*1 t_{DRQS} and t_{DRQH} are specified for the rising edge of clock followed by T_3.
*2 t_{DRQS} and t_{DRQH} are specified for the rising edge of clock.
*3 DMA cycle starts.
*4 CPU cycle starts.

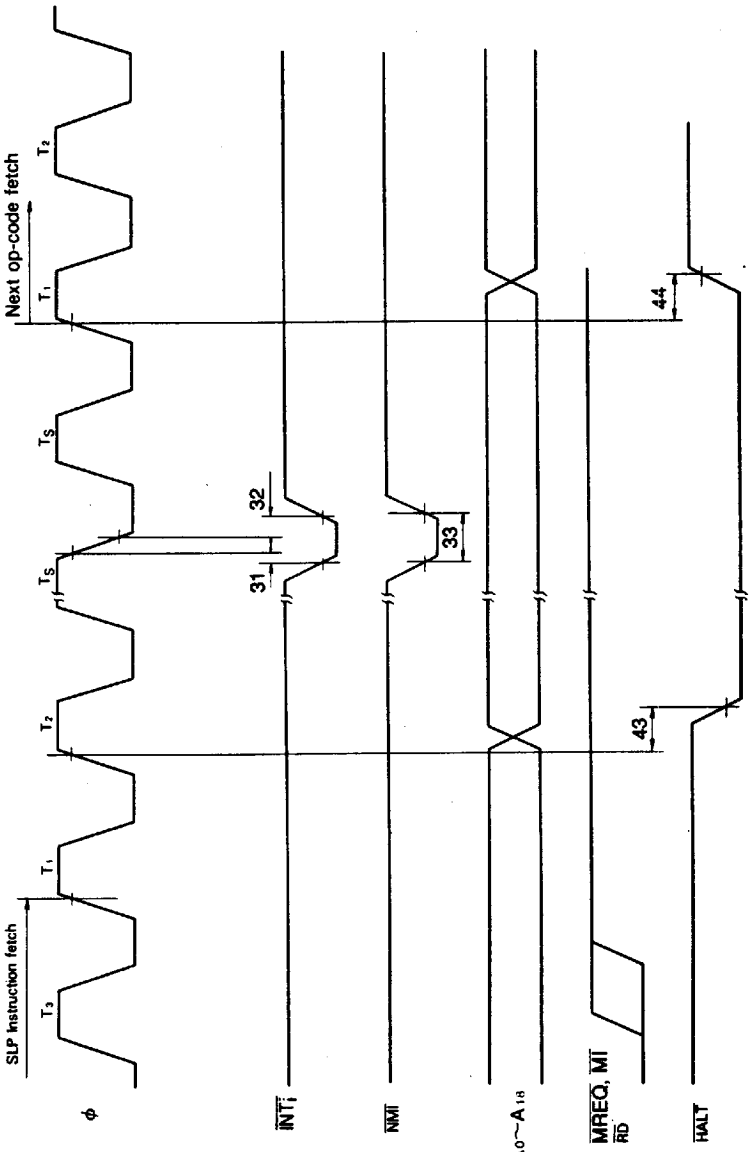




E Clock Timing (Minimum timing example of P_{WEL} and P_{WEH})



Timer Output Timing



SLP Execution Cycle

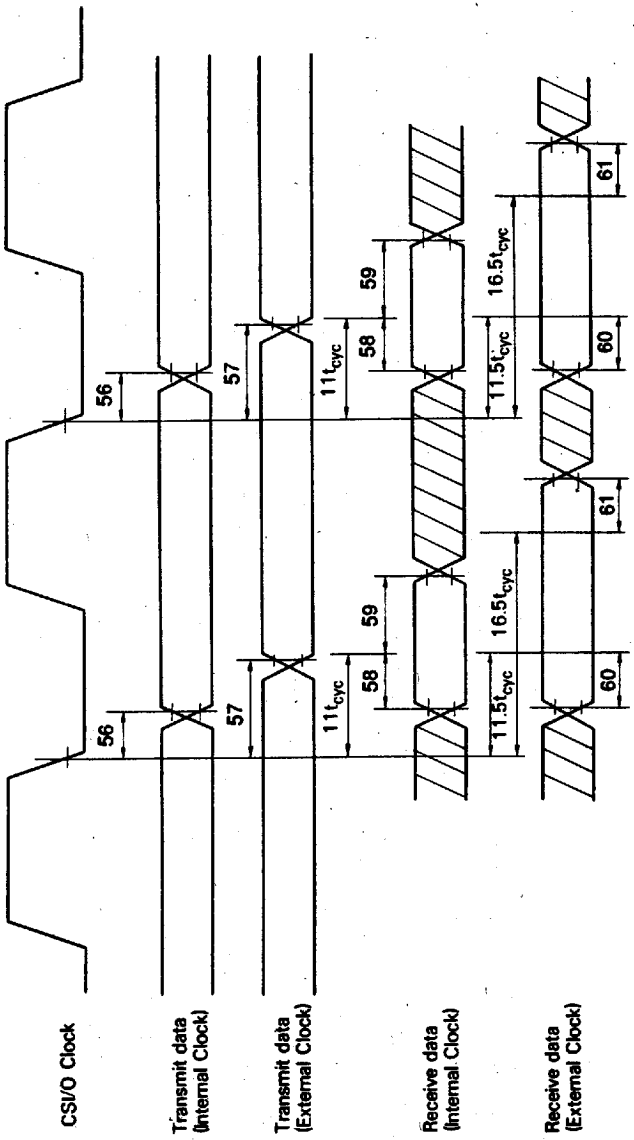
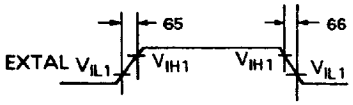


Figure 68. CSI/O Receive/Transmit Timing

TIMING DIAGRAMS (Continued)



External Clock Rise Time and Fall Time

Input Rise Time and Fall Time (Except EXTAL, $\overline{\text{RESET}}$)