Zero Power CMOS Hard Array Logic ZHAL™24A Series

Features/Benefits

- **Zero standby power**
- **Low power operation**
- **High-speed CMOS technology**
- **HC and HCT compatible**
- **24-pin SKINNYDIP® and 28-pin PLCC packages save space**
- **Low power alternative for most 24-pin PAL® devices, including 20L8/ 20R8/ 20R6/ 20R4**

Description

This family of Zero Power Hard Array Logic (ZHAL) devices utilizes a unique architecture that is designed for a high degree of flexibility in implementing most patterns of the listed 24-pin PAL/HAL® devices. Prototyping should be done using standard PAL devices before converting to ZHAL circuits for production. ZHAL devices are fabricated by Monolithic Memories with custom metallization masks defined by a user-supplied HAL Design Specification.

The ZHAL devices are ideal in low-power applications that require high-speed operation. These attributes are achieved through the use of Monolithic Memories' advanced high-speed CMOS process. Now system designers have the option of using a ZHAL device that matches fast PAL device speeds, but with the added feature of zero standby power. These features are needed in power-critical areas such as portable digital equipment or lap-top computers.

Ordering Information

PART NUMBER	PACKAGE	ARRAY INPUTS	OUTPUTS	
			COMB	REG
ZHAL12L10A	NS, NL	12	10	—
ZHAL14L8A	NS, NL	14	8	—
ZHAL16L6A	NS, NL	16	6	—
ZHAL18L4A	NS, NL	18	4	—
ZHAL20L2A	NS, NL	20	2	—
ZHAL20C1A	NS, NL	20	2	—
ZHAL20L8A	NS, NL	20	8	—
ZHAL20R8A	NS, NL	20	—	8
ZHAL20R6A	NS, NL	20	2	6
ZHAL20R4A	NS, NL	20	4	4
ZHAL20L10A	NS, NL	20	10	—
ZHAL20X10A	NS, NL	20	—	10
ZHAL20X8A	NS, NL	20	2	8
ZHAL20X4A	NS, NL	20	6	4
ZHAL20S10A	NS, NL	20	10	—
ZHAL20RS10A	NS, NL	20	—	10
ZHAL20RS8A	NS, NL	20	2	8
ZHAL20RS4A	NS, NL	20	6	4

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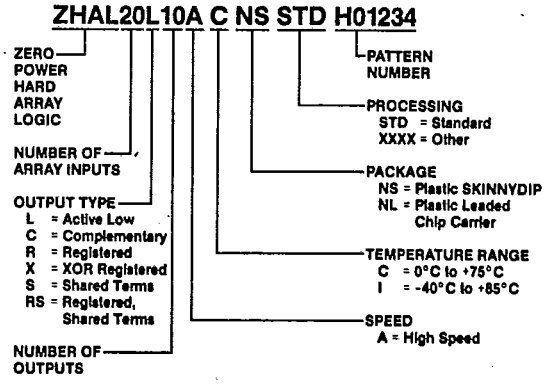

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Pin Configurations — DIP and PLCC

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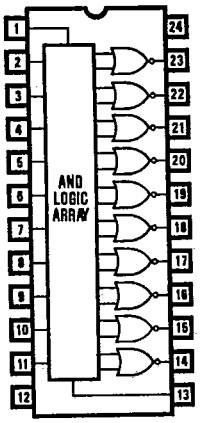

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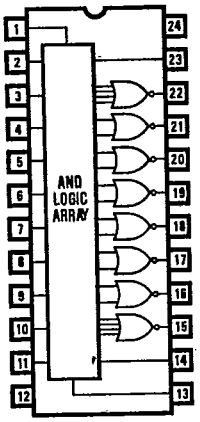

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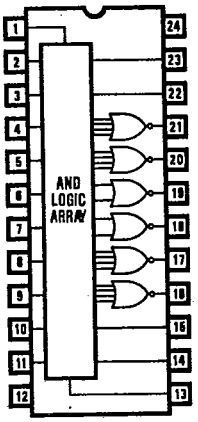

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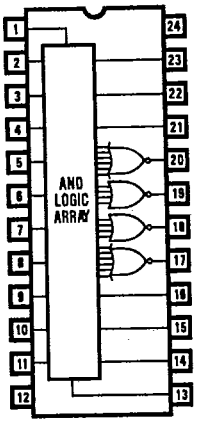

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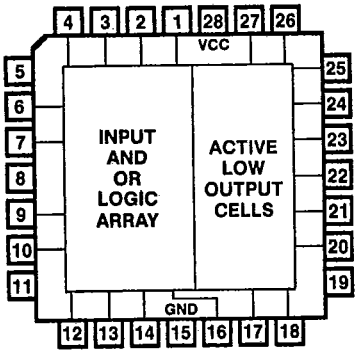

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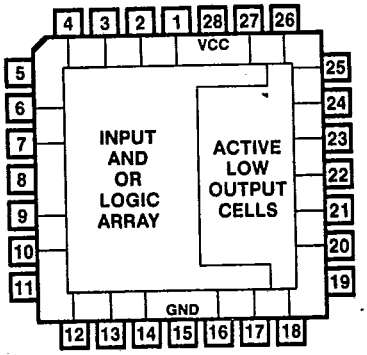

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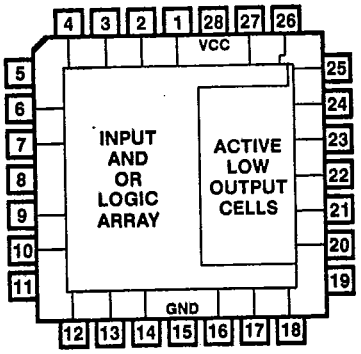

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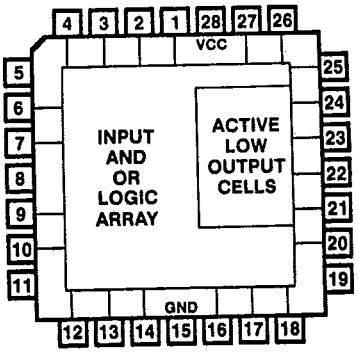

Pin Configurations — DIP and PLCC

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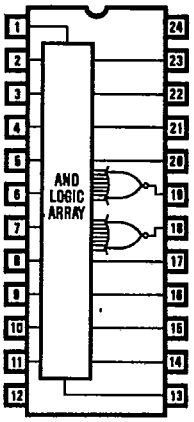

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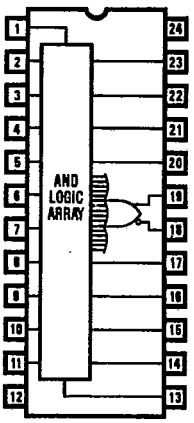

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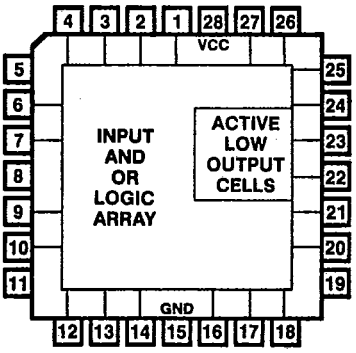

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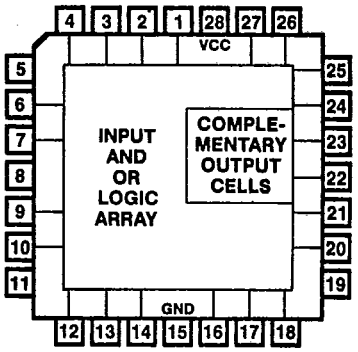

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Pin Configurations — DIP and PLCC

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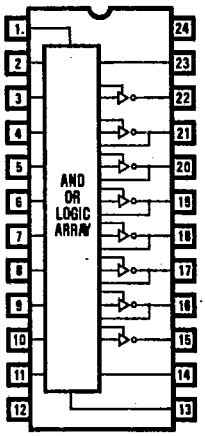

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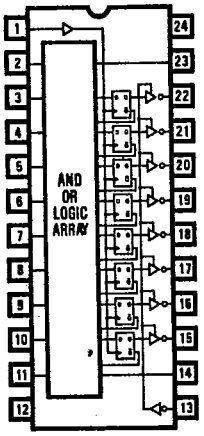

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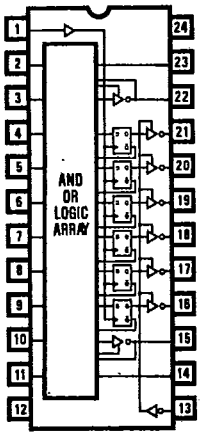

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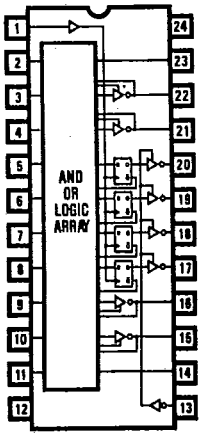

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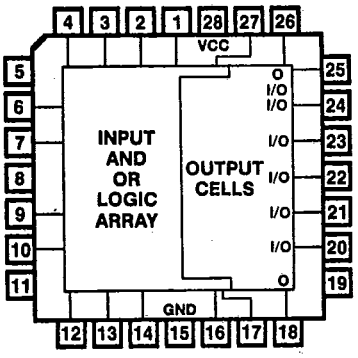

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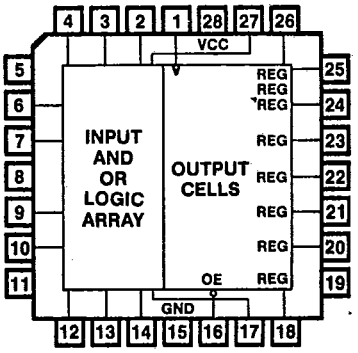

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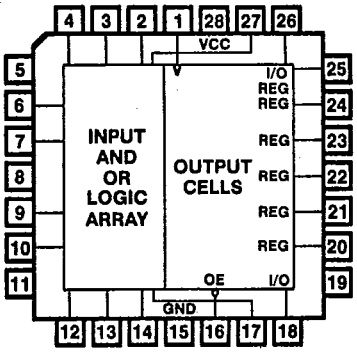

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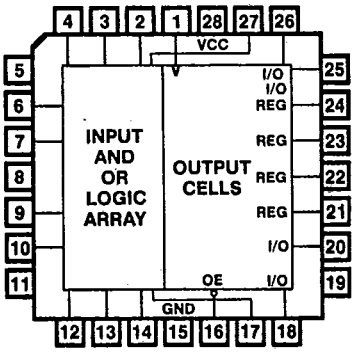

Pin Configurations — DIP and PLCC

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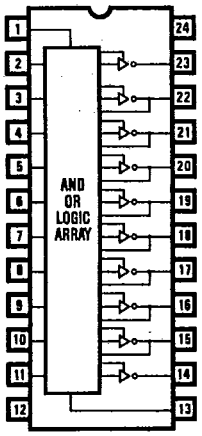

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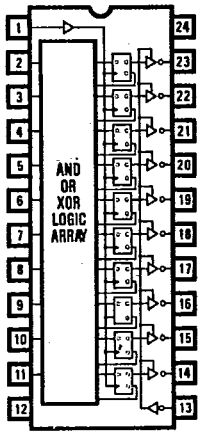

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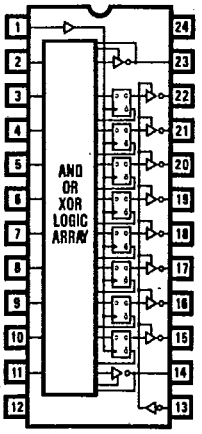

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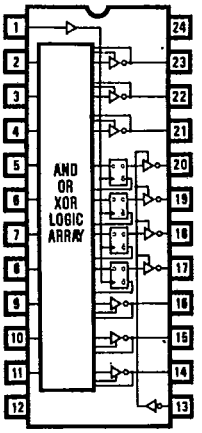

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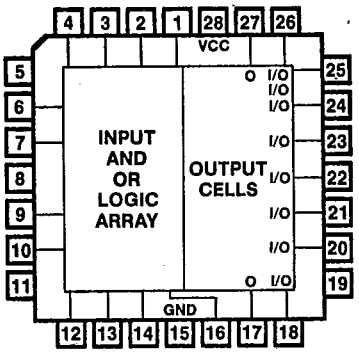

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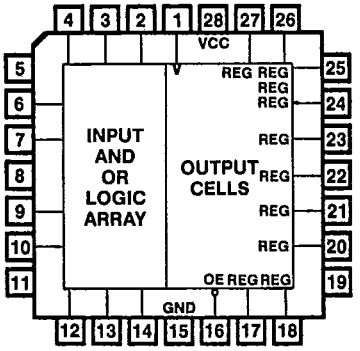

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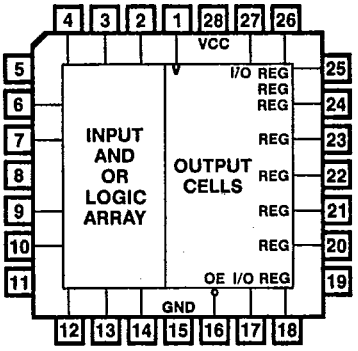

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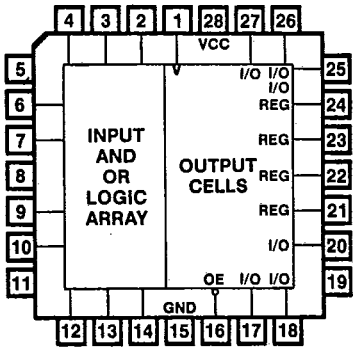

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Pin Configurations — DIP and PLCC

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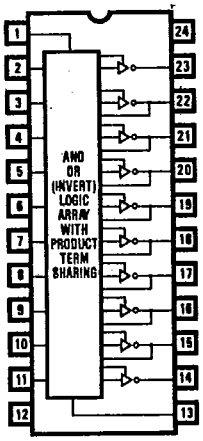

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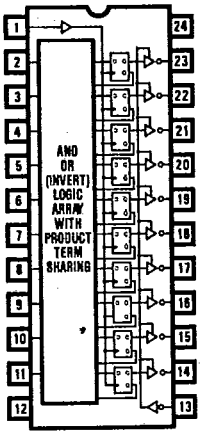

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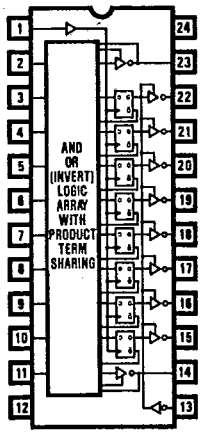

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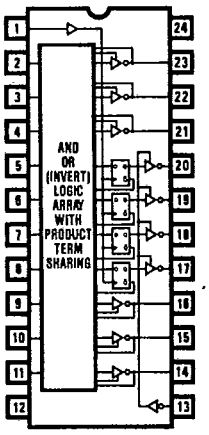

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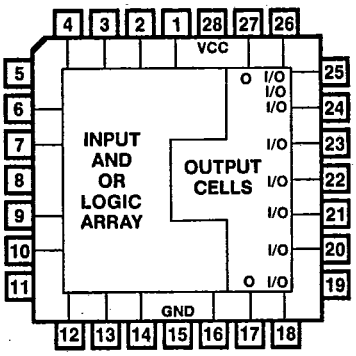

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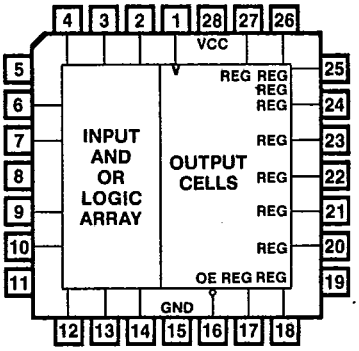

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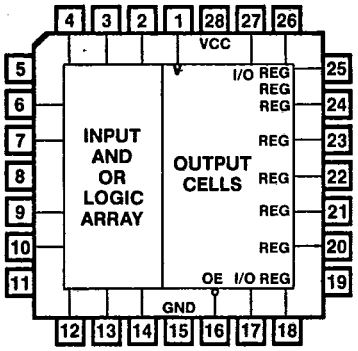

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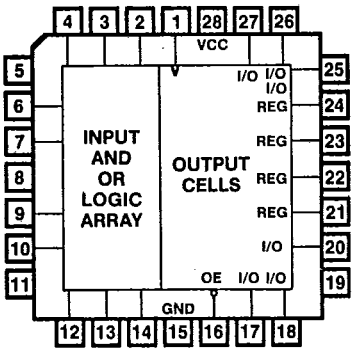

Operating Conditions

SYMBOL	PARAMETER	INDUSTRIAL MIN	INDUSTRIAL TYP	INDUSTRIAL MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–40	25	85	0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage			0		0.8	V
V_{IH}[1]	High-level input voltage			2		V_{CC}	V
I_{IL}	Low-level input current	V_{CC} = MAX V_I = GND				–1	μA
I_{IH}	High-level input current	V_{CC} = MAX V_I = V_{CC}				1	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8 mA		0.1	0.4	V
		V_{CC} = 5 V	I_{OL} = 1 μA			0.05	
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = –6 mA	3.76[2]	4.1		V
		V_{CC} = 5 V	I_{OH} = –1 μA	4.95			
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = GND		0	–10	μA
I_{OZH}[3]			V_O = V_{CC}		0	10	μA
I_{CC}	Standby supply current[4]	I_O = 0 mA, V_I = GND or V_{CC}			0	100	μA
	Operating supply current	f = 1 MHz, I_O = 0 mA, V_I = GND or V_{CC}			2	5[5]	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	INDUSTRIAL MIN	INDUSTRIAL TYP	INDUSTRIAL MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input to output	R_L = 1 KΩ C_L = 50 pF		13	25[6]		13	25[6]	ns

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Notes:
1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. JEDEC standard no. 7 for high-speed CMOS devices.
3. Applies to pins 14-23 for DIP (pins 17, 18, 20-27 for PLCC).
4. Disable output pins = V_{CC} or GND.
5. Add 3 mA per additional 1.0 MHz of operation over 1 MHz.
6. For outputs with more than 12 inputs in a product term, t_{PD} = 30 ns.

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Operating Conditions

SYMBOL	PARAMETER		INDUSTRIAL MIN	INDUSTRIAL TYP	INDUSTRIAL MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	20R8A, 20R6A, 20R4A	15	4		15	4		ns
t_{su}	Setup time from input or feedback to clock		20[1]	11		20[1]	11		ns
t_h	Hold time		0	-10		0	-10		ns
T_A	Operating free-air temperature		-40	25	85	0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage				0		0.8	V
V_{IH}[2]	High-level input voltage				2		V_{CC}	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = GND			-1	μA
I_{IH}	High-level input current	Pin 10[3]	V_{CC} = MAX	V_I = V_{CC}		8	30	μA
		All other pins					1	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8 mA		0.1	0.4	V
			V_{CC} = 5 V	I_{OL} = 1 μA			0.05	
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = -6 mA	3.76[4]	4.1		V
			V_{CC} = 5 V	I_{OH} = -1 μA	4.95			
I_{OZL}[5]	Off-state output current		V_{CC} = MAX	V_O = GND		0	-10	μA
I_{OZH}[5]				V_O = V_{CC}		0	10	μA
I_{CC}	Standby supply current[6]		I_O = 0 mA, V_I = GND or V_{CC}			0	100	μA
	Operating supply current		f = 1 MHz, I_O = 0 mA, V_I = GND or V_{CC}			2	5[7]	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS (See Test Load)	INDUSTRIAL MIN	INDUSTRIAL TYP	INDUSTRIAL MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output 20L8A, 20R6A, 20R4A		R_L = 1 KΩ C_L = 50 pF		13	25[1]		13	25[1]	ns
t_{CLK}	Clock to output or feedback 20R8A, 20R6A, 20R4A				8	15		8	15	ns
t_{PZX}	Input to output enable	20L8A, 20R6A, 20R4A			12	25		12	25	ns
t_{PXZ}[8]	Input to output disable				12	25		12	25	ns
t_{PXZ}[8] / t_{PZX}	Pin 13 (DIP) to output disable/enable	20R8A, 20R6A, 20R4A			10	20		10	20	ns
f_{MAX}	Maximum frequency			28.5	40		28.5	40		MHz

Notes:
1. For outputs with more than 12 inputs in a product term, t_{SU} = 25 ns and t_{PD} = 30 ns.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Pin 10 DIP, pin 13 PLCC (PRELOAD pin). Applies to registered devices only.
4. JEDEC standard no. 7 for high-speed CMOS devices.
5. Applies to pins 14-23 for DIP (pins 17, 18, 20-27 for PLCC).
6. Disable output pins = V_{CC} or GND.
7. Add 3 mA per additional 1.0 MHz of operation over 1 MHz.
8. C_L = 5 pF.

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Operating Conditions

SYMBOL	PARAMETER		INDUSTRIAL MIN	INDUSTRIAL TYP	INDUSTRIAL MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	20X10A, 20X8A, 20X4A	15	5		15	5		ns
t_{su}	Setup time from input or feedback to clock		25[1]	15		25[1]	15		ns
t_h	Hold time		0	-10		0	-10		ns
T_A	Operating free-air temperature		-40	25	85	0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage				0		0.8	V
V_{IH}[2]	High-level input voltage				2		V_{CC}	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = GND			-1	μA
I_{IH}	High-level input current	Pin 10[3]	V_{CC} = MAX	V_I = V_{CC}		8	30	μA
		All other pins					1	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8 mA		0.1	0.4	V
			V_{CC} = 5 V	I_{OL} = 1 μA			0.05	
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = -6 mA	3.76[4]	4.1		V
			V_{CC} = 5 V	I_{OH} = -1 μA	4.95			
I_{OZL}[5]	Off-state output current		V_{CC} = MAX	V_O = GND		0	-10	μA
I_{OZH}[5]				V_O = V_{CC}		0	10	μA
I_{CC}	Standby supply current[6]		I_O = 0 mA, V_I = GND or V_{CC}			0	100	μA
	Operating supply current		f = 1 MHz, I_O = 0 mA, V_I = GND or V_{CC}			2	5[7]	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS (See Test Load)	INDUSTRIAL MIN	INDUSTRIAL TYP	INDUSTRIAL MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output 20L10A, 20X8A, 20X4A		R_L = 1 KΩ C_L = 50 pF		13	25[1]		13	25[1]	ns
t_{CLK}	Clock to output or feedback 20X10A, 20X8A 20X4A				10	15		10	15	ns
t_{PZX}	Input to output enable	20L10A, 20X8A, 20X4A			12	25		12	25	ns
t_{PXZ}[8]	Input to output disable				12	25		12	25	ns
t_{PXZ}[8] / t_{PZX}	Pin 13 (DIP) to output disable/enable	20X10A, 20X8A, 20X4A			15	20		15	20	ns
f_{MAX}	Maximum frequency			22.2	32		22.2	32		MHz

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Notes:
1. For outputs with more than 12 inputs in a product term, t_{SU} = 30 ns and t_{PD} = 30 ns.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Pin 10 DIP, pin 13 PLCC (PRELOAD pin). Applies to registered devices only.
4. JEDEC standard no. 7 for high-speed CMOS devices.
5. Applies to pins 14-23 for DIP (pins 17, 18, 20-27 for PLCC).
6. Disable output pins = V_{CC} or GND.
7. Add 3 mA per additional 1.0 MHz of operation over 1 MHz.
8. C_L = 5 pF.

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Operating Conditions

SYMBOL	PARAMETER		INDUSTRIAL MIN	INDUSTRIAL TYP	INDUSTRIAL MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	20RS10A, 20RS8A, 20RS4A	15	4		15	4		ns
t_{su}	Setup time for input to clock		20[1]	11		20[1]	11		ns
t_h	Hold time		0	-10		0	-10		ns
T_A	Operating free-air temperature		-40	25	85	0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage				0		0.8	V
V_{IH}[2]	High-level input voltage				2		V_{CC}	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = GND			-1	μA
I_{IH}	High-level input current	Pin 10[3]	V_{CC} = MAX	V_I = V_{CC}		8	30	μA
		All other pins					1	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8 mA		0.1	0.4	V
			V_{CC} = 5 V	I_{OL} = 1 μA			0.05	
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = -6 mA	3.76[4]	4.1		V
			V_{CC} = 5 V	I_{OH} = -1 μA	4.95			
I_{OZL}[5]	Off-state output current		V_{CC} = MAX	V_O = GND		0	-10	μA
I_{OZH}[5]				V_O = V_{CC}		0	10	μA
I_{CC}	Standby supply current[6]		I_O = 0 mA, V_I = GND or V_{CC}			0	100	μA
	Operating supply current		f = 1 MHz, I_O = 0 mA, V_I = GND or V_{CC}			2	5[7]	mA

Switching Characteristics Over Operating Conditions

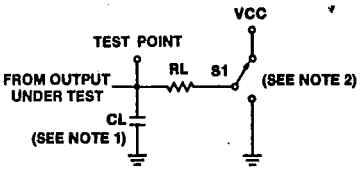
SYMBOL	PARAMETER		TEST CONDITIONS (See Test Load)	INDUSTRIAL MIN	INDUSTRIAL TYP	INDUSTRIAL MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output 20S10A, 20RS8A, 20RS4A		R_L = 1 KΩ C_L = 50 pF		13	25[1]		13	25[1]	ns
t_{CLK}	Clock to output or feedback 20RS10A, 20RS8A, 20RS4A				8	15		8	15	ns
t_{PZX}	Input to output enable	20S10A, 20RS8A, 20RS4A			12	25		12	25	ns
t_{PXZ}[8]	Input to output disable				12	25		12	25	ns
t_{PXZ}[8]	Pin 13 (DIP) to output disable/enable	20RS10A, 20RS8A, 20RS4A			10	20		10	20	ns
t_{PZX}										
f_{MAX}	Maximum frequency			28.5	40		28.5	40		MHz

Notes:
1. For outputs with more than 12 inputs in a product term, t_{SU} = 25 ns and t_{PD} = 30 ns.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Pin 10 DIP, pin 13 PLCC (PRELOAD pin). Applies to registered devices only.
4. JEDEC standard no. 7 for high-speed CMOS devices.
5. Applies to pins 14-23 for DIP (pins 17, 18, 20-27 for PLCC).
6. Disable output pins = V_{CC} or GND.
7. Add 3 mA per additional 1.0 MHz of operation over 1 MHz.
8. C_L = 5 pF.

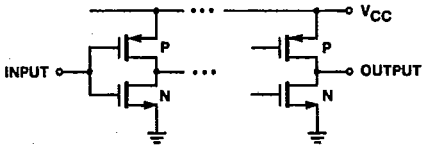
Absolute Maximum Ratings

Supply voltage, V_{CC} ..... -0.5 V to 7 V
DC input voltage, V_I ..... -0.5 V to V_{CC} +0.5 V
DC output voltage, V_O ..... -0.5 V to V_{CC} +0.5 V
DC output source/sink current per output pin, I_O ..... ±35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} ..... ±100 mA
Input diode current, I_{IK}:
V_I<0 ..... -20 mA
V_I>V_{CC} ..... +20 mA
Output diode current, I_{OK}:
V_O<0 ..... -20 mA
V_O>V_{CC} ..... +20 mA
Storage temperature ..... -65°C to +150°C

Switching Test Load



Schematic of Inputs and Outputs



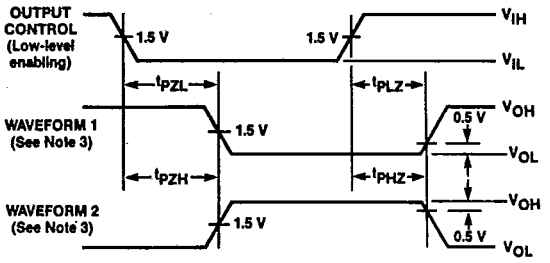
Output Register PRELOAD†

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing of state sequencer designs by allowing direct setting of output states for improved test coverage. The procedure for PRELOAD using DIP pin numbers, is as follows:

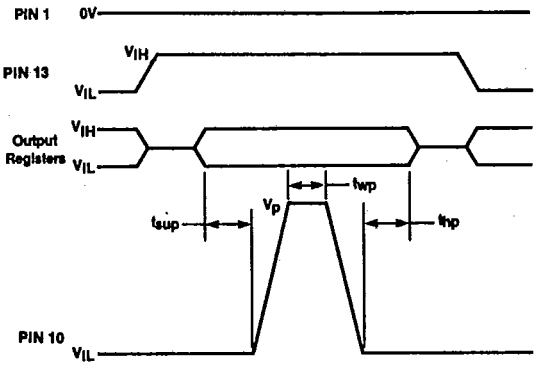
1. Raise V_{CC} to 4.5 V.
2. Disable output registers by setting pin 13 to V_{IH}. Set pin 1 to 0 V.
3. Apply V_{IL}/V_{IH} to all registered outputs.
4. Pulse pin 10 to V_p (12 V), then back to 0 V.
5. Remove V_{IL}/V_{IH} from all registered outputs.
6. Lower pin 13 to V_{IL} to enable the output registers.
7. Verify for V_{OL}/V_{OH} at all registered outputs.

† Note: Only applies to parts with output registers.
Typical t_{sup} = 50 ns
t_{wp} = 100 ns
t_{hp} = 50 ns
I_{IH} = 30μA (Pin 10)

Enable/Disable Delay



Notes: 1. CL includes probe and jig capacitance.
2. When measuring t_{PLZ} and t_{PZL}, S1 is tied to V_{CC}.
When measuring t_{PHZ} and t_{PZH}, S1 is tied to ground.
t_{PZX} is measured with C_L = 50 pF. t_{PXZ} is measured with C_L = 5 pF.
When measuring propagation delay times of three-state outputs, S1 is open, i.e., not connected to V_{CC} or ground.
3. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.



Zero Power
CMOS Hard Array Logic
ZHAL™24A Series

ZHAL24A Evaluation #4

Features/Benefits

- **Demonstration pattern for ZHAL24A Series (ZHAL20X8A)**
- **8-bit counter**
- **Three-state output**
- **Expandable in 8-bit increments**
- **Equivalent to 74ACT461**

Description

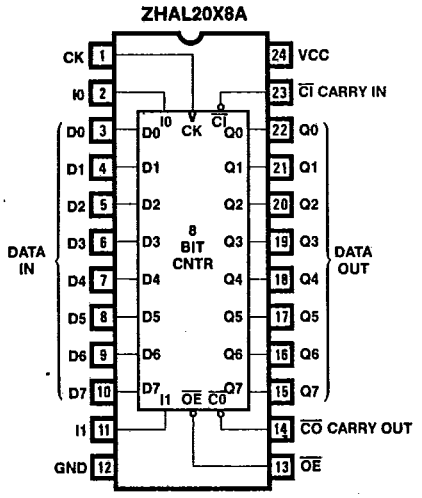
The ZHAL24A Evaluation #4 pattern is provided as an example of the features and characteristics of the ZHAL24A Series products. The design consists of an 8-bit synchronous counter with parallel load, clear, and hold capability. Two function select inputs (I0, I1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0). The CLEAR operation resets the output register to all LOWs. The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CI}$ = LOW), otherwise the operation is a HOLD. The carry-out ($\overline{CO}$) is TRUE ($\overline{CO}$ = LOW) when the output register (Q7-Q0) is all HIGHs, otherwise FALSE ($\overline{CO}$ = HIGH).

The data output pins are enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH.

Two or more 8-bit counters may be cascaded to provide larger counters. The operation codes were chosen such that when I1 is HIGH, I0 may be used to select between LOAD and INCREMENT as in a program counter (JUMP/INCREMENT).

Logic Symbol



Function Table

$\overline{OE}$	CK	I1	I0	$\overline{CI}$	D7-D0	Q7-Q0	OPERATION
H	*	*	*	*	*	Z	HI-Z*
L	↑	L	L	X	X	L	CLEAR
L	↑	L	H	X	X	Q	HOLD
L	↑	H	L	X	D	D	LOAD
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q plus 1	INCREMENT

*When $\overline{OE}$ is HIGH, the three-state outputs are disabled to the high-impedance states; however, sequential operation of the counter is not affected.

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance (off) state
↑ = LOW-to-HIGH clock transition

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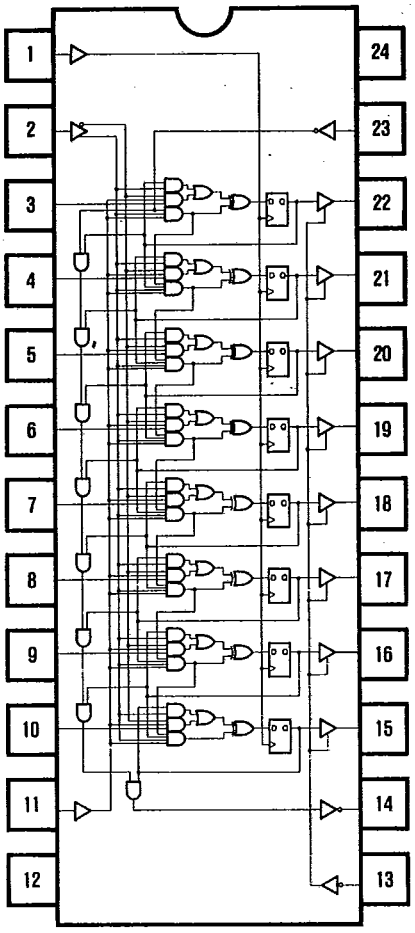
Logic Diagram

ZHAL20X8A



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```
Title     ZHAL24A Evaluation 4 (74ACT461)
Pattern   P7023
Revision  B
Author    Birkner/Kazmi/Blasco
Company   Monolithic Memories, Inc.
Date      1986

CHIP ZHAL24A_Evaluation_4 PAL20X8

CK   I0 D0 D1 D2 D3 D4 D5 D6 D7  I1 GND
/OE /CO Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0 /CI VCC

EQUATIONS

/Q0 :=  /I1*/I0                              ;CLEAR LSB
     +       I0*/Q0                          ;COUNT/HOLD
    :+:  I1*/I0*/D0                          ;LOAD D0 (LSB)
     +   I1* I0* CI                          ;COUNT

/Q1 :=  /I1*/I0                              ;CLEAR
     +       I0*/Q1                          ;COUNT/HOLD
    :+:  I1*/I0*/D1                          ;LOAD D1
     +   I1* I0* CI*Q0                       ;COUNT

/Q2 :=  /I1*/I0                              ;CLEAR
     +       I0*/Q2                          ;COUNT/HOLD
    :+:  I1*/I0*/D2                          ;LOAD D2
     +   I1* I0* CI*Q0*Q1                    ;COUNT

/Q3 :=  /I1*/I0                              ;CLEAR
     +       I0*/Q3                          ;COUNT/HOLD
    :+:  I1*/I0*/D3                          ;LOAD D3
     +   I1* I0* CI*Q0*Q1*Q2                 ;COUNT

/Q4 :=  /I1*/I0                              ;CLEAR
     +       I0*/Q4                          ;COUNT/HOLD
    :+:  I1*/I0*/D4                          ;LOAD D4
     +   I1* I0* CI*Q0*Q1*Q2*Q3              ;COUNT

/Q5 :=  /I1*/I0                              ;CLEAR
     +       I0*/Q5                          ;COUNT/HOLD
    :+:  I1*/I0*/D5                          ;LOAD D5
     +   I1* I0* CI*Q0*Q1*Q2*Q3*Q4           ;COUNT

/Q6 :=  /I1*/I0                              ;CLEAR
     +       I0*/Q6                          ;COUNT/HOLD
    :+:  I1*/I0*/D6                          ;LOAD D6
     +   I1* I0* CI*Q0*Q1*Q2*Q3*Q4*Q5        ;COUNT

/Q7 :=  /I1*/I0                              ;CLEAR MSB
     +       I0*/Q7                          ;COUNT/HOLD
    :+:  I1*/I0*/D7                          ;LOAD D7 (MSB)
     +   I1* I0* CI*Q0*Q1*Q2*Q3*Q4*Q5*Q6     ;COUNT

IF (VCC)  CO = CI*Q0*Q1*Q2*Q3*Q4*Q5*Q6*Q7    ;CARRY OUT
```