

Features

- Very High Operating Speed
- Operation down to DC with Square Wave Input
- Low Phase Noise (Typically better than -150dBc/Hz at 1kHz)
- 5V Single Supply Operation
- Low Power Dissipation: 420mW (Typ)
- Surface Mount Plastic Package With Exposed Pad (See Application Notes)

Applications

- DC to 10 GHz PLL applications
- HyperLan
- LMDS
- Instrumentation
- Satellite Communications
- Fibre Optic Communications; OC48, OC192
- Ultra Low Jitter Clock Systems

Issue 1

November 2002

Ordering Information

ZL40812/DCE (tubes) 8 lead e-pad SOIC
 ZL40812/DCF (tape and reel) 8 lead e-pad SOIC

-40°C to +85°C

Description

Description The ZL40812 is one of a range of 5V supply, very high speed low power prescalers for professional applications with a fixed modulus of divide by 16. The dividing elements are static D type flip flops and therefore allow operation down to DC if the drive signal is a pulse waveform with fast risetimes. The output stage has internal 50 ohm pull up giving a 1V p-p output. See application notes for more details.

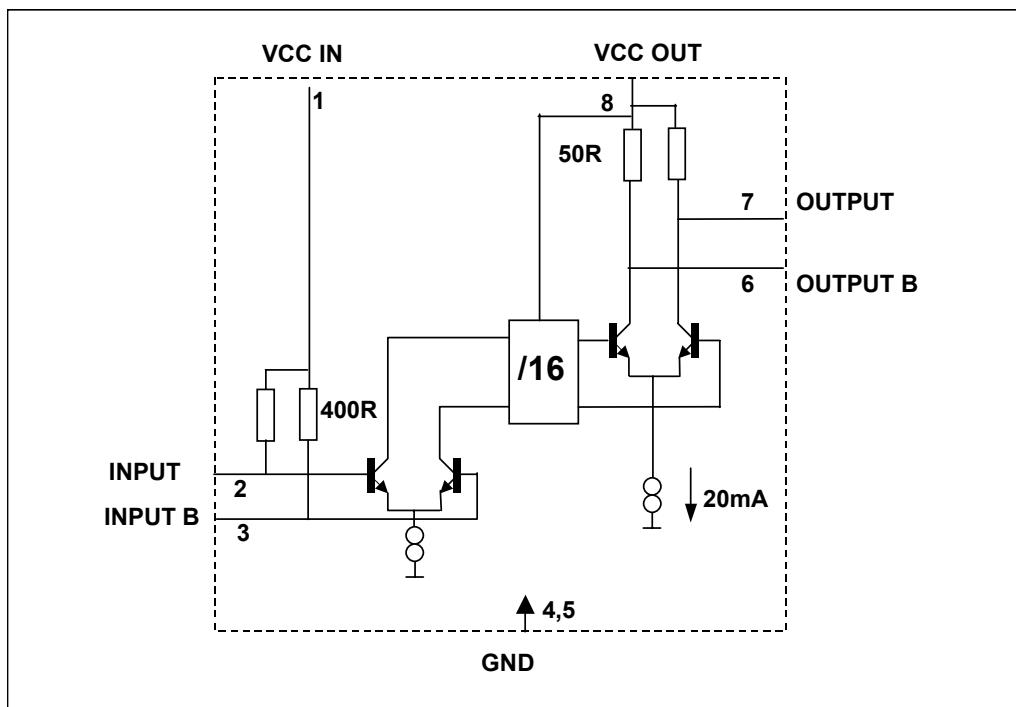
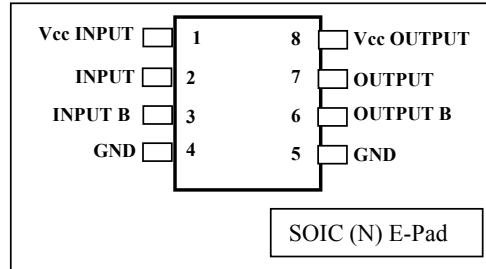


Figure 1 - Block Diagram

Pin Connection - Top View



Application Configuration

Figure 2 shows a recommended application configuration. This example shows the devices set up for single ended operation.

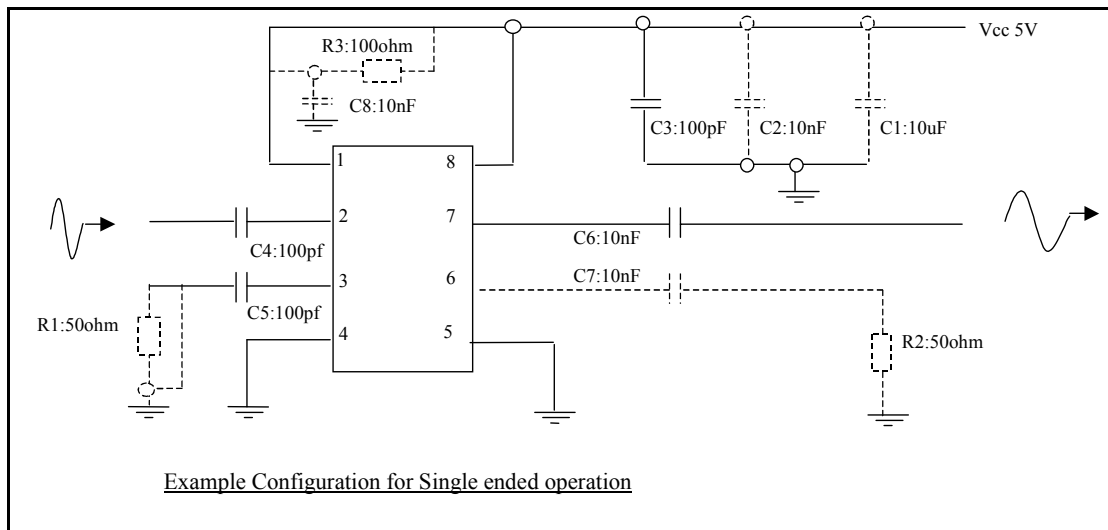


Figure 2 - Recommended Circuit Configuration

The above circuit diagram shows some components in dotted lines. These are optional in many applications.

1. C1 (10 μ F) and C2 (10 nF) power supply decoupling capacitors may be available on the board already.
2. R3 (100 Ohm) and C8 (10 nF) can be included if further power supply decoupling is required for the first stage biasing circuit. This may optimise the noise and jitter performance. The values are suggestions and may have to be modified if the existing supplies are particularly noisy.
3. R1 (50 Ohm), in series with C5 (100 pF), may reduce feedthrough of the input signal to the output.
4. R2 (50 Ohm) and C7 (10 nF) will help to balance the current drawn from the power supply and may reduce voltage transients on the power supply line

Evaluation Boards From Zarlink Semiconductor

Zarlink Semiconductor provide a prescaler evaluation board. These are primarily for those interested in performing their own assessment of the operation of the prescalers. The boards are supplied unpopulated and may be assembled for single ended or differential input and output operation. Once assembled, all that is required is an Rf source and a DC supply for operation. The inputs and outputs are connected via side launch SMA connectors.

Absolute Maximum Ratings

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	Vcc		6.5V	
2	Prescaler Input Voltage			2.5	Vp-p
3	ESD protection (Static Discharge)			2	kV
4	Storage temperature	T _{ST}	-65	150	°C
5	Maximum Junction Temp			125	°C
6	Thermal Characteristics	Thja		58.6	°C/W multi-layer PCB

AC/DC Electrical Characteristics

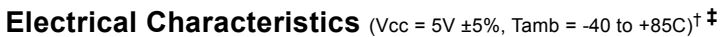
Electrical Characteristics (T_{amb} = 25°C, Vcc = 5V)^{† ‡}

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Supply current	1		0.35		mA	Input stage bias current
Supply current	8		100	130	mA	Divider and output stages
Input frequency	2,3	2		11	GHz	RMS sinewave (See Note 1)
Input sensitivity	2,3		-8		dBm	f _{in} = 1GHz to 2GHz
Input sensitivity	2,3		-15	-10	dBm	f _{in} = 2GHz to 9.5GHz
Input sensitivity	2,3		-10	0	dBm	f _{in} = 11GHz
Input overload	2,3		8		dBm	f _{in} = 1GHz to 4GHz
Input overload	2,3		11		dBm	f _{in} = 5GHz to 11GHz
Input Edge Speed	2,3	900			V/is	For <2GHz operation.
Output voltage	6,7		1		Vp-p	Differential Into 50ohm pullup resistors
Output power	6,7	-3	-1	1.2	dBm	Single-ended output, f _{in} = 2GHz to 10GHz, pwr ip= -10dBm
Phase Noise (10kHz offset)	6,7		-152		dBc/Hz	F _{in} = 5GHz, pwr ip = 0dBm
O/P Duty Cycle	6,7	45	50	55	%	

Note 1: The device characterisation test method incremented the amplitude over the entire range of frequency and ensures that there are no "holes" in the characteristic.

[†] Input sensitivity and output power values assume 50 Ohm source and load impedances.

[‡] Characteristics are guaranteed by either production test or design.



Note 1: Pin 1 is the Vcc pin for the 1st stage bias current. In some applications e.g. if the power supply is noisy, it may be advantageous to add further supply decoupling to this pin (i.e. an additional R, C filter, see diagram of the recommended circuit configuration, Figure 2).

† These characteristics are guaranteed by design and characterisation over the range of operating conditions unless otherwise stated.

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Input and Output Characteristics†

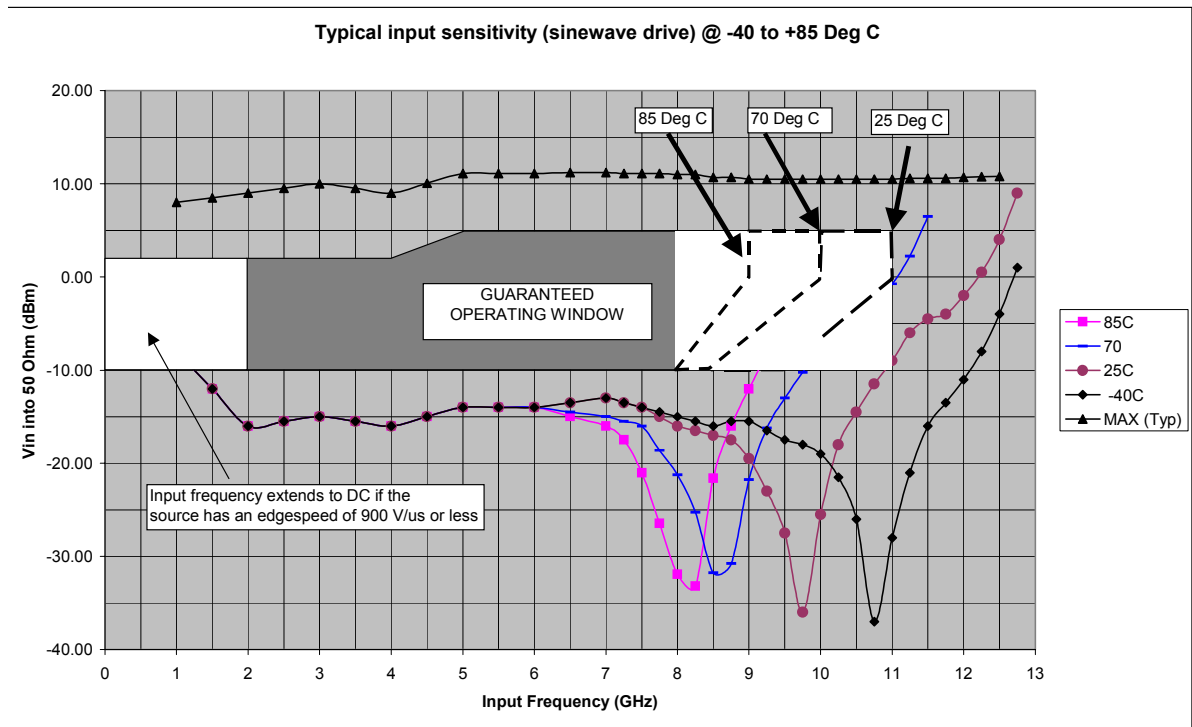
Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Input sensitivity	2,3		-15	-10	dBm	Tamb = 85C, Fin = 2 to 8 GHz
Input overload	2,3	2	5		dBm	fin = 2 GHz
Input overload	2,3	2	8		dBm	fin = 4 GHz
Input overload	2,3	5	13		dBm	fin = 9 GHz
Input overload	2,3	5	11		dBm	fin = 10 GHz
Input Edge Speed	2,3	900			V/is	For <2GHz Operation, see Note 1
Output voltage	6,7		1		Vp-p	Differential Into 50ohm pullup resistors
Output power	6,7	-4	-1	2	dBm	Single-ended output, fin = 2GHz to 10GHz, pwr ip= -10dBm
O/P Duty Cycle	6,7	45	50	55	%	
Trise and Tfall	6,7		110		ps	

Note 1: for an input signal frequency of less than 2GHz, the slew rate of the sinewave signal becomes progressively too slow for the divider.

† Input sensitivity and output power values assume 50 Ohm source and load impedances

For details of the test set-up, refer to the Application Note for RF Prescalers.

The following graph summarises the Input and Output Characteristics table



Single Ended Output Power

The following graphs show how the output power varies with supply.

Differential output power will be 3dB.

Figure 3 - Pout, Freq, Temp @ Vcc = 4.75V

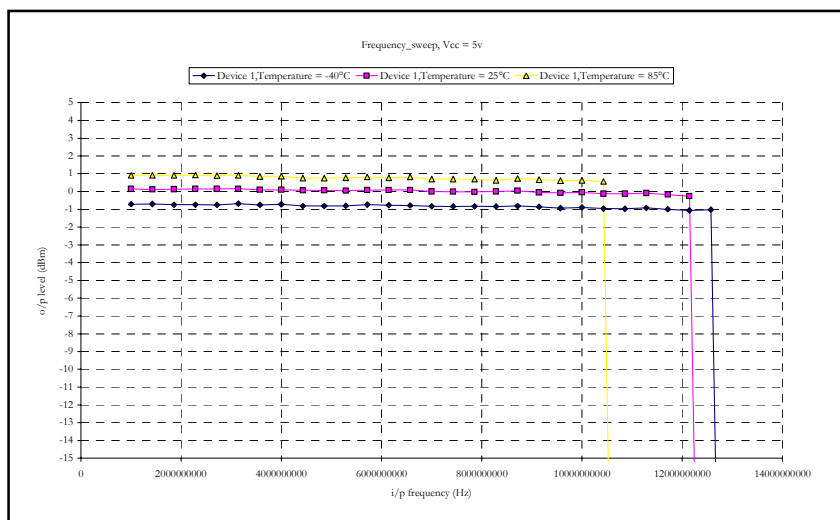


Figure 4 - Pout, Freq, Temp @ Vcc = 5V

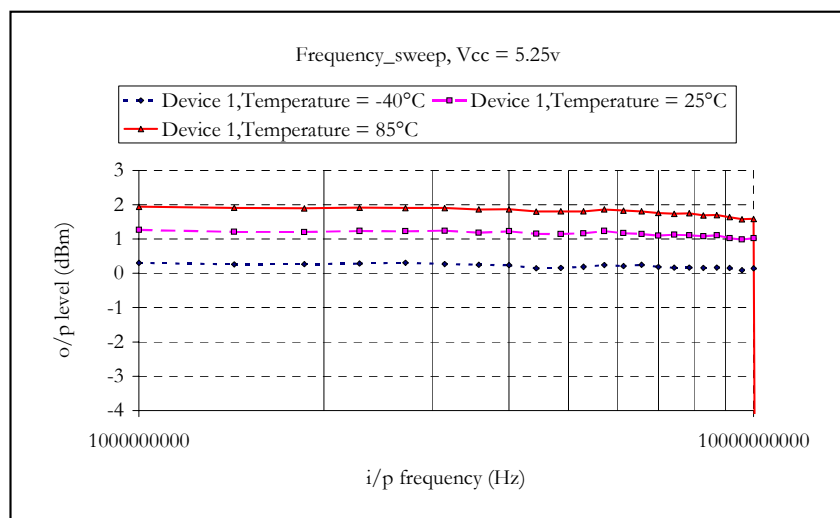


Figure 5 - Pout, Freq, Temp @ Vcc = 5.25V

Oscillographs of the Divider Output Waveforms

The following oscillographs show that the low-level feedthrough of the input waveform can be further reduced by summing the two output pins of the device differentially, refer to Figure 6 and Figure 7.

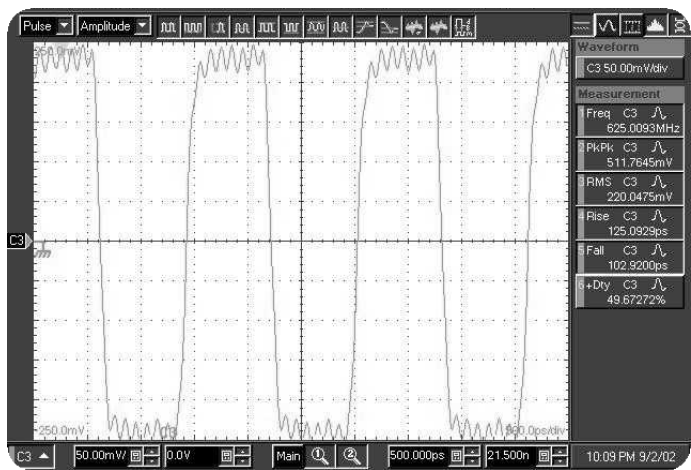


Figure 6 - Output waveform-single-ended
VCC=5V, Vin=2dBm, Fin=10GHz

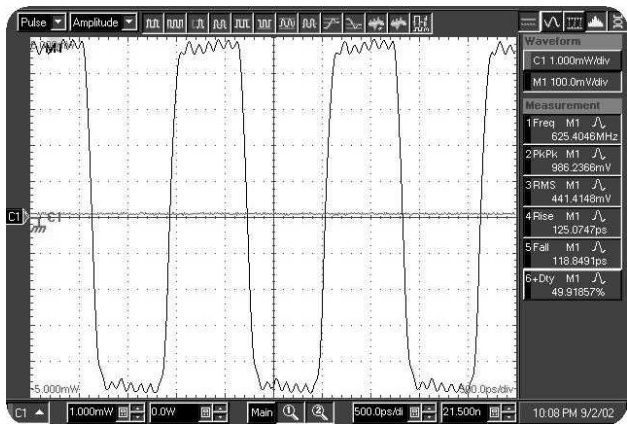
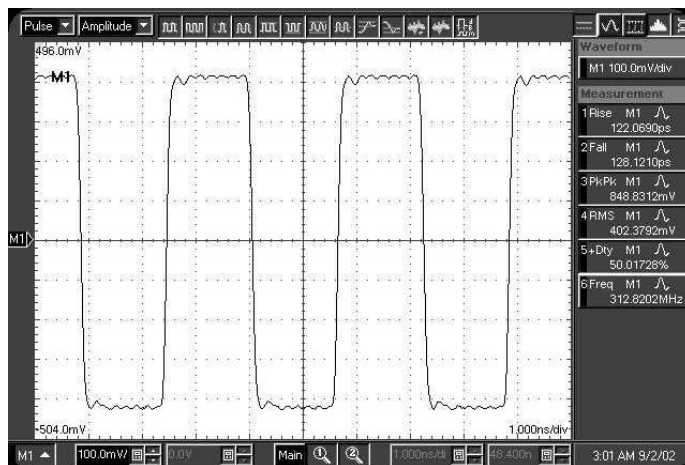
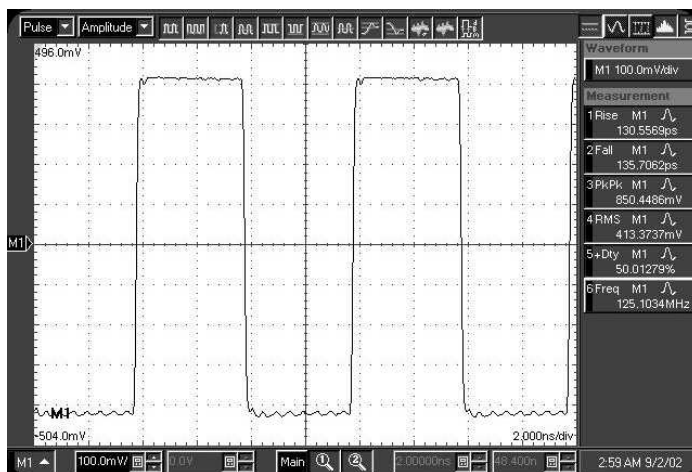


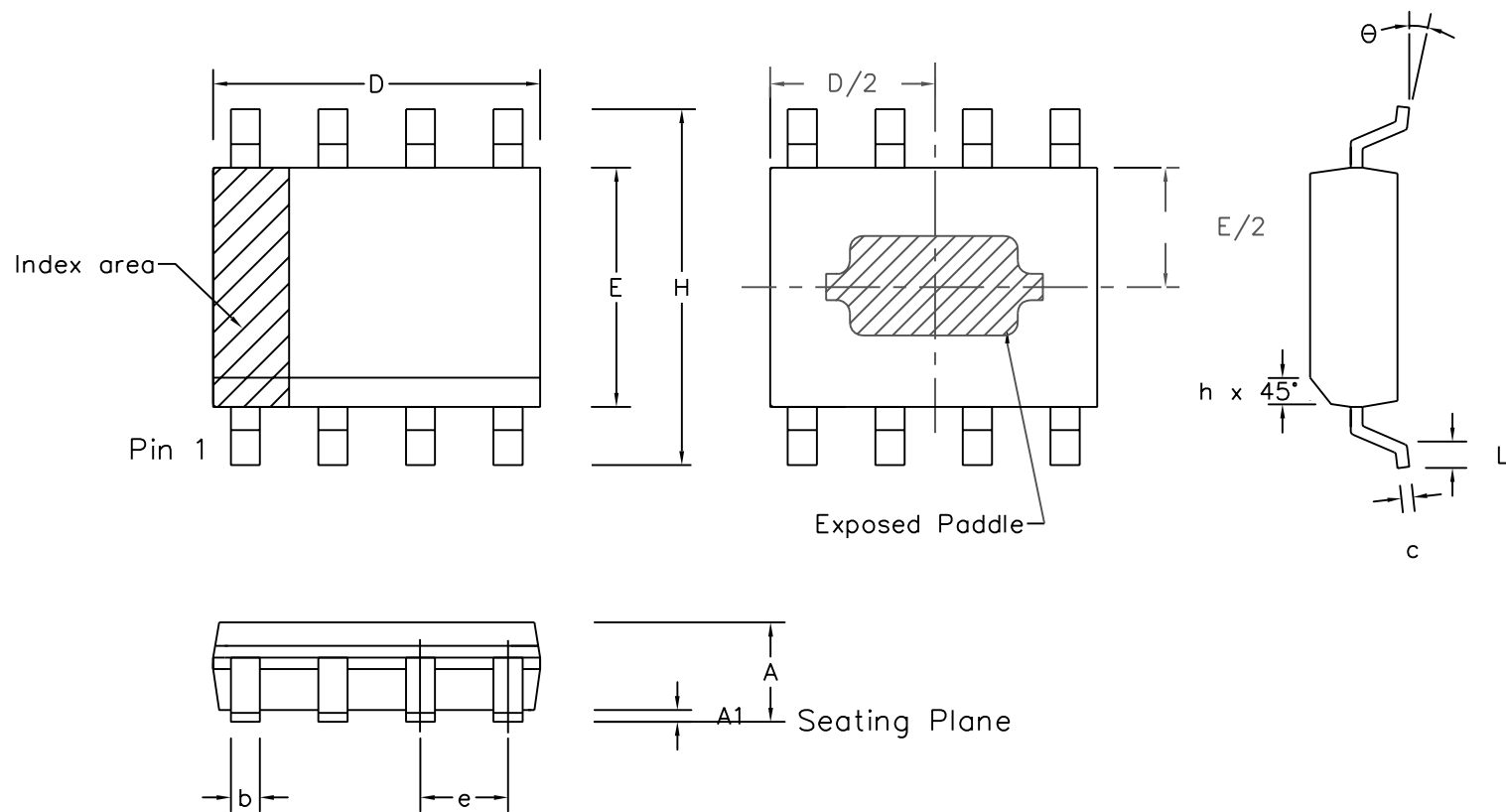
Figure 7 - Output waveform - differential
VCC=5V, Vin=2dBm, Fin=10GHz



**Figure 8 - Output waveform - differential
VCC=4.75V, Vin=-10dBm, Fin=5GHz**




**Figure 9 - Output waveform - differential
VCC=4.75V, Vin=-dBm, Fin=2GHz**



	Min Inches	Max inches	Min mm	Max mm
A	0.056	0.066	1.43	1.68
A1	0.000	0.004	0.00	0.10
D	0.189	0.196	4.80	4.98
H	0.230	0.244	5.84	6.20
E	0.150	0.157	3.81	3.99
L	0.16	0.35	0.41	0.89
e	0.050 BSC		1.27 BSC	
b	0.0138	0.0192	0.35	0.49
c	0.0075	0.0098	0.19	0.25
O	0°	8°	0°	8°
h	0.010	0.016	0.25	0.41
Pin Features			Pin Features	
N	8		8	

- Notes:
- Controlling dimensions are in inches.
 - Dimensions D & E do not include mould flash, protusion or gate burrs. These shall not exceed 0.006” per side.
 - Exposed paddle not to scale on drawing
 - Extrusion of the exposed pad in bottom side is 0.20 MM Typical

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ISSUE	1						Previous package codes	Package Outline for 8 lead e-pad SOIC (0.150" Body width)
ACN	212933						MH / S	
DATE	14Jun02							GPD00790
APPRD.								



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