


SGS-THOMSON
 MICROELECTRONICS

STP3N90
STP3N90FI

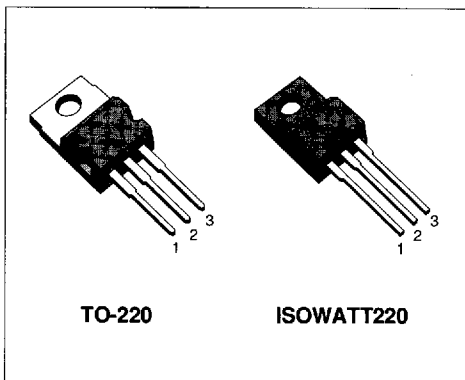
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

TYPE	V _{DS}	R _{DS(on)}	I _D
STP3N90	900 V	< 4.5 Ω	3.2 A
STP3N90FI	900 V	< 4.5 Ω	1.9 A

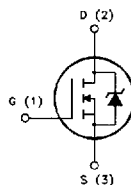
- TYPICAL R_{DS(on)} = 3.9 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW INPUT CAPACITANCE
- LOW GATE CHARGE
- APPLICATION ORIENTED CHARACTERIZATION

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- CONSUMER AND INDUSTRIAL LIGHTING
- DC-AC INVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLY (UPS)



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP3N90	STP3N90FI	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	900		V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	900		V
V _{GS}	Gate-source Voltage	± 20		V
I _D	Drain Current (continuous) at T _c = 25 °C	3.2	1.9	A
I _D	Drain Current (continuous) at T _c = 100 °C	2	1.2	A
I _{DM} (*)	Drain Current (pulsed)	13	13	A
P _{tot}	Total Dissipation at T _c = 25 °C	100	40	W
	Derating Factor	0.8	0.32	W/°C
V _{ISO}	Insulation Withstand Voltage (DC)	—	2000	V
T _{stg}	Storage Temperature	-65 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(*) Pulse width limited by safe operating area

THERMAL DATA

		TO-220	ISOWATT220	
$R_{thj-case}$	Thermal Resistance Junction-case Max	1.25	3.12	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	62.5		°C/W
$R_{thc-sink}$	Thermal Resistance Case-sink Typ	0.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	3.2	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	160	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	4.2	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive ($T_c = 100^\circ\text{C}$, pulse width limited by T_j max, $\delta < 1\%$)	2	A

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^\circ\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ $V_{GS} = 0$	900			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_c = 125^\circ\text{C}$			250 1000	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 1.7\text{ A}$ $V_{GS} = 10\text{ V}$ $I_D = 1.7\text{ A}$ $T_c = 100^\circ\text{C}$		3.9	4.5 9	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	3.2			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 1.7\text{ A}$	1	3.5		S
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		650	850	pF
C_{oss}	Output Capacitance			82	105	pF
C_{rss}	Reverse Transfer Capacitance			28	40	pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 30\text{ V}$ $I_D = 2.1\text{ A}$			50	ns
t_r	Rise Time	$R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 3)			110	ns
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 640\text{ V}$ $I_D = 3\text{ A}$ $R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 5)		170		A/ μ s
Q_g	Total Gate Charge	$V_{DD} = 400\text{ V}$ $I_D = 3\text{ A}$ $V_{GS} = 10\text{ V}$		42	55	nC
Q_{gs}	Gate-Source Charge			6		nC
Q_{gd}	Gate-Drain Charge			17		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(volt)}$	Off-voltage Rise Time	$V_{DD} = 640\text{ V}$ $I_D = 3\text{ A}$		95	120	ns
t_f	Fall Time	$R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$		20	25	ns
t_c	Cross-over Time	(see test circuit, figure 5)		120	165	ns

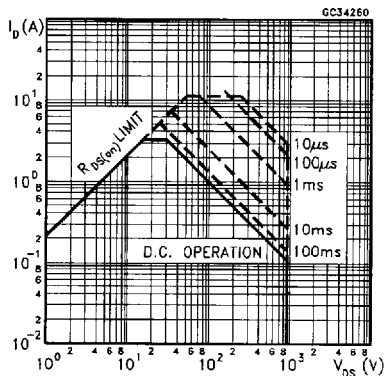
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				3.2	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				13	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 3.2\text{ A}$ $V_{GS} = 0$			2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 3\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 80\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, figure 5)		700		ns
Q_{rr}	Reverse Recovery Charge			8.8		μC
I_{RRM}	Reverse Recovery Current			25		A

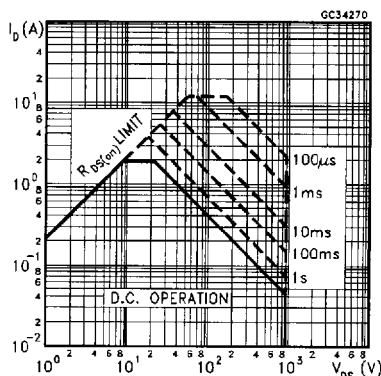
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(\bullet) Pulse width limited by safe operating area

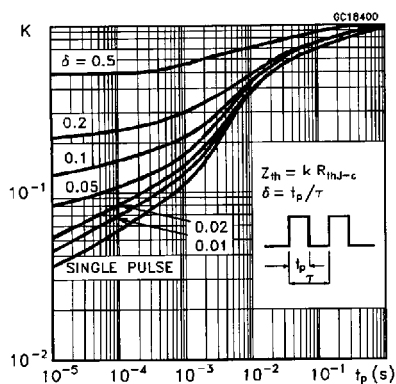
Safe Operating Areas For TO220



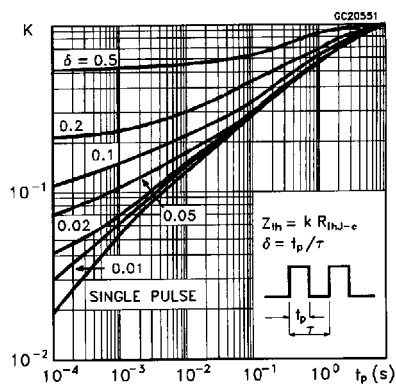
Safe Operating Areas For ISOWATT220



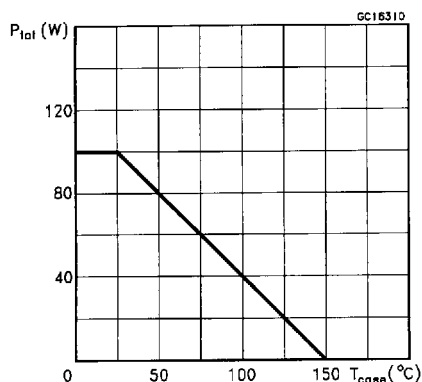
Thermal Impedance For TO-220



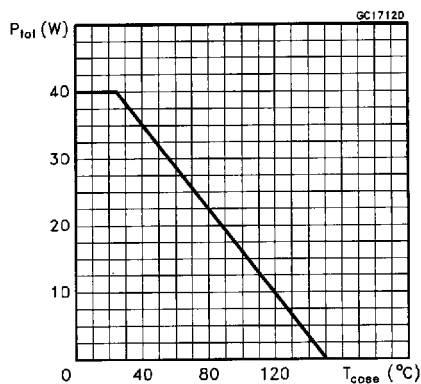
Thermal Impedance For ISOWATT220



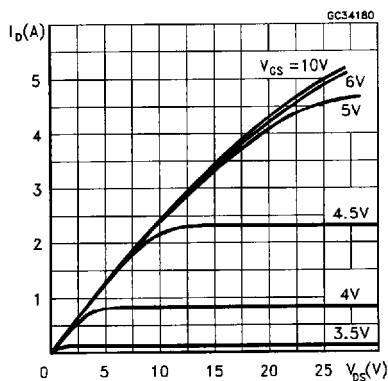
Derating Curve For TO-220



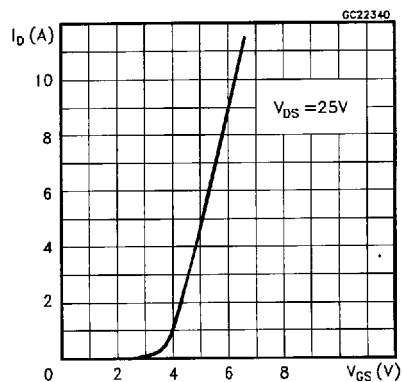
Derating Curve For ISOWATT220



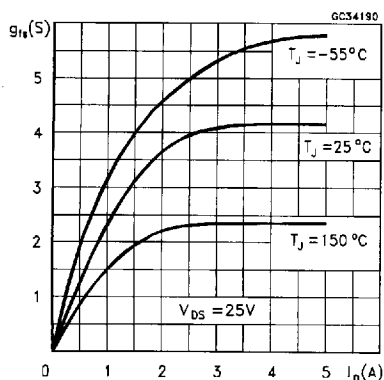
Output Characteristics



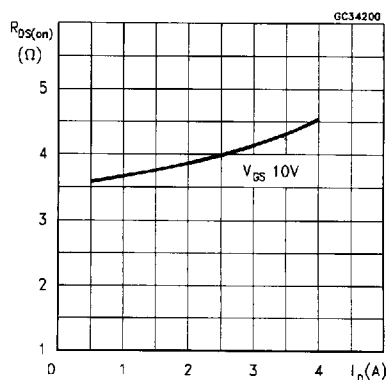
Transfer Characteristics



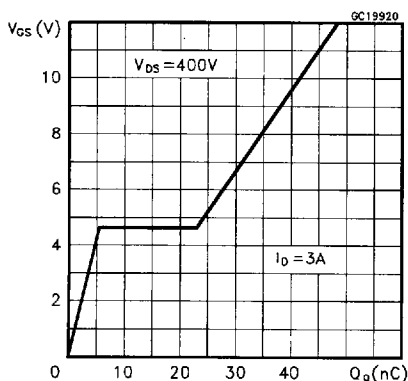
Transconductance



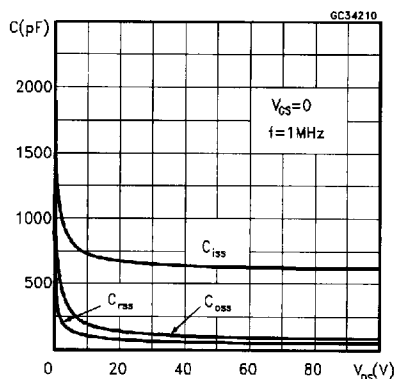
Static Drain-source On Resistance



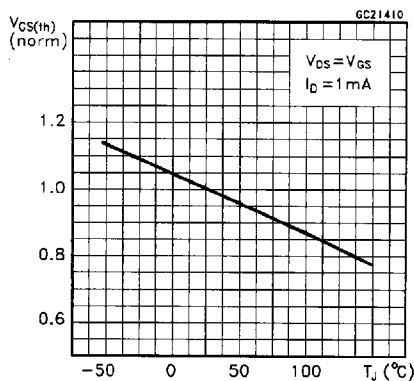
Gate Charge vs Gate-source Voltage



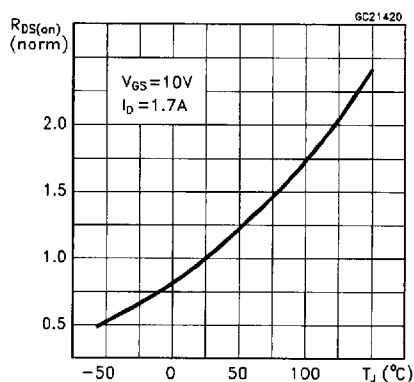
Capacitance Variations



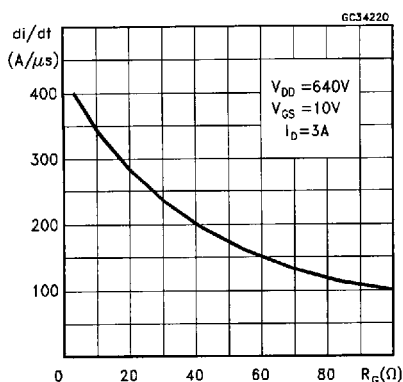
Normalized Gate Threshold Voltage vs Temperature



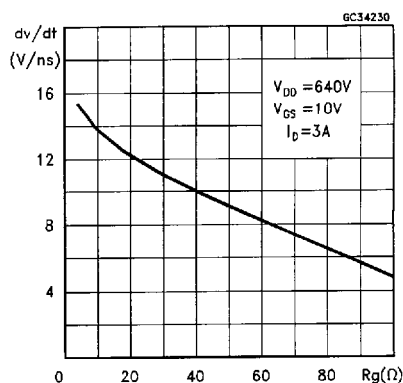
Normalized On Resistance vs Temperature



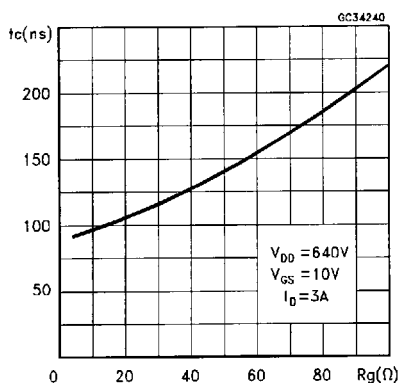
Turn-on Current Slope



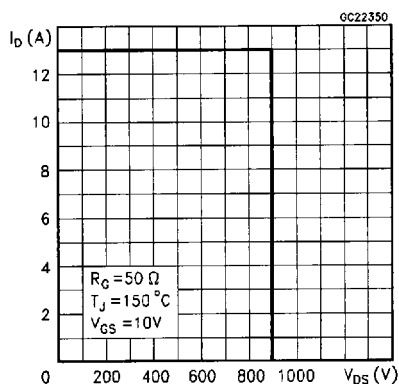
Turn-off Drain-source Voltage Slope



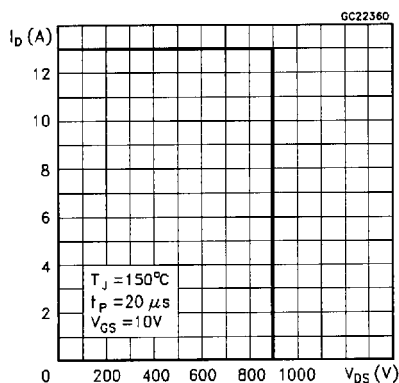
Cross-over Time



Switching Safe Operating Area



Accidental Overload Area



Source-drain Diode Forward Characteristics

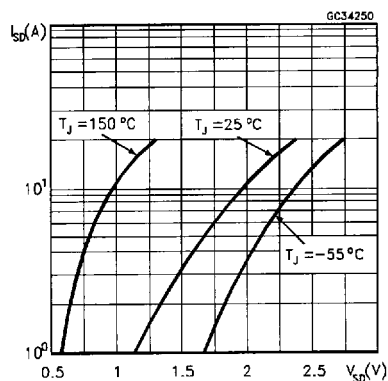
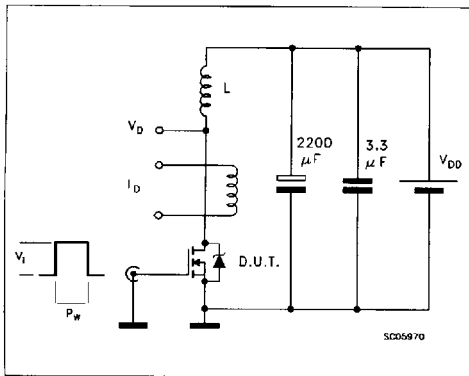
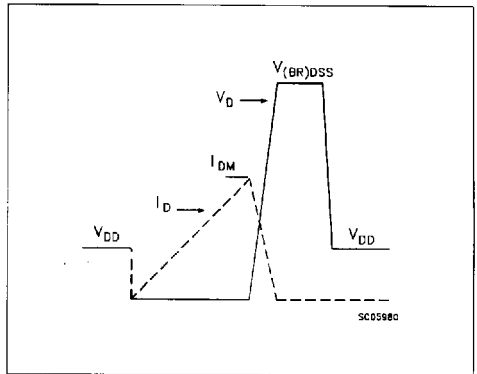
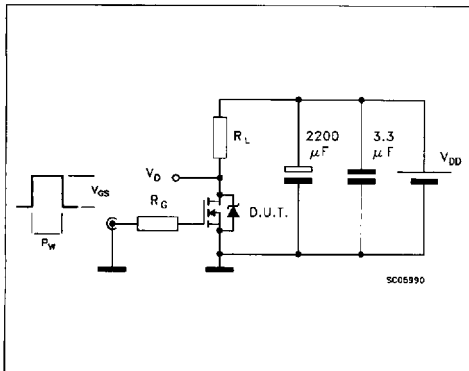
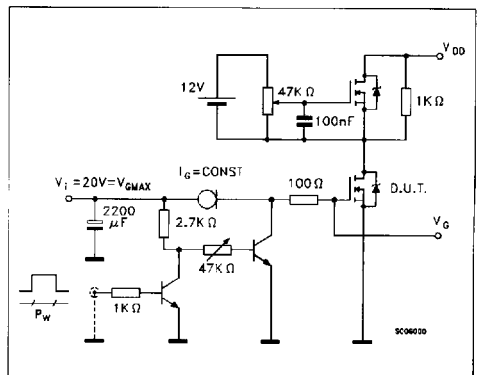


Fig. 1: Unclamped Inductive Load Test Circuits**Fig. 2: Unclamped Inductive Waveforms****Fig. 3: Switching Times Test Circuits For Resistive Load****Fig. 4: Gate Charge Test Circuit****Fig. 5: Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time**