NPN video transistor BFQ161

FEATURES

- Low output capacitance
- High gain bandwidth
- High current applicability
- Good thermal stability
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Pre-stage driver in high resolution colour graphics monitors.

DESCRIPTION

NPN video transistor in a SOT54 (TO-92) plastic package.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter

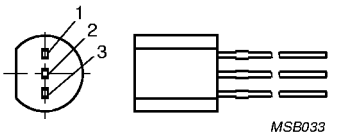


Fig.1 Simplified outline (SOT54; TO-92).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	20	V
V_{CER}	collector-emitter voltage	R_{BE} = 100 Ω	–	19	V
I_C	collector current (DC)		–	500	mA
P_{tot}	total power dissipation	$T_s \leq 75$ °C; note 1	–	1	W
h_{FE}	DC current gain	I_C = 300 mA; V_{CE} = 5 V	25	–	
f_T	transition frequency	I_C = 300 mA; V_{CE} = 5 V; T_{amb} = 25 °C	1	–	GHz
T_j	junction temperature		–	150	°C

Note

1. T_s is the temperature at the soldering point of the collector pin, 4 mm from the body.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	20	V
V_{CEO}	collector-emitter voltage	open base	–	10	V
V_{CER}	collector-emitter voltage	R_{BE} = 100 Ω	–	19	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	500	mA
P_{tot}	total power dissipation	$T_s \leq 75$ °C; notes 1 and 2; see Fig.3	–	1	W
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		–	150	°C

Notes

1. T_s is the temperature at the soldering point of the collector pin, 4 mm from the body.
2. Transistor mounted on a printed-circuit board with a metallized pad area of 10 mm^2.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 1	75	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient		175	K/W
$R_{th\ s\text{-}a}$	thermal resistance from soldering point to ambient		100	K/W

Note

1. T_s is the temperature at the soldering point of the collector pin, 4 mm from the body.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 5 mA; I_E = 0	20	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 10 mA; I_B = 0	10	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_E = 0.1 mA; I_C = 0	3	–	–	V
I_{CES}	collector-emitter cut-off current	I_B = 0; V_{CE} = 10 V	–	–	100	μA
h_{FE}	DC current gain	I_C = 300 mA; V_{CE} = 5 V; T_{amb} = 25 °C; see Fig.4	25	–	–	
		I_C = 100 mA; V_{CE} = 5 V; T_{amb} = 25 °C; see Fig.4	40	50	–	
C_{cb}	collector-base capacitance	I_C = 0; V_{CB} = 5 V; f = 1 MHz; see Fig.5	–	4.3	–	pF
C_c	collector capacitance	$I_E = i_e$ = 0; V_{CB} = 5 V; f = 1 MHz	–	6	–	pF
f_T	transition frequency	I_C = 300 mA; V_{CE} = 5 V; see Fig.6	1	–	–	GHz

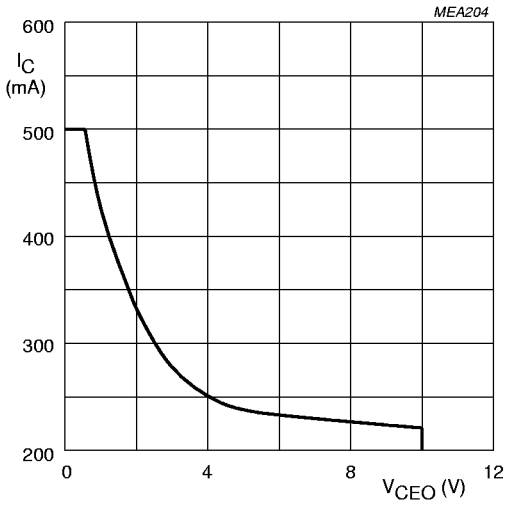


Fig.2 DC SOAR.

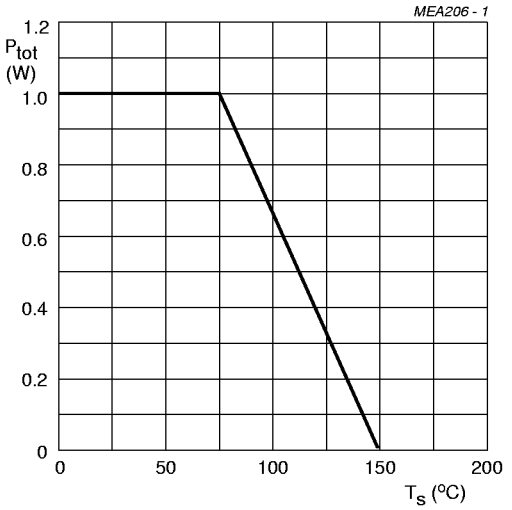
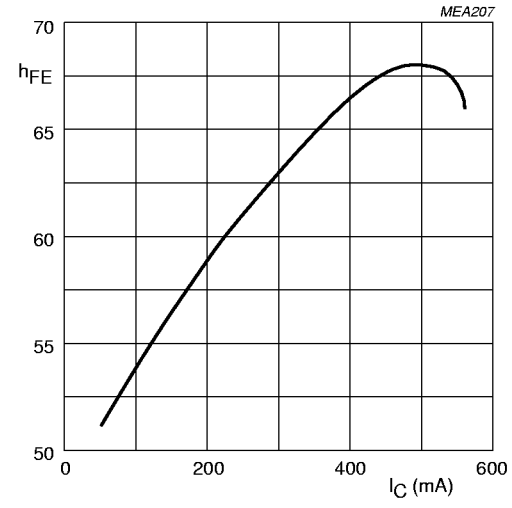
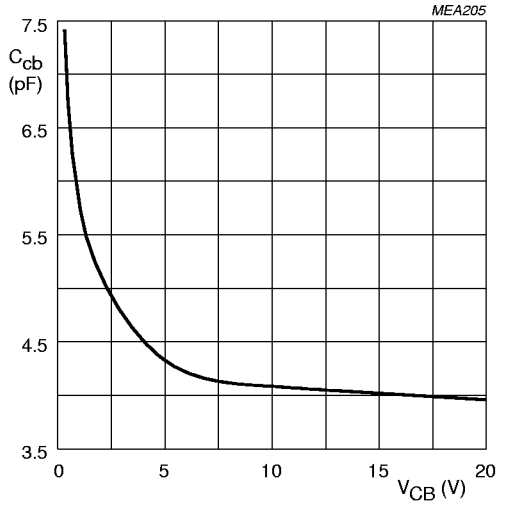


Fig.3 Power derating curve.



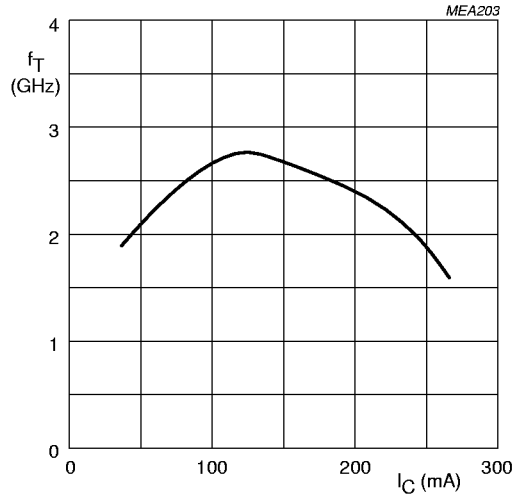
V_{CE} = 5 V; T_{amb} = 25 °C.

Fig.4 DC current gain as a function of collector current; typical values.



f = 1 MHz; T_{amb} = 25 °C.

Fig.5 Collector-base capacitance as a function of collector-base voltage; typical values.

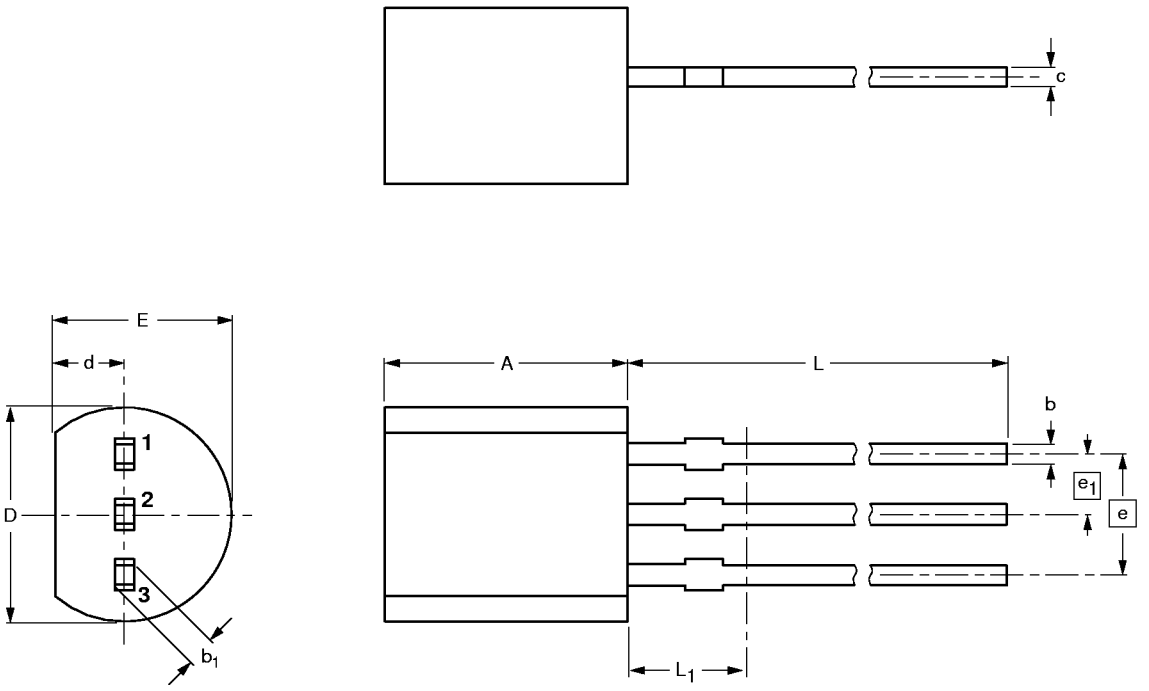


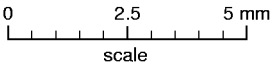
V_{CE} = 5 V; T_{amb} = 25 °C.

Fig.6 Transition frequency as a function of collector current; typical values.

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**





DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1(1)
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28