BFS21
BFS21A

T-27-25

MATCHED N-CHANNEL FETS

Matched pair of symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes, mounted together in a metal S-clip.

These devices are intended for low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at T_{amb} = 25 °C; I_D = 0,5 mA; V_{DG} = 15 V

			BFS21	BFS21A	
Gate cut-off current	I_G	<	0,5	0,5	nA
Gate -source voltage difference	$\lvert\Delta V_{GS}\rvert$	<	20	10	mV
Thermal drift of gate-source voltage difference	$\left\lvert\frac{d\Delta V_{GS}}{dT}\right\rvert$	<	75	40	μV/K
Difference in transfer impedance	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	15	7,5	Ω
Difference in penetration factor	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	1	0,5	mV/V
Common mode rejection ratio	CMRR	>	60	66	dB

MECHANICAL DATA

SOT-52 (see next page)

BFS21
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TOTAL DEVICE

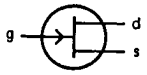
Dimensions in mm

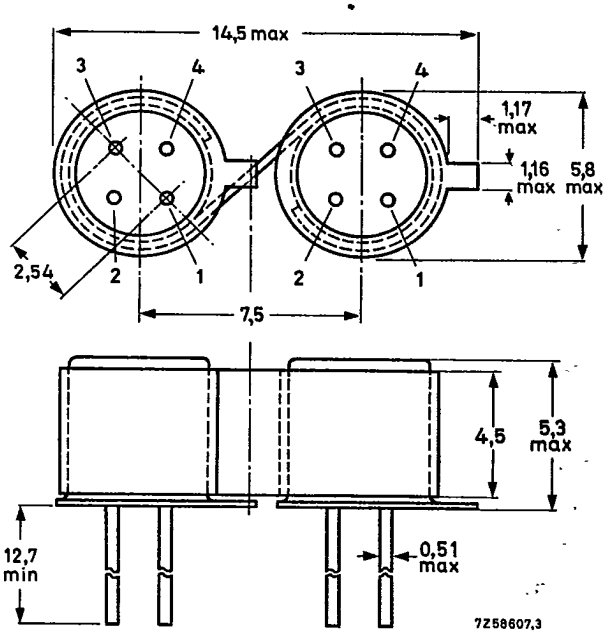
MECHANICAL DATA

SOT52

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case





Maximum lead diameter is guaranteed only for 12,7 mm.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage between any 2 terminals	V	max.	30 V
Drain current	I_D	max.	4 mA
Gate current	I_G	max.	0,5 mA
Total power dissipation up to T_{amb} = 100 °C	P_{tot}	max.	30 mW
Operating ambient temperature	T_{amb}		−20 to + 100 °C

CHARACTERISTICS (total device)

T_{amb} = 25 °C unless otherwise specified

			BFS21	BFS21A	
Drain current ratio V_{DG} = 15 V; V_{GS} = 0; T_j = 25 °C	$\frac{I_{D1-S1S}}{I_{D2-S2S}}$	>	0.95	0.95	
		<	1.05	1.05	
Gate-source voltage difference					
I_D = 500 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}\rvert$	<	20	10	mV
I_D = 100 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}\rvert$	<	20	10	mV
Thermal drift of gate-source voltage difference					
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert\frac{d\,\Delta V_{GS}}{dT}\right\rvert$	<	75	40	μV/K
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert\frac{d\,\Delta V_{GS}}{dT}\right\rvert$	<	75	40	μV/K
Change of gate-source voltage difference with ambient temperature					
T_{amb} = 25 to 100 °C					
I_D = 500 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1})\rvert$	<	6	3	mV
I_D = 100 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1})\rvert$	<	6	3	mV
Difference of penetration factors*					
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	1	0.5	10^{-3}
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	1	0.5	10^{-3}
Difference of transfer impedances**					
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	15	7.8	Ω
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	75	37.5	Ω

* The difference between the penetration factors is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$$\left(\Delta\frac{g_{os}}{g_{fs}} = \frac{d\,\Delta V_{GS}}{d\,V_{DG}} \text{ at } I_D = \text{constant}\right)$$

** The difference between the transfer impedances is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$$\left(\Delta\frac{1}{g_{fs}} = \frac{d\,\Delta V_{GS}}{d\,I_D} \text{ at } V_{DG} = \text{constant}\right)$$

CHARACTERISTICS (continued) (total device)

		BFS21	BFS21A	
Common mode rejection ratio*				
I_D = 500 μA; V_{DG} = 15 V	CMRR	> 60	66	dB
I_D = 100 μA; V_{DG} = 15 V	CMRR	> 60	66	dB

INDIVIDUAL TRANSISTOR

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25°	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}	−65 to +	175	°C
Junction temperature	T_j	max.	175	°C

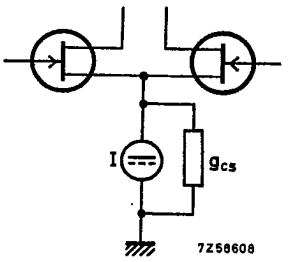
THERMAL RESISTANCE

From junction to ambient in free air (for individual transistor without S-clip)	$R_{th\ j\text{-}a}$	=	590	K/W

* Common mode rejection ratio

$$(C\ M\ R\ R)^{-1} = \Delta \frac{g_{os}}{g_{fs}} + \tfrac{1}{2}\, g_{cs}\, \Delta \frac{1}{g_{fs}}$$

where g_{cs} in this formula is the output conductance of the summing current source.



The guaranteed values of CMRR apply at g_{cs} = 0.1 μΩ^{-1}

Matched N-channel FETs

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CHARACTERISTICS (individual transistor)

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current			
I_D = 500 μA; V_{DS} = 15 V	I_G	<	0.5 nA
I_D = 500 μA; V_{DS} = 15 V; T_{amb} = 100 °C	I_G	<	25 nA
Drain current			
V_{DS} = 15 V; V_{GS} = 0; T_j = 25 °C	I_{DSS}	>	1 mA
Gate-source cut-off voltage			
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	6 V
Transfer conductance at f = 1 kHz			
I_D = 500 μA; V_{DS} = 15 V	g_{fs}	>	1.0 mS
Output conductance at f = 1 kHz			
I_D = 500 μA; V_{DS} = 15 V	g_{os}	<	15 μS
Input capacitance at f = 1 MHz			
I_D = 500 μA; V_{DS} = 15 V	C_{is}	<	5 pF
Feedback capacitance at f = 1 MHz			
I_D = 500 μA; V_{DS} = 15 V	C_{rs}	<	0.75 pF
Equivalent noise voltage			
f = 10 Hz			
I_D = 500 μA; V_{DS} = 15 V	$V_n/\sqrt{B}$	<	200 nV/√Hz
V_{DS} = 15 V; V_{GS} = 0	$V_n/\sqrt{B}$	<	75 nV/√Hz