PLESSEY Semiconductors

T-51-19

ZN1036E/D

PROGRAMMABLE COUNTER TIMER INTEGRATED CIRCUIT

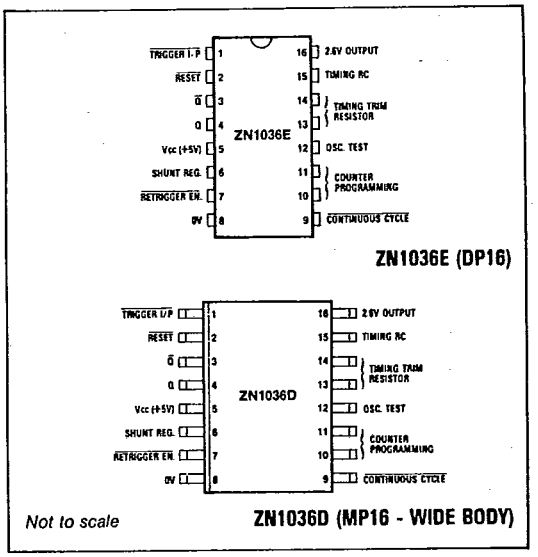
The ZN1036 combines linear and digital functions on the same chip such that simple precision timers can be constructed using the minimum of low cost external components. The frequency of an on-chip oscillator is determined by an external capacitor and resistor. Fine adjustment can then be achieved by the variation of an external trimming resistor. A buffered oscillator output can be used to monitor the trimming operation without affecting the oscillator frequency.

Pulses from the oscillator are fed into a programmable counter and the output changes state after a preset number of pulses. The counter is programmable in 4 stages - 4095, 2047, 1023 and 511 counts.

In this way precise time periods can be defined by timing capacitors and resistors of much smaller value than would be required by single RC time constant timers.

The count can be initiated either (a) with trigger input LO and supply going HI (supply initiation), or (b) with supply HI and trigger input going LO (trigger initiation). The timer can also be retriggered at any point (thus initiating a new timing period) or reset, terminating the time period.

The IC can operate from normal +5V logic supplies or from any higher voltage using a dropping resistor and internal shunt regulator connected to the supply pin.



Pin connections (top view)

FEATURES

- External Control of Operational Mode
- Accurate and Repeatable Performance
- Complementary High Current Output Drivers
- Buffered Oscillator Output for Easy Oscillator Calibration
- Time Period Trimming
- Supply or Trigger Input Timing Initiation
- Continuous Cycle Facility
- On-Chip Regulator or TTL Supply Option
- Minimum of External Components Required
- Available in Plastic DIL (DP) — ZN1036E and Miniature Plastic DIL (MP) — ZN1036D

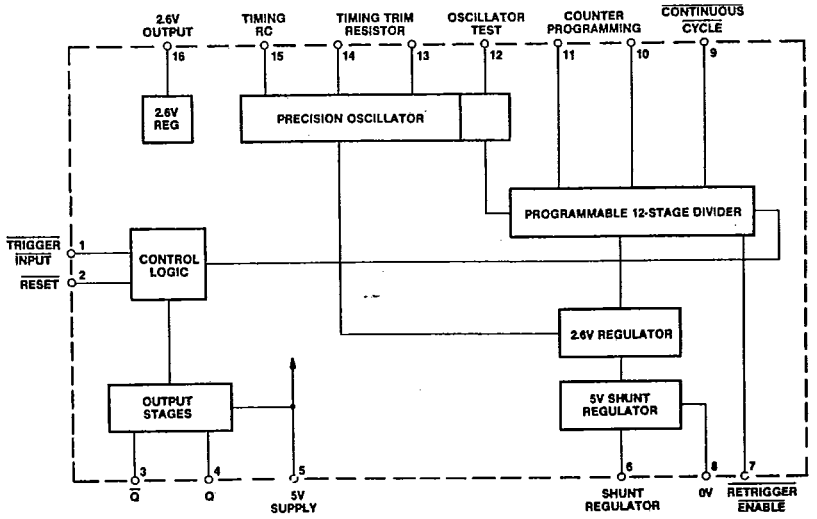


Fig.1

ABSOLUTE MAXIMUM RATINGS

Dissipation	250mW derate above 30°C at 5mW/°C
Output source current	25mA
Output sink current	25mA
Operating temperature range	0 to +70°C
Storage temperature range	−55 to +125°C

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Timing section						See Note 5
Timing resistor	R_T	2k7		5M6	Ω	
Timing capacitor	C_T	0.1			nF	See Fig 2
Trim resistor	R_{trim}	0		560	kΩ	
Repetitive timing error			0.01		%	
Timing initiation and reset						
(a) Supply voltage initiation						
Voltage to initiate timing	V_{CC}	4.7			V	supply applied to pin 5 with Pin 1 connected to Pin 8
Rate of change of V_{CC}				0.25	V/μs	
(b) Trigger input initiation						
Voltage to initiate timing	$V_{T(LO)}$			1	V	
Voltage to prevent initiation of timing	$V_{T(HI)}$	2.2			V	
Minimum pulse to trigger			2		μs	
(c) Supply voltage reset						
Voltage to reset	V_{CC}		3.6		V	See note 2
External clock input						
Frequency				250	kHz	Clock input to pin 14 via a 10k resistor
Drive current	I_{clk}		0.1		mA	
Pulse width	t_{clk}	2			μs	
Pulse amplitude	V_{clk}	2.5		5.5	V	

Parameter	Symbol	Conditions	
Time multiplying factor	M	Pin 10	Pin 11
4095		H	H
2047		H	L
1023		L	H
511		L	L

ELECTRICAL CHARACTERISTICS (Cont.) T-51-19

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply						Note 4
(a) Externally regulated						connected to Pin 5
Supply voltage Supply current	V_{CC} I_{CC}	4.5	3.8	5.5 4.5	V mA	V_{CC} = 5V outputs unloaded
(b) Internally regulated (5V shunt regulator)						connect pin 5 to Pin 6. Note 4
Operating current range	I_R	5		55	mA	see Note 3
Regulated voltage	V_R	4.5		5.5	V	I_R = 10mA
Slope resistance			1.25		Ω	I_R = 7 – 55mA
Regulated voltage change with temperature			35		mV	I_R = 7 – 55mA t = 0 to +70°C
(c) Reference voltage (2.5V series regulator)						
Regulated voltage	V_{REF}	2.4	2.5	2.6	V	V_{CC} = 5V, Pin 16 unloaded
Load current	I_{REF}		1		mA	V_{CC} = 5V
Slope resistance			2.5		Ω	
Output drive Q to $\overline{Q}$						V_{CC} = 5V
Output voltage	$V_{O(HI)}$ $V_{O(LO)}$	2.5 0.3	3.0 0.4	3.2 0.6	V V	$I_{O(HI)}$ = 25mA $I_{O(LO)}$ = – 25mA
Output current	$I_{O(HI)}$ $I_{O(LO)}$			– 25 + 25	mA mA	Source Sink
Rise time	t_r		300		ns	I_O = 5mA, V_{CC} = 5V
Fall time	t_f		100		ns	I_O = 5mA, V_{CC} = 5V
Propagation delay V_T Low to V_O High	t_p		2.3	2.5	μs	
Oscillator test output swing		3	4	5	V	10k Pull up to 5V
Temperature coefficient	T_C		0.008		%/°C	R_{TRIM} = 56k

Note 1 Time = MCR

C = capacitance in μF
R = resistance in MΩ
M = multiplying factor

For $t_{osc} \geqslant 10\mu s$

At $t_{osc} < 10\mu s$ this relationship no longer holds as the reset time becomes a significant fraction of t_{osc}

Ncte 2 In order to reset the timer the supply voltage should be reduced to 2V although reset may be typically acheived at 3.6V. Reset will not occur with the supply greater than 4V

Note 3 Since the +5V regulator cannot be used on its own without the rest of the circuit, the minimum operating current includes the 4.5mA maximum supply current taken by the timer.

Note 4 A 0.1μF capacitor should be connected between V_{CC} (Pin 5) and G_{ND} (Pin8) at all times.

Note 5 Minimum recommended oscillator period = 4μs

SECTION 1 THE TIMING FUNCTION

1.1 Fixed time period

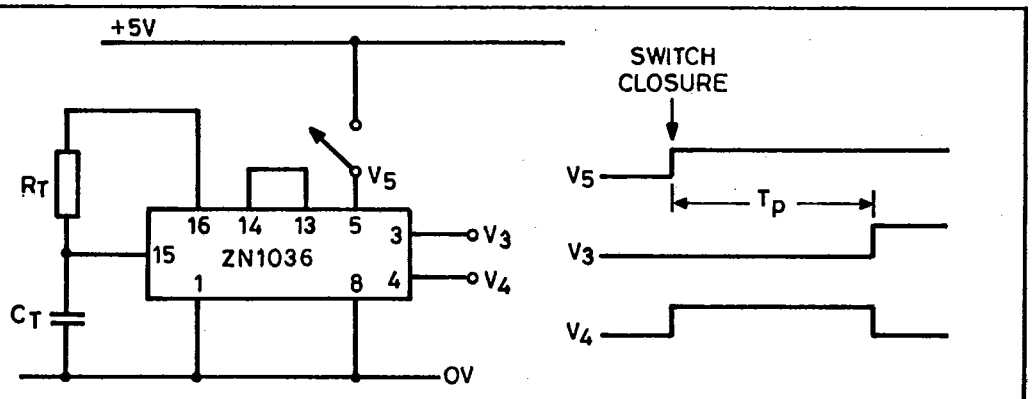


Fig. 2

External components R_T and C_T determine the length of period T_p. The timing components set the period of an internal oscillator to C_T R_T ±10% and an internal divider causes a change in the output state after a preset number of oscillator cycles (determined by counter programming Pins).

When the time period is initiated Pin 4 goes Hi for a time period T_p. On completion of the time period, Pin 4 goes Lo and Pin 3 which was previously Lo goes Hi and remains Hi until the timing sequence is re-initiated.

1.2 Trimming the time period

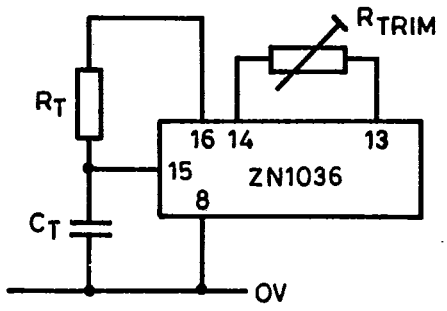


Fig. 3

1.3 Design of variable period timers

Time periods from 2.044ms to infinity may theoretically be obtained using the ZN1036 integrated timer circuit. The following section should enable the designer to get the best possible circuit configuration achievable within the design limits. The necessary information is presented below, Fig 4, in the form of a timing components against oscillator period graph. The graph has been plotted using a 56kΩ trim resistor between Pins 13 and 14.

The maximum range of oscillator period possible for a particular value - or timing capacitor can easily be obtained from the graph. To obtain the time period the oscillator period (from Fig. 4) is multiplied by the multiplying factor M (determined by programming Pins 10 and 11)

The periods obtained with the timing components selected from Fig. 4 may be trimmed to the exact time required using a variable resistor up to the value of 560kΩ between Pins 13 and 14.

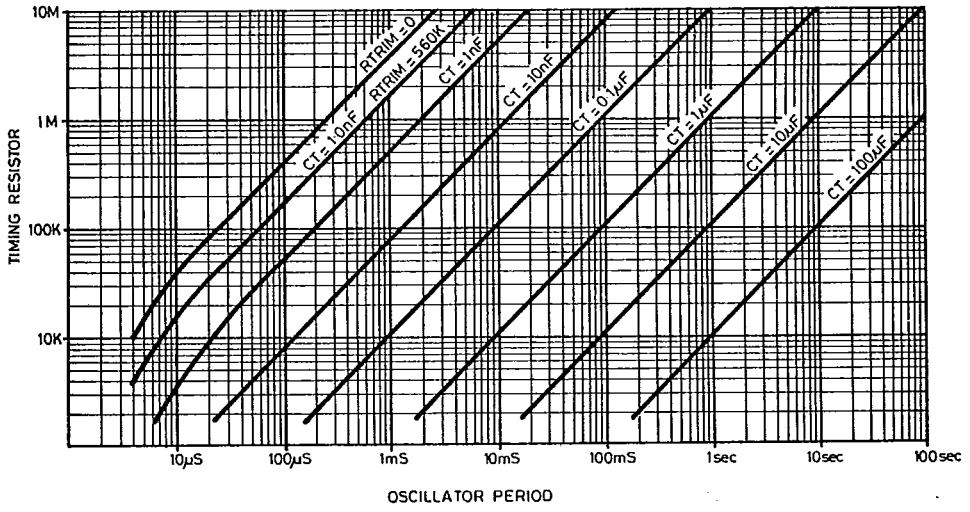


Fig. 4 Oscillator period

SECTION 2 INPUT AND OUTPUT CIRCUITS

Note 2.1 External clock

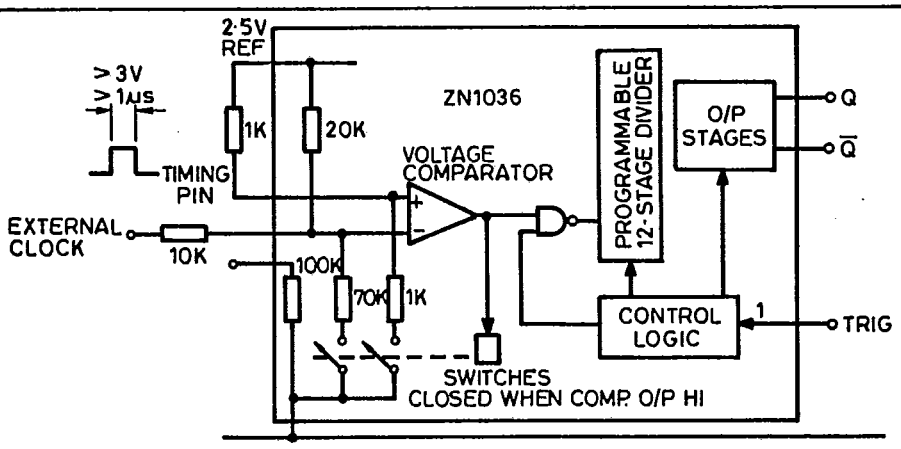


Fig. 5

The ZN1036 can be used with an external clock as shown in the circuit of Fig. 5.

The internal clock is disabled by connecting a 1k resistor from the timing pin 15 to the +2.5V reference pin 16 thus preventing the non-inverting i/p to the amplifier dropping below the inverting input voltage. The amplifier output is therefore HI and the internal switches are closed.

An external clock pulse, provided it meets the limits defined in the characteristics, will override the disabling on pin 15 and, if the trigger i/p on pin 1 is LO, will cause a pulse to be passed to the divider circuit.

The output Q and $\overline{Q}$ will change from LO to HI and vice versa at the end of a present number of external clock pulses.

Note 2.2 Timing initiation and reset

2.2.1 Supply initiated

When pin 1 is held 'LO' and the supply is switched on, the control logic and counters are automatically reset as the supply rises to its on voltage. This also initiates timing at the same instant by gating the oscillator output into the counter. After the set time the outputs change state and remain thus until the supply is switched off or another period is initiated.

If, during such a timing cycle the trigger input is taken HI, no matter how many times or for how long, the condition of the outputs and the length of the timing period will not be affected. If the supply drops below the reset level even for a few microseconds then the timing period will be terminated. It will be reset and restarted when the supply rises again above the reset level. Thus a supply drop-out has the effect of increasing the time period. The timer can also be reset at any time by taking Pin2 Lo.

2.2.2 Trigger initiated

Allowing pin 1 to rise with the supply prevents timer initiation by the supply.

Pulling the trigger input 'LO' now initiates a normal timing period. A further period may be initiated by dropping the trigger LO again. This period is not affected when the trigger input level is altered during timing - as long as the 'retrigger enable' (Pin 7) remains Hi. When the retrigger enable goes Lo during timing any further trigger pulse will cause the initiation of a further time period at that point. The period is terminated again by the supply falling below the reset level or a Lo pulse to reset Pin 2. Since the normal condition of the trigger is Hi the timing will not restart on restoration of supply. A supply drop-out during a trigger initiated timing period has the effect of shortening the set time.

2.2.3 A simple repetitive timer

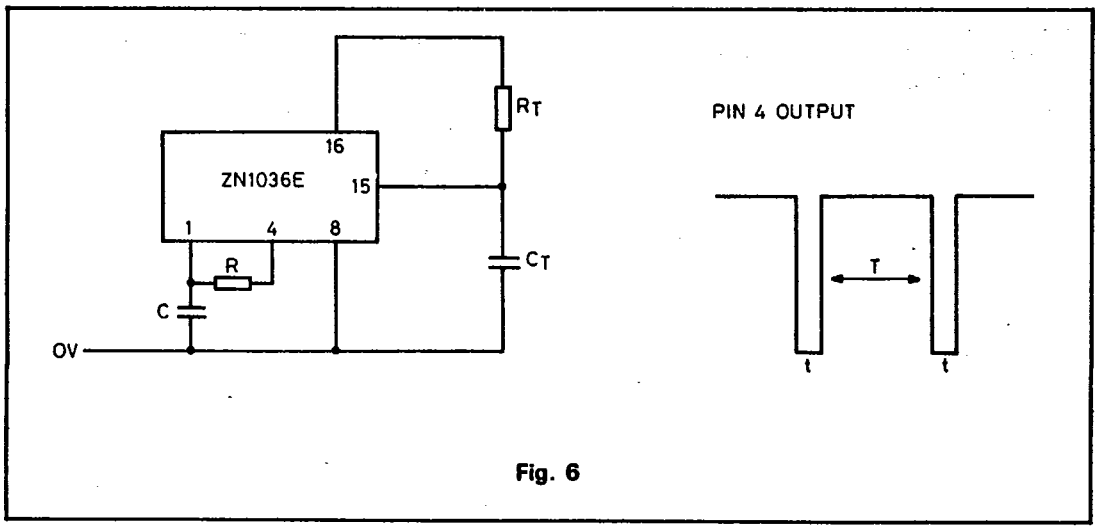


Fig. 6

A capacitor and resistor in the feedback loop can be used and the pulse length t determined by the values of C and R. T is determined by timing components R_T and C_T. R may be any value up to 10k whilst C is limited to 10μF.

2.2.4 A simple closed loop timer

The ZN1036 enables the designer to construct multistage timers with ease as one can be triggered by a single wire link from the output of another.

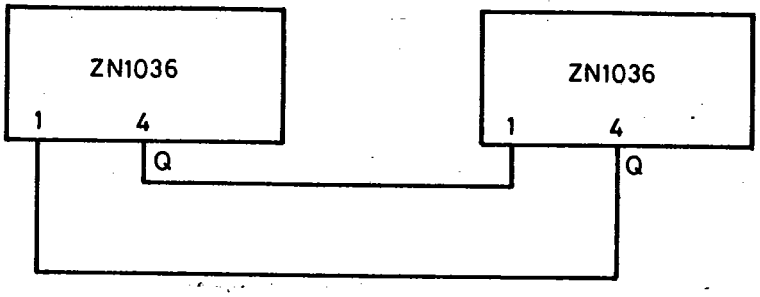


Fig.7

This may in theory be extended to any number of counters but for more than 3 there will be other modes of oscillation. For a ring of three, component tolerances will usually ensure that one mode is dominant with only one Q output Hi at a time. Higher numbers may not operate in the desired mode unless one set time is greater than the sum of all the others.

Fig. 8 shows a four stage ring timer.

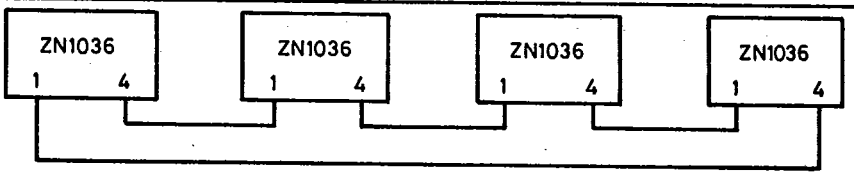


Fig. 8

2.2.5 ZN1036 Waveforms

The function of this device is demonstrated below as a Waveform diagram (Fig. 9)

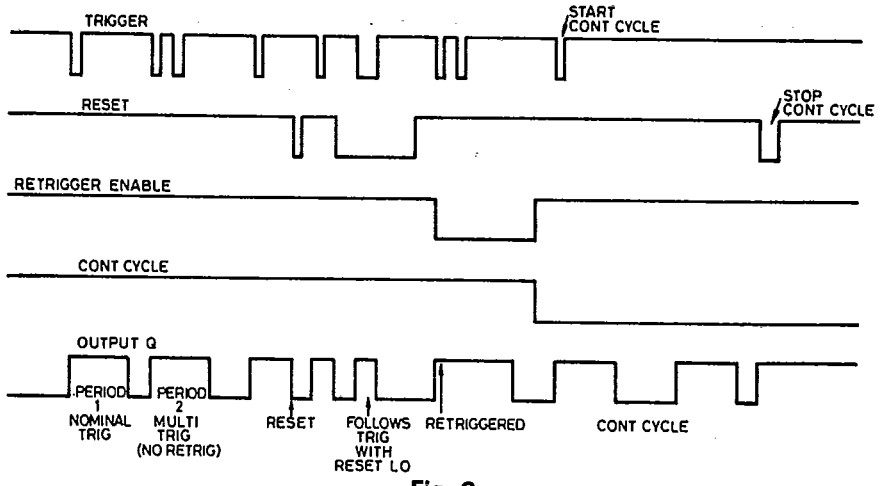


Fig. 9

2.3 Trigger input circuit

The input circuit comprises of a buffer input followed by a schmitt trigger circuit. The buffer pull up resistor can be as low as 30kΩ. So to pull the input down below the IV threshold a pull down resistor of less than 5.6kΩ is recommended for worst case design.

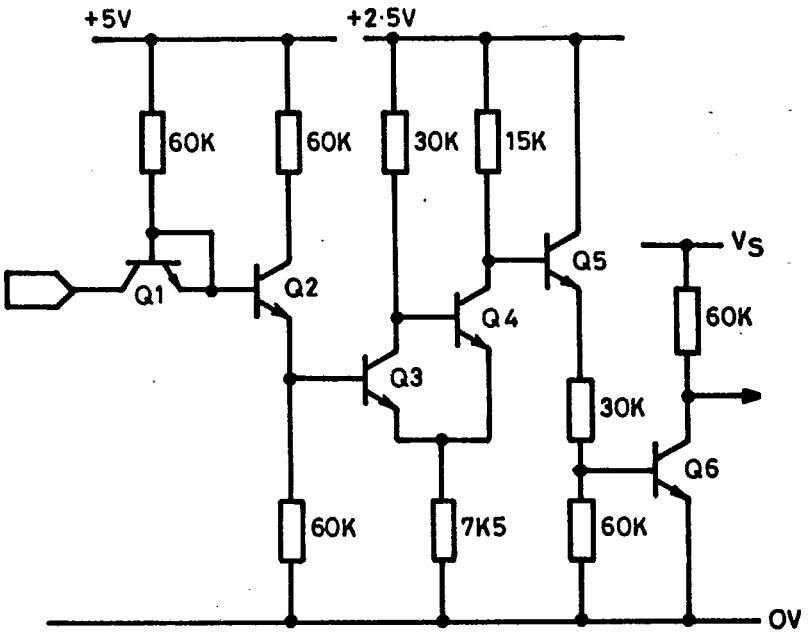


Fig. 10

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2.4 Output drive circuits

The Q and $\overline{Q}$ output drive circuits have the form illustrated in Fig. 11

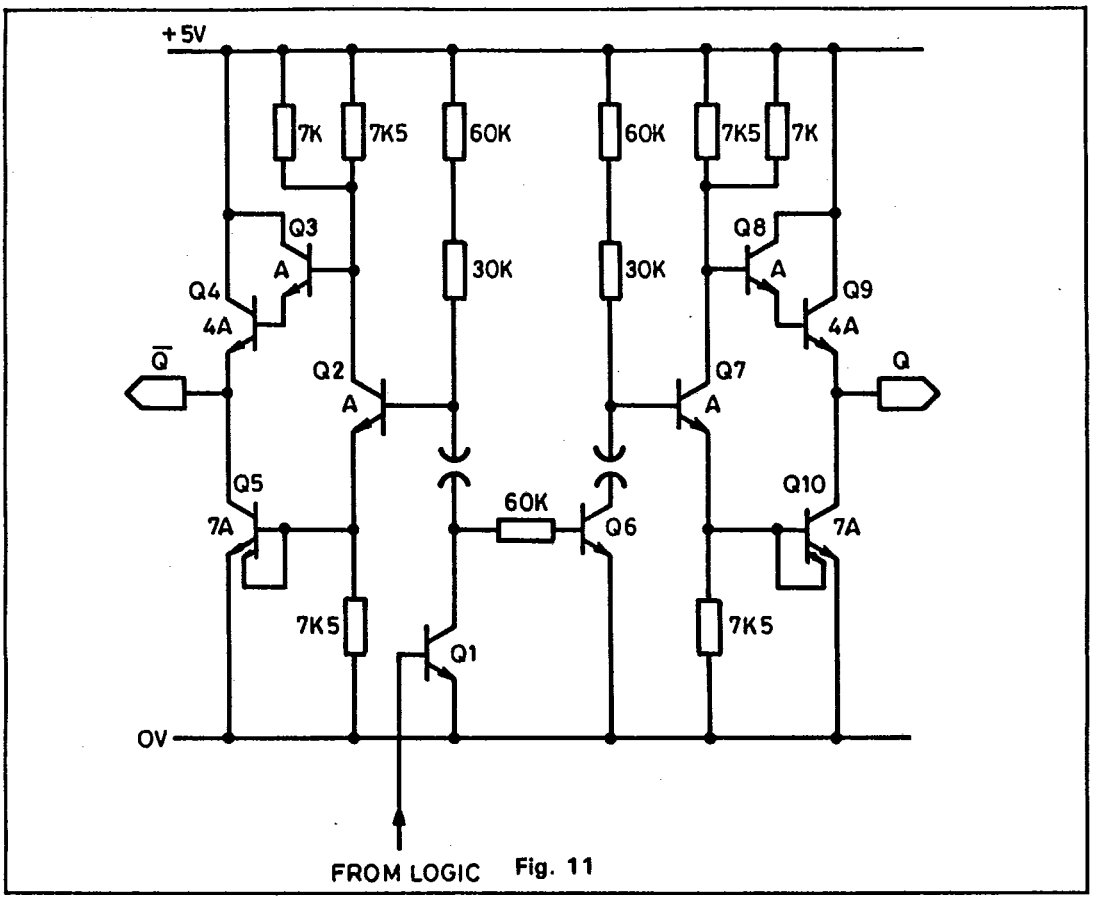

Fig. 11

2.5 Load circuits

2.5.1 Transistor driven relay

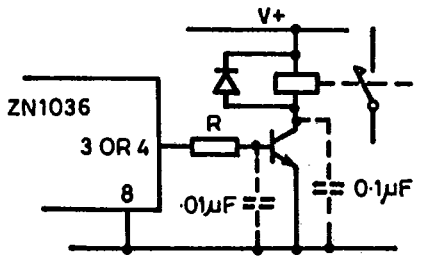

Fig. 12

The value of R is chosen to limit current to minimum required by the transistor under the worst condition.

If interference is experinenced suppression capacitors as shown may be needed.

2.5.2 Thyristor driven relay

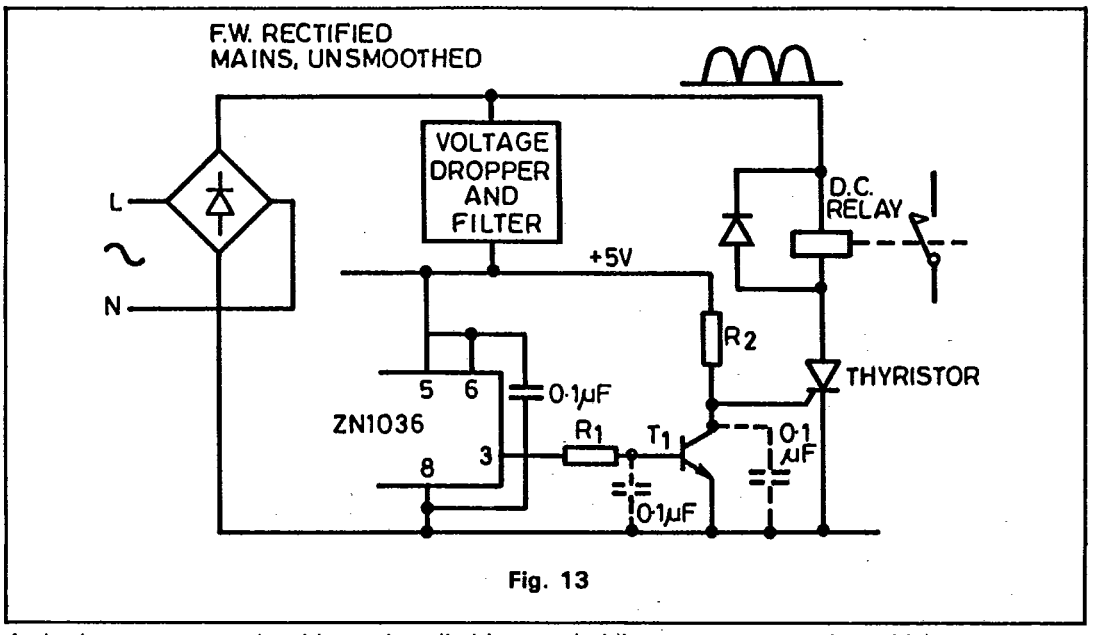

Fig. 13

A thyristor gate may be driven via a limiting resistor directly from pin 3 for DELAY-TO-ON timers. Fig. 13 illustrates a circuit for achieving DELAY-TO-OFF using a thyristor. R_2 can be as high as 10k for low gate current thyristors. The thyristor is chosen such that the reduction in gate-cathode impedance achieved with a saturated transistor is sufficient to increase the holding current to a value which ensures turn OFF and R_1 is chosen so that the transistor (T_1) just reaches saturation.

For 240 volts a.c. mains it may be necessary to use a 110 volt d.c. relay with a dropping resistor of equal resistance since 220 volts d.c. relays are not easily obtainable.

2.5.3 Triac a.c. load circuit positive firing

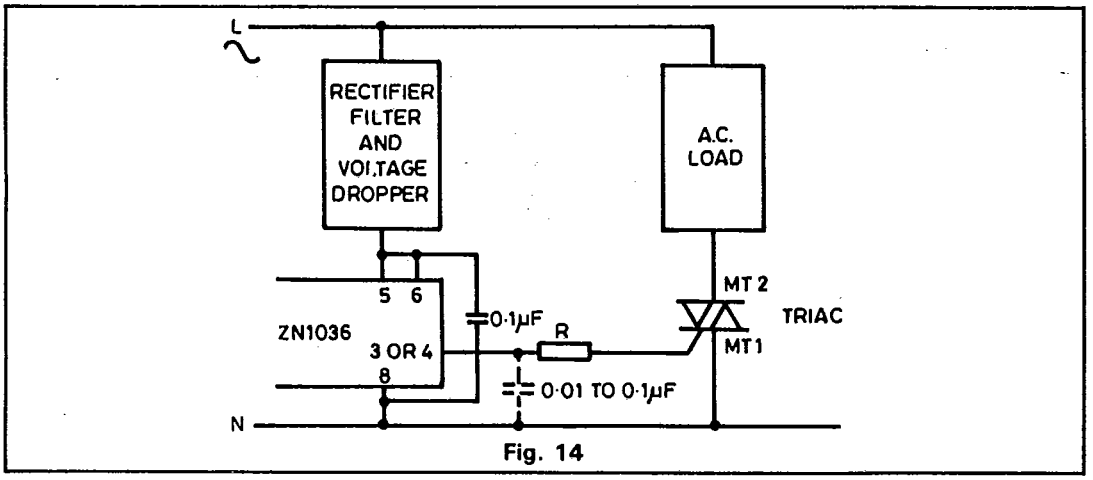

Fig. 14

The value of R is chosen to limit the current to the minimum required by the triac for positive firing in both quadrants.

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2.5.4 Triac a.c. load circuit negative firing

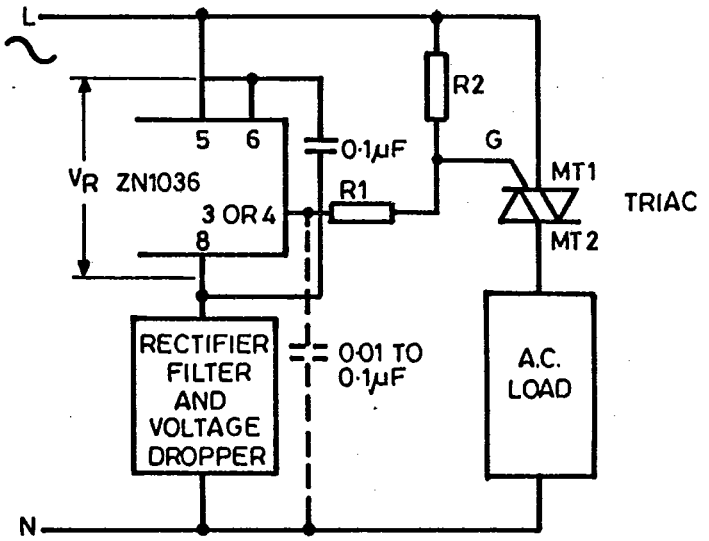


Fig. 15

The value of R_2 is chosen to prevent any leakage currents biasing the triac gate ON during OFF periods. R_1 is chosen to limit the gate current to the maximum required by the triac for negative firing in both quadrants.

Triacs in general are easier to fire in the negative gate mode than the positive and in this configuration the 1036 output drive voltage is a maximum since the total output swing would be $V_{R\,Min} - V_{O(LO)\,Max} \simeq 4.3$ volts for a current of 25mA. Negative firing triac circuits therefore enable triacs of greater power to be driven directly from the ZN1036 outputs than would be the case for positive firing circuits.

2.5.5 Output state indication

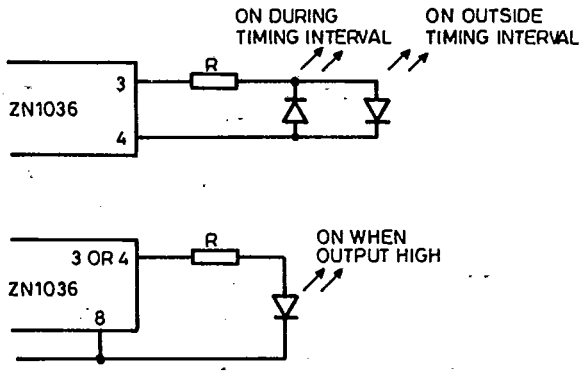


Fig. 16

The value of R is chosen to limit the current to the LED requirements. When mains supplies are used the extra power in the dropper resistor may make the use of neon indicators across the load preferable to LEDs.

SECTION 3 POWER SUPPLIES AND REFERENCES

3.1 Externally regulated supplies

If a 5V ±10% supply rail is available then the internal shunt regulator is not necessary and by leaving pin 6 unconnected the minimum current drain of 2mA required is avoided. The current available from the supply should not fall below a level of:

$$I_{CC} = (5mA + \text{the output current from pins 3 or 4})$$

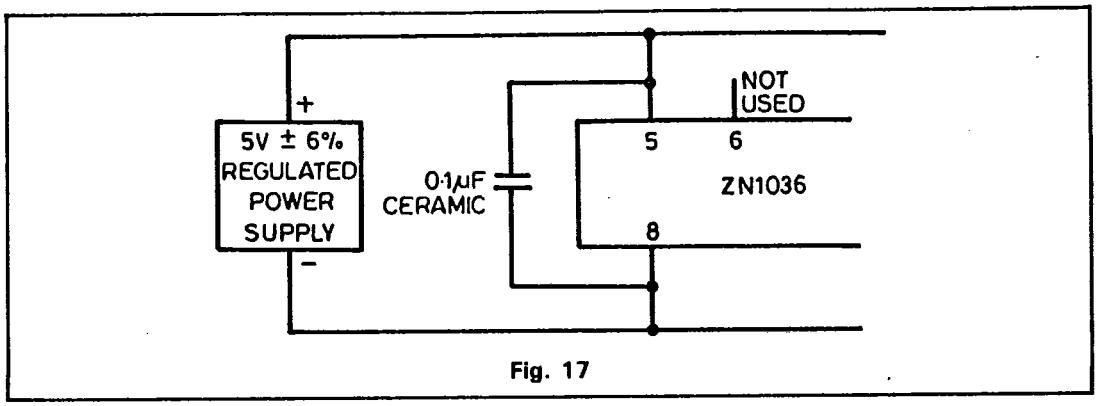


Fig. 17

N.B. The supply should be decoupled by 0.1μF capacitor connected as close as possible to pins 5 and 8.

3.2 Internally regulated supplies

3.2.1 d.c. supplies greater than 5 volts

By connecting pin 6 to pin 5 an on-chip shunt regulator allows the use of unregulated d.c. supplies higher than 5 volts. To illustrate the use of the shunt regulator a supply circuit design for operation with a typical process equipment supply of +24V and ±25% is shown below.

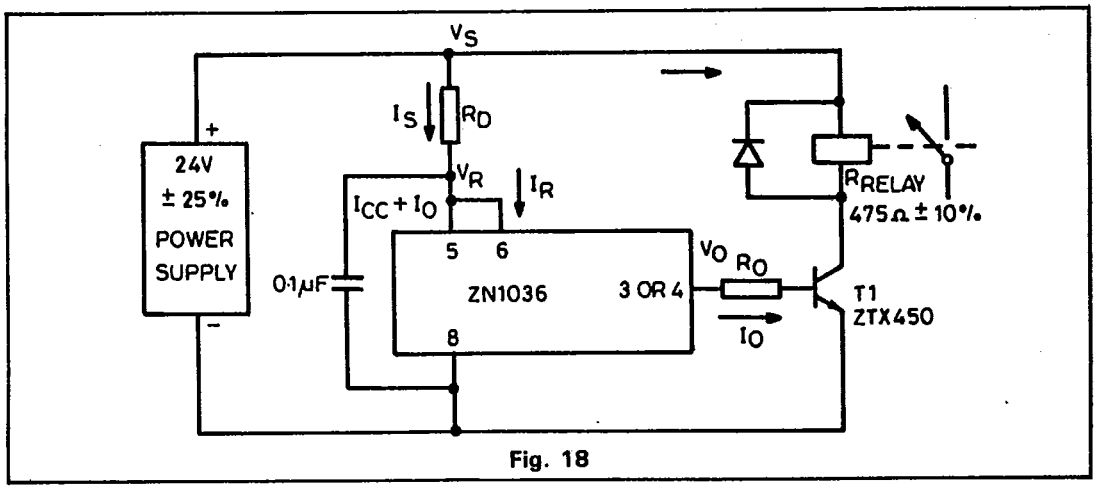


Fig. 18

N.B. The supply decoupling capacitor also acts as stabilisation for the internal regulator and the connection between pins 6 and 5 should therefore be as short as possible.

The values of R_O and R_D used in the circuit of Fig. 18 are calculated as follows. For R_O we need $I_{O(Min)}$, the minimum current required into the base of T_1 for worst case conditions.

$$I_{O(Min)} = I_{B(Max)}$$

$$= \frac{1}{h_{FE(Min)}} \times \frac{24(+25\%)}{475(-10\%)}$$

$$= \frac{1}{50} \cdot \frac{30}{427}$$

$$\mathbf{I_{O(Min)} = 1.4mA}$$

Deriving $V_{O(Min)}$ for the output circuit (Fig. 11)

$$V_{O(Min)} = V_{R(Min)} - 2 \times (\text{Internal } V_{BE})$$

$$= 4.7 - 1.4$$

$$\mathbf{V_{O(Min)} = 3.3 \text{ volts}}$$

Hence $$R_O = \frac{3.3 - V_{BE\,T_1}}{1.4}\ k\Omega \quad (V_{BE\,T_1} = 0.6V)$$

$$= 1.9k$$

Choose $\mathbf{R_O = 1.8k}$ (Nearest lower preferred value)

To calculate R_D we need $V_{O(Max)}$ and $I_{S(Min)}$

As above $$V_{O(Max)} = V_{R(Max)} - 2 \times (\text{Internal } V_{BE})$$

$$= 5.3 - 1.4V$$

$$\mathbf{V_{O(Max)} = 3.9 \text{ volts}}$$

and with the value of R_O chosen the actual current is

$$I_{O(Max)} = \frac{3.9 - V_{BE\,T_1}}{1.8} = 1.8mA$$

From which the minimum allowable supply current can be obtained

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$

$$= 5 + 1 + 1.8$$

$$\mathbf{I_{S(Min)} = 8.8mA}$$

Hence $$R_D = \frac{V_{S(Min)} - V_{R(Max)}}{I_{S(Min)}}$$

$$= \frac{18 - 5.3}{8.8}\ k$$

$$\mathbf{R_D = 1.5k} \text{ (Nearest preferred value)}$$

The power dissipated in the dropping resistor and the ZN1036 can be obtained also from

$$I_{S(Max)} = \frac{V_{S(Max)} - V_{R(Min)}}{1.5k(-5\%)}$$

$$= \frac{30-4.7}{1.425}\ mA$$

$$I_{S(Max)} = \mathbf{18mA}$$

Hence the ZN1036 dissipation = 90mW max. and power dissipation by dropping resistor = 450mW max.

The calculations assume ±2% tolerance resistors.

3.2.2 a.c. mains supplies

A transformer may be used to drop the voltage from the mains and a rectified d.c. supply provided as discussed in 3.2.1

However the on-chip shunt regulator makes the transformer unnecessary since the supply may be obtained directly from the mains or from any other source of a.c. or d.c. higher than 5 volts. With a load such as the directly driven triac (sections 2.5.3 and 2.5.4) a half wave rectifier is used since either the line or neutral has a connection common to the load circuit and the I.C. supply thus preventing the use of a bridge rectifier.

The calculation of the smoothing and voltage dropping components is described below.

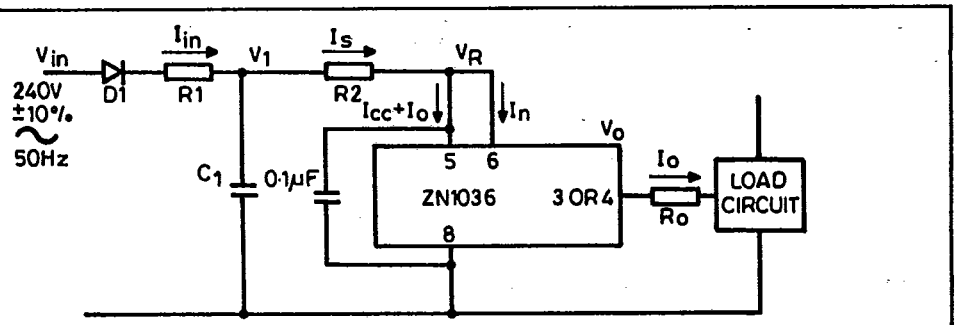


Fig. 19

The value of R_O and $I_{O(Max)}$ are calculated as in 3.2.1 and as an example a current $I_{O(Min)}$ of 10mA is assumed (the gate current for a 0.35A Triac, RS 202).

Therefore $V_{O(Min)} = \mathbf{3.3V}$

$$R_O = \frac{3.3 - V_G}{10.10^{-3}}\ \Omega \quad (V_G T_1 = 2V \text{ for RS } 202)$$

$R_O = \mathbf{120\Omega}$ (Nearest lower preferred value)

$V_{O(Max)} = \mathbf{3.9V}$

Hence $I_{O(Max)} = \frac{3.9 - V_G}{0.12}\ mA$

$I_{O(Max)} = \mathbf{16mA}$

And the minimum value of supply current for correct operation is therefore T-51-19

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$

$$= 5 + 2 + 16$$

$$\mathbf{I_{S(Min)} = 23mA}$$

If we assume that C1 is a 25 volt working capacitor and that 3 volts peak to peak ripple is allowable then the highest value for $V_{1(Min)}$ will be

$$V_{1(Min)} = 25(-20\%) - 3 \text{ (Allowing for } \pm 10\% \text{ variation in mains supply)}$$

$$\mathbf{V_{1(Min)} = 17V}$$

Therefore

$$R_2 = \frac{17 - V_{R(Max)}}{23} \text{ k}\Omega$$

$$\mathbf{R_2 = 510\Omega} \text{ (Nearest preferred value)}$$

The current i_{in} will flow for very nearly the full half cycle, 10ms in the case of 50Hz supplies, since V_1 is low compared to the peak mains voltage.

Now

$$i_{in(avg)} = \frac{V_{in(pk)} - V_{1(avg)}}{\pi R_1}$$

and this current from the rectifier must be equal to the current into the timer circuit.

$$i_{in(avg)} = I_{S(avg)}$$

and the average value of this current is

$$I_{S(avg)} = \frac{V_{1(Min)} + V_{RIPPLE(avg)} - V_{R(Min)}}{R_2}$$

$$= \frac{17 + 1.5 - 4.7}{510}$$

$$= 27mA$$

Therefore

$$R_1 = \frac{\sqrt{2} \times 240\,(-10\%) - (17 + 1.5)}{\pi \times 27} \text{ k}\Omega$$

$$= \mathbf{3k3} \text{ (Nearest preferred value)}$$

For the required ripple of 3V pk.pk. we can obtain

$$C_1 = \frac{I_{S(avg)} \times 10ms}{3}$$

$$C_1 = \frac{27 \times 10^{-5}}{3}$$

$$\mathbf{C_1 = 100\mu F} \text{ (Nearest higher preferred value)}$$

In order to calculate the maximum power dissipation in the dropping resistor we need to know $i_{in(avg)}$ for the upper limit of mains voltage.

Maximum value of $i_{in(avg)} = \frac{V_{in(pk)(Max)} - V_{1(Max)}}{\pi R_1}$

$= \frac{2 \times 240\ (+10\%) - 20}{h \times 3.3 \times 10^3}$

Max. $i_{in(avg)}$ = 34mA

and Max dissipation in $R_1 = \frac{\pi^2}{4} \times i_{in}^2{}_{(avg)} \times R_1$

P_{R1} = 9.4 watts

When a d.c. load such as the thyristor relay driver of section 2.4.2 is required then a full wave bridge circuit can be used as shown below.

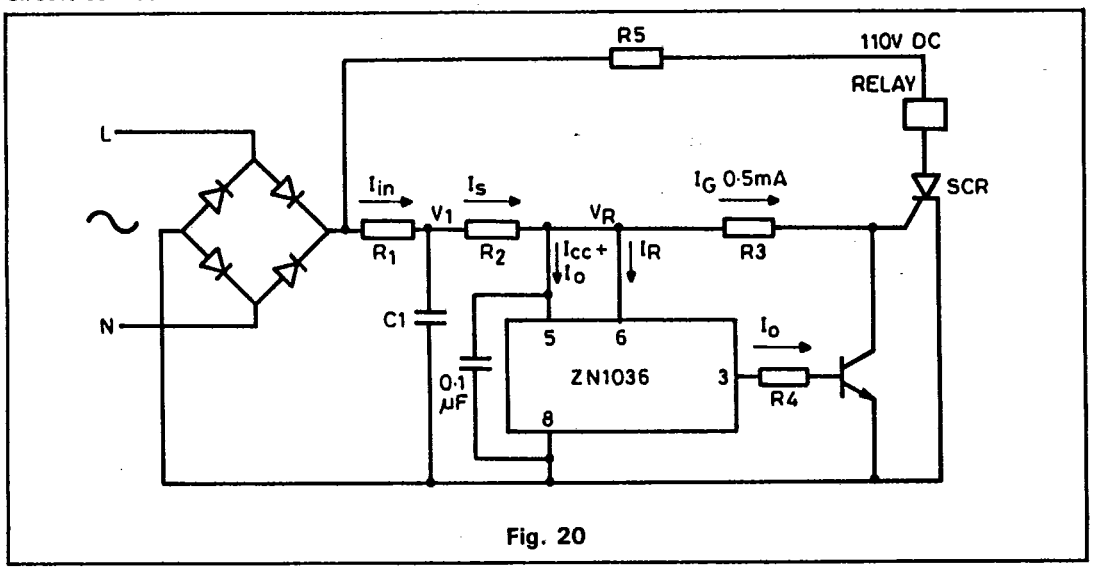


Fig. 20

The DELAY-TO-OFF timer circuit of Fig. 13 has been taken as an example. A typical circuit might have the relay resistance equal to $R_5 = 10k$ and for a 240V ± 10% mains supply the SCR could be a BRX49 which requires less than 0.5mA on gate current. To ensure gate turn-off a ZTX450 transistor with a base current of 0.5mA is sufficient with the above load.

Hence $I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)} + I_G$

$= 5 + 2 + 0.5 + 0.5$

$I_{S(Min)}$ = 8mA

Choosing C_1 to be 25 volts working and 3 volts peak to peak ripple as in the previous example. Then

$V_{1(Min)} = 25\ (-20\%) - 3$

= 17 volts

And $R_2 = \frac{17 - V_{R(Max)}}{8}\ K\Omega$

= **1.5k** (Nearest preferred value)

To find the value of C_1 required estimate the angle of conduction. Thus for a sine wave input conduction with change when the voltage on the smoothing capacitor is equal to the instantaneous value of the input voltage less the rectifier voltage drop.

So $V_1 + 1.2 = V_{in(pk)} \text{ Sin } \theta$

and for small values $\theta = \text{Sin } \theta$

Hence $\theta = \dfrac{V_1 + 1.2}{V_{in(pk)}}$

(assuming 1.2 volt drop across the briage rectifier).

for the rising sine wave $\theta_r = \dfrac{V_{1(Min)} + 1.2}{V_{in(pk)}}$

and for the falling sine wave $\theta_f = \dfrac{V_{1(Max)} + 1.2}{V_{in(pk)}}$

$$\theta_{tot} = \frac{V_{1(Min)} + V_{1(Max)} + 2.4}{V_{in(pk)}}$$

$$= \frac{17 + 20 + 2.4}{305}$$ (Taking lowest mains input as worst case).

$$= 0.13 \text{ radian}$$

The angle of non conduction $\theta_{tot} \simeq 8°$ and the capacitance will discharge by 3 volts in this period which in terms of time is

$$t = \frac{8}{180°} \times 10\text{ms (for 50Hz mains)}$$

$$= 0.44\text{ms}$$

and since $C \simeq \dfrac{\Delta t}{\Delta V} \cdot I_{S(Max)}$ $\qquad (I_{S(Max)} \simeq I_{S(Min)} + 20\%)$

$$\simeq \frac{44 \times 10^{-5}}{3} \times 8 \times 10^{-3} \ (+20\%)$$

$$\simeq 1.4\mu F$$

So we can choose a $2.2\mu F$ of 25 volt working or higher for C_1.

The mains dropping resistor can be simply obtained with sufficient accuracy by assuming 100% conduction. Thus

$$R_1 = \frac{2}{\pi} \times \frac{V_{in(pk)} - V_{1(Max)}}{I_{S(Min)}}$$

$$= \frac{2 \times 305\ 1\ 20}{\pi \times 8 \times 10^{-3}}$$

(Lowest mains voltage gives worst case).

$$\simeq 22\text{k (Next lowest preferred value)}$$

In order to calculate the power dissipated by the dropping resistor P_{R1} we need to know $i_{in(avg)}$ for the higher limit of the supply.

Maximum value of $$i_{in(avg)} \simeq \frac{2\,(V_{in\,(pk)\,(Max)} - V_{1(Max)})}{\pi\, R_1}$$

$$= \frac{2}{\pi}\left[\frac{2 \times 240\,(+10\%) - 20}{22 \times 10^{-3}}\right]$$

$$i_{in(avg)} = \mathbf{10mA}$$

Hence $$P_{R1} = \frac{\pi^2}{8} \times 10^{-4} \times 22 \times 10^3$$

$$P_{R1} = \mathbf{2.7\ watts}$$

The calculations have been performed using the 235V ±10% 50Hz mains figures. Similar calculations may be done for 110V 60Hz or whatever supplies are available.

Note 3.3 Reference supply

The 2.6V reference on pin 16 may be used for an external reference other than for the timing components.

SECTION 4 INTERFERENCE SUPPRESSION

Two types of interference, mains borne and electromagnetically radiated interference, can affect the operation of the timing circuit. In environments where such noise is encountered steps should be taken to reduce its effect on the timing circuit and the following notes should enable the circuit designer to avoid interference problems. The points discussed are illustrated by referring to a mains delay-to-on, and timer design illustrated in Figs. 21 and 22.

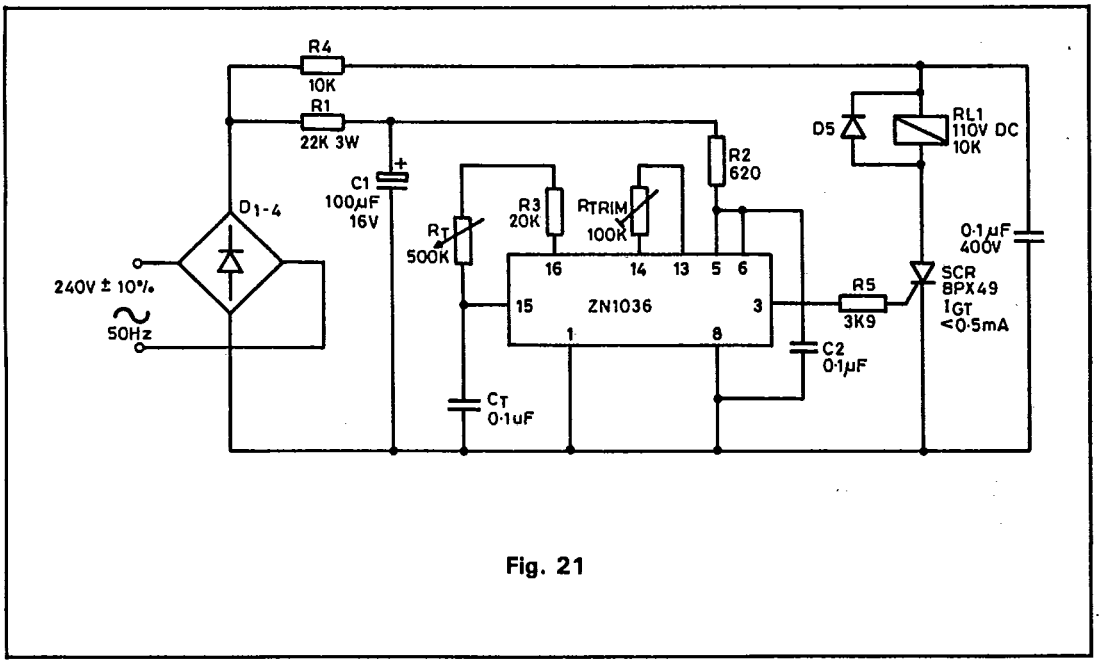


Fig. 21

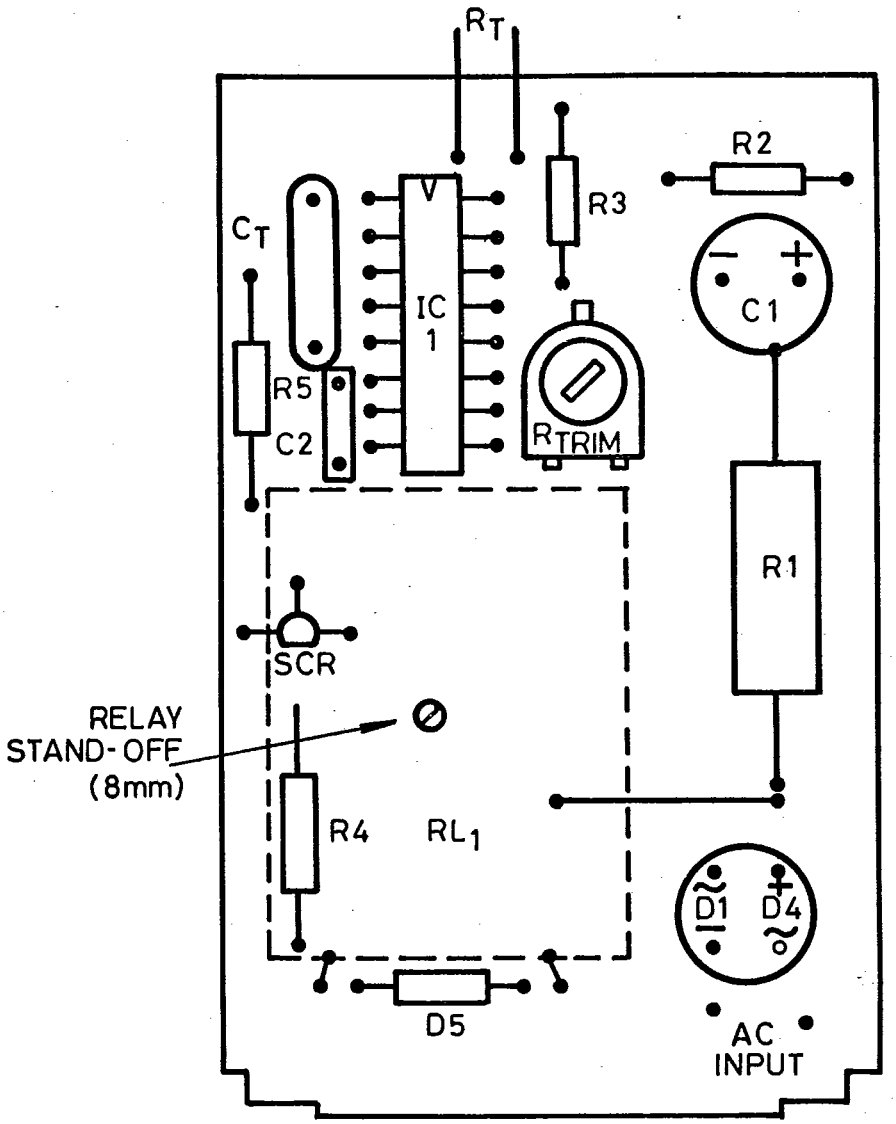


Fig. 22

Note 4.1 Mains borne interference

If the supply is reduced below (typically) 3.5V at any time, even for less than a microsecond then the logic and counter section of the ZN1036 will be reset and restoration of the normal supply may result in the initiation of a new timing period regardless of the initiation state. The effects of pulses on the supply are described in operating note 2.1.

Positive spikes are effective only when they produce a negative overshoot large enough to cause reset.

Negative spikes can be reduced by using a full diode bridge circuit, as in Fig. 21 which rectifies the spikes as well as the a.c. supply, or a half bridge where an a.c. load is being driven and the timer ground cannot be separated from neutral. The dropping resistor R_1, with C_1, forms a low pass filter for mains smoothing and additional filtration is provided by R_2 and C_2. These filters will also attenuate noise spikes. The shunt regulator in conjunction with the dropping resistors R_1 and R_2 provides considerable spike attenuation as well as d.c. regulation. The circuit of Fig. 21 for example, has an attenuation of supply spikes of 15000:1 due to the regulator alone. When a 5 volt supply designed for TTL, or similar requirements is available and the shunt regulator is not connected, protection against interference is not usually necessary since the supply itself should be capable of suppressing mains borne interference.

If a transformer is used to isolate the timer from the mains then the voltage drop can be devided between the transformer and the series resistor. The greater the series resistance then the greater the attenuation of noise by the shunt regulator and the smoothing capacitor. A transformer drop to 24V d.c. is a useful compromise allowing the use of 24V relays. The transformer itself will attenuate high frequency spikes.

Note 4.2 Electromagnetically induced noise

The ZN1036 oscillator frequency is determined by the time taken to change C_T via R_T from about 1.6 to 2.2 volts on pin 15. A single interference pulse of 0.1V on this pin could cause an error on a single time constant of 20% but since the timing period of a ZN1036 timer is made up of 511, 1023, 2047, or 4095 RC charging times then a large number of interference pulses in a timing period would be required to cause such a timing error. Where such interference exists, and bearing in mind that for a constant rate of interference pulses the effect becomes greater for increasing length of time period, steps should be taken to screen pin 15 from eletro-magnetically induced noise. Since the oscillator is required to operate for example in one of its modes at

$$\frac{4095}{20 \times 10^{-3}} \text{ Hz},$$

i.e. 200kHz, pin 15 is sensitive to radiated high frequency interference. Mains borne pulses can be equally troublesome if steps are not taken to isolate pin 15 from such interference. The method used in the design example of Fig. 22 is effective against both EMI and Mains Borne noise. A ground plane is produced by leaving a large area of copper on the component side of a double sided PCB with clearance holes for the component connections. The ground pin (8) is connected to the earth plane and the earthy side of components such as C_T and the decoupling capacitors are also connected directly to the ground plane. In this way the connections have a low impedance to pin 8 and the possibility of coupling interference pulses from the load or decoupling components into the oscillator circuit via common earth leads is reduced considerably. At the same time the printed circuit connections are screened from EMI.

An external screen such as a metal case can be effective against radiated interference but it does not have the advantage of an earth plane with regard to the reduction of common earth lead interference.

Any leads connected to pin 15 are susceptable to interference pick-up and should be screened. A remote variable timing resistor can be connected to the PCB either by twin screened lead with the screen to ground or single screened with the screen connected to pin 16. It will be noticed that the fixed part of the timing resistance is connected very close to pin 15 to help decouple the connecting leads to the variable resistor.

When the ZN1036 oscillator frequency is near to that of the mains supply, or to low harmonics, care should be taken in the layout of the circuitry and in the position of components such as mains transformers to obviate this effect. Stray coupling of mains frequencies can have the effect of locking the oscillator to that frequency and producing a band over which variation in timing components will not cause a corresponding variation in timing period.

SECTION 5 TIMER CALIBRATION

T-51-19

5.1 Direct measurement

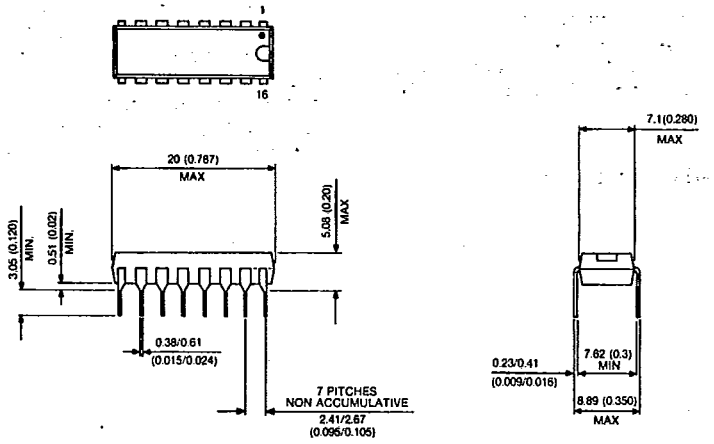
Timer circuits may be calibrated directly by measuring the time period between changes of state on the output pins 3 or 4. Accuracies of better than 0.2% can be achieved using this method.

5.2 Oscillator period measurement

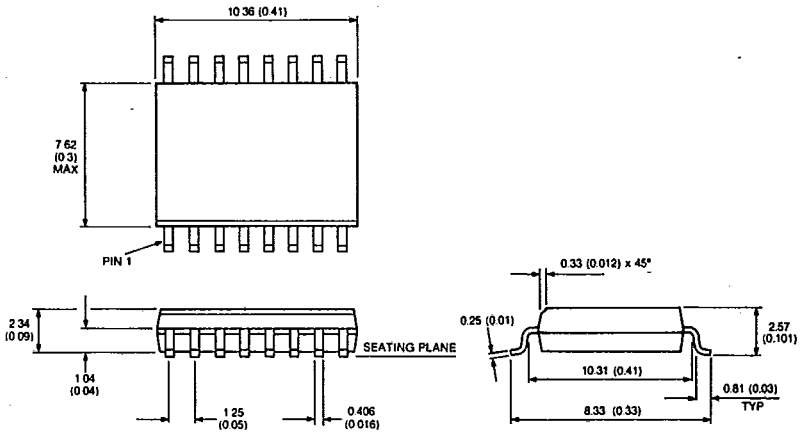
The measurement of oscillator period is a much quicker method of calibration and this is made possible on the ZN1036 by the inclusion of a low impedance output. This output is Pin 12 and an external pull up resistor of 5-10k is required. This enables the designer to calibrate the oscillator easily without affecting its operation and without the necessity for a high impedance probe.

PACKAGE DETAILS

Dimensions are in millimetres.



16-LEAD PLASTIC DIL - DP16



16-LEAD MINIATURE PLASTIC DIL (MP16 - WIDE BODY)