A-D CONVERTER

ZN427E-8
ZN427J-8

FERRANTI semiconductors ®

Microprocessor Compatible 8 Bit Successive Approximation A - D Converter

FEATURES

- Easy interfacing to microprocessors, or operates as a 'stand-alone' converter
- Fast: 10 μs conversion time guaranteed
- No missing codes over operating temperature range
- Data outputs 3-state TTL compatible, other logic inputs and outputs TTL and CMOS compatible
- Choice of on-chip or external voltage reference
- Ratiometric operation
- Unipolar and bipolar input ranges
- Complementary to ZN428 DAC
- Choice of commercial or military temperature range

DESCRIPTION

The ZN427 is an 8-bit successive approximation converter with 3-state outputs to permit easy interfacing to a common data bus. The IC contains a voltage switching DAC, a fast comparator, successive approximation logic and a 2.56 volt precision band-gap reference, the use of which is pin-optional to retain flexibility. An external fixed or varying reference may therefore be substituted, thus allowing ratiometric operation.

Only passive external components are required for operation of the converter.

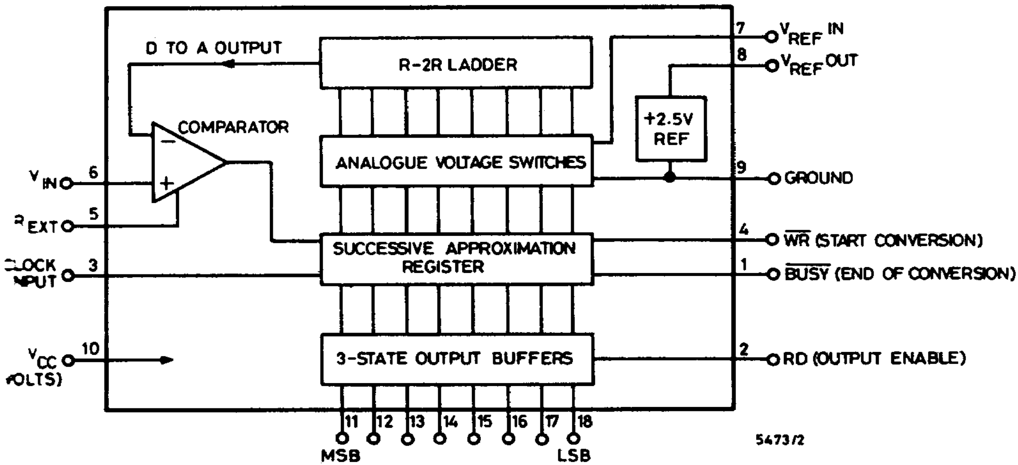


Fig. 1 – System Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	+7.0 volts
Max. Voltage, Logic and V_{REF} inputs	V_{CC}
Operating temperature range	0°C to +70°C (ZN427E-8) –55°C to +125°C (ZN427J-8)
Storage temperature range	–55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
CONVERTER					
Resolution	8	—	—	Bits	
Linearity Error	—	—	±0.5	LSB	
Differential Non-Linearity	—	±0.5	—	LSB	
Linearity Error T.C.	—	±3	—	ppm/°C	
Differential Non-Linearity T.C.	—	±6	—	ppm/°C	
Full Scale (Gain) T.C.	—	±2.5	—	ppm/°C	External Ref. 2.5V
Zero T.C.	—	±8	—	μV/°C	
Zero Transition 00000000 to 00000001	12	15	18	mV	$V_{REF\ IN}$ = 2.560V
F.S. Transition 11111110 to 11111111	2.545	2.550	2.555	V	$V_{REF\ IN}$ = 2.560V
Conversion Time	—	—	10	μs	See Note 1
External Reference Voltage	1.5	—	3.0	V	
Supply Voltage (V_{CC})	4.5	—	5.5	V	
Supply Current	—	25	40	mA	
Power Consumption	—	125	—	mW	
COMPARATOR					
Input Current	—	1	—	μA	V_{IN} = 3V, R_{EXT} = 82kΩ
Input Resistance	—	100	—	kΩ	V_{-} = –5V
Tail Current, I_{EXT}	25	—	150	μA	
Negative Supply, V–	–3.0	—	–30.0	V	See COMPARATOR
Input Voltage	–0.5	—	3.5	V	(Page 10)
INTERNAL VOLTAGE REFERENCE					
Output Voltage	2.475	2.560	2.625	V	R_{REF} = 390Ω C_{REF} = 4 μ7
Slope Resistance	—	0.5	2	Ω	
V_{REF} Temperature Coefficient	—	50	—	ppm/°C	
Reference Current	4	—	15	mA	See REFERENCE (Page 9)

ELECTRICAL CHARACTERISTICS (continued)

	Min.	Typ.	Max.	Units	Conditions
LOGIC					
(over operating temp.)					
High Level Input Voltage V_{IH}	2	—	—	V	
Low Level Input Voltage V_{IL}	—	—	0.8	V	
High Level Input Current,	—	—	50	μA	V_{IN} = 5.5V, V_{CC} = max.
$\overline{WR}$ and RD inputs I_{IH}	—	—	15	μA	V_{IN} = 2.4V, V_{CC} = max.
High Level Input Current,	—	—	100	μA	V_{IN} = 5.5V, V_{CC} = max.
Clock Input I_{IH}	—	—	30	μA	V_{IN} = 2.4V, V_{CC} = max.
Low Level Input Current I_{IL}	—	—	–5	μA	V_{IN} = 0.4V, V_{CC} = max.
High Level Output Current I_{OL}	—	—	–100	μA	
Low Level Output Current I_{OL}	—	—	1.6	mA	
High Level Output Voltage V_{OH}	2.4	—	—	V	I_{OH} = max., V_{CC} = min.
Low Level Output Voltage V_{OL}	—	—	0.4	V	I_{OL} = max., V_{CC} = min.
Disabled Output Leakage	—	—	2	μA	V_O = 2.4V
Input Clamp Diode Voltage	—	—	–1.5	V	
Read Input to Data Output	—	—	250	ns	See Fig. 8
Enable/Disable Delay Time t_{RD}	—	180	250	ns	
Start Pulse Width t_{WR}	250	160	—	ns	See Fig. 8
$\overline{WR}$ to $\overline{BUSY}$ Propagation	—	—	250	ns	
Delay t_{BD}	—	—	—		
Clock Pulse Width	500	—	—	ns	
Maximum Clock Frequency	900	1000	—	kHz	See Note 1

Note 1 : A 900 kHz clock gives a conversion time of 10μs (9 clock periods).

GENERAL CIRCUIT OPERATION

The ZN427 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{WR}$ input the $\overline{BUSY}$ output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF}/2$ from the DAC. This is compared to the input voltage V_{IN} ; a decision is made on the next negative clock edge to reset the MSB to 0 if $\frac{V_{REF}}{2} > V_{IN}$ or leave it set to 1 if $\frac{V_{REF}}{2} < V_{IN}$. Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2} + \frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to V_{IN} and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the ninth negative clock edge $\overline{BUSY}$ goes high indicating that the conversion is complete.

During a conversion the RD input will normally be held low to keep the 3-state buffers in their high impedance state. Data can be read out by taking RD high, thus enabling the 3-state outputs. Readout is non-destructive. The $\overline{BUSY}$ output may be tied to the RD input to automatically enable the outputs when the data is valid.

For reliable operation of the converter the start pulse applied to the $\overline{WR}$ input must meet certain timing criteria with respect to the converter clock. These are detailed in the timing diagram of figure 2.

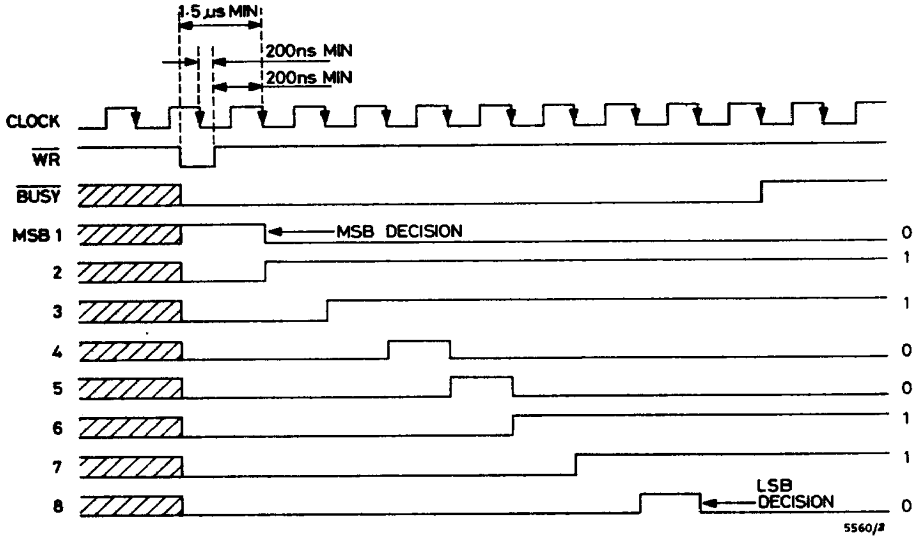


Fig. 2 Timing Diagram

NOTES ON TIMING DIAGRAM

1. A conversion sequence is shown for the digital word 01100110. For clarity the 3-state outputs are shown as being enabled during the conversion, but normal practice would be to disable them until the conversion was complete.

2. The $\overline{BUSY}$ output goes low during a conversion. When $\overline{BUSY}$ goes high at the end of a conversion the output data is valid. In a microprocessor system the $\overline{BUSY}$ output can be used to generate an interrupt request when the conversion is complete.

3. In the timing diagram cross hatching indicates a 'don't care' condition.

4. The start pulse operates as an asynchronous (independent of clock) reset that sets the MSB output to 1 and sets all other outputs and the end of conversion flag to 0. This resetting occurs on the low-going edge of the start pulse and as long as $\overline{WR}$ is low the converter is inhibited. Conversion commences on the first active (negative going) clock edge after the $\overline{WR}$ input has gone high again, when the MSB decision is made. A number of timing constraints thus apply to the start pulse.

(a) The minimum duration of the start pulse is 250ns, to allow reliable resetting of the converter logic circuits.

(b) There is no limit to the maximum duration of the start pulse.

(c) To allow the MSB to settle at least 1.5μs must elapse between the negative going edge of the start pulse and the first active clock edge that initiates the MSB desicion.

(d) To ensure reliable clocking the positive-going edge of the start pulse should not occur within 200 ns of an active (negative-going) clock edge. The ideal place for the positive-going edge of the start pulse is coincident with a positive-going clock edge. As a special case of the above conditions the start pulse may be synchronous with a negative-going clock pulse.

PRACTICAL CLOCK AND SYNCHRONISING CIRCUITS

The actual method of generating the clock signal and synchronising it to the start conversion pulse (or vice versa) will depend on the system in which the ZN427 is incorporated.

When used with a microprocessor the ZN427 can be treated as RAM and can be assigned a memory address using an address decoder. If the μP clock is used to drive the ZN427 and the μP write pulse meets the ZN427 timing criteria with respect to the μP clock then generating the start pulse is simply a matter of gating the decoded address with the microprocessor write pulse. Whilst the conversion is being performed the microprocessor can perform other instructions or No operation (NOP). When the conversion is complete the outputs can be enabled onto the data bus by gating the decoded address with the read pulse. A timing diagram for this sequence of operations is given in figure 3.

An advantage of using the microprocessor clock is that the conversion time is known precisely in terms of machine cycles. The data outputs may therefore be read after a fixed delay of at least nine clock cycles after the end of the $\overline{WR}$ pulse, when the conversion will be complete.

Alternatively the read operation may be initiated by using the $\overline{BUSY}$ output to generate an interrupt request.

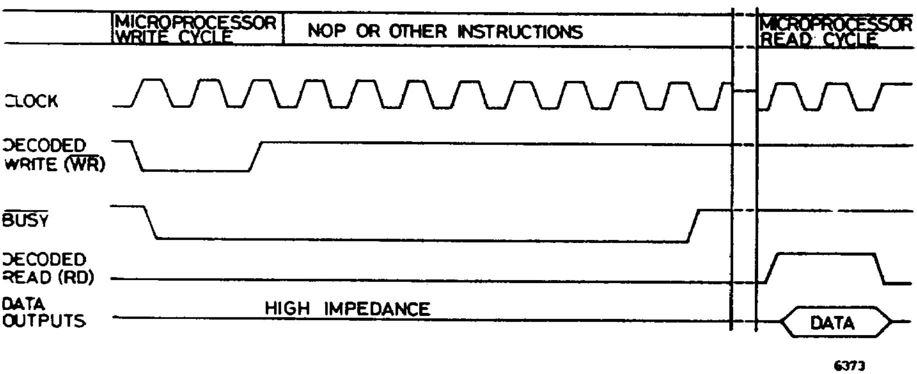


Fig. 3 Typical Timing Diagram Using μP clock and Write Pulse

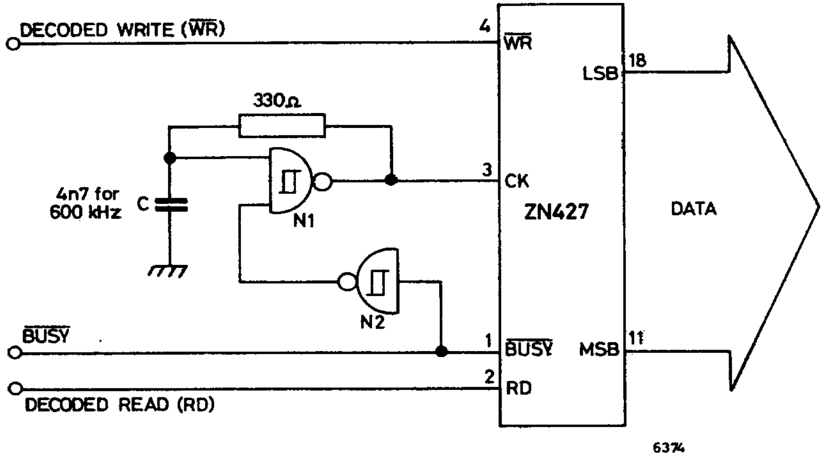
In some systems, for example single-chip microcomputers such as the 8048, this simple method may not be feasible for one or more of the following reasons:

(a) The MPU clock is not available externally.

(b) The clock frequency is too high.

(c) The write pulse timing criteria make it unsuitable for direct use as a start conversion pulse.

If any of these conditions apply then the self-synchronising clock circuit of figure 4a is recommended.



N1 N2 = ZN7413 or ½ 74132 Schmitt Trigger

$$f_{CK} = \frac{1}{360.C} \text{ (Hz, F)}$$

Fig. 4a. Self-Synchronising Clock Circuit

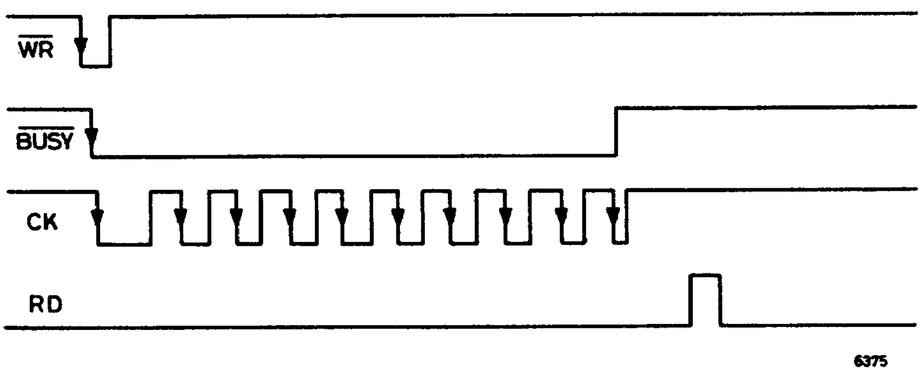


Fig 4b. Timing Diagram For Circuit of Figure 4a.

N1 is connected as an astable multivibrator which, when the $\overline{BUSY}$ output is high, is inhibited by the output of N2 holding one of its inputs low. The start conversion pulse resets the $\overline{BUSY}$ flag and N1 begins to oscillate. When the conversion is completed $\overline{BUSY}$ goes high and the clock is inhibited.

Since the start pulse starts the clock it may occur at any time. The only constraints on the start pulse are that it must be longer than 250 ns but at least 200 ns shorter than the first clock pulse. The first clock pulse is in fact longer than the rest since C1 starts from a fully charged condition whereas on subsequent cycles it charges between the upper and lower thresholds (V_{T+} and V_{T-}) of the Schmitt trigger.

LOGIC INPUTS AND OUTPUTS

The logic inputs of the ZN427 utilise the emitter-follower configuration shown in fig. 5. This gives extremely low input currents for CMOS as well as TTL compatibility.

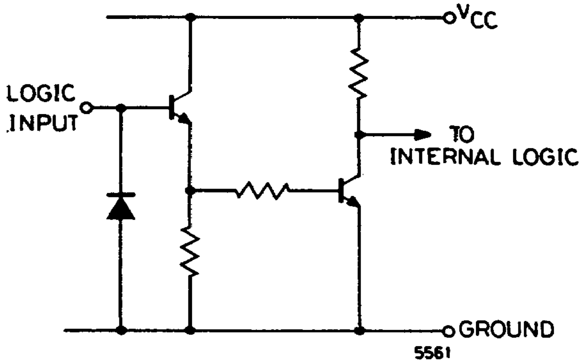
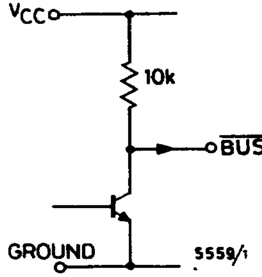


Fig. 5. Equivalent Circuit of all Inputs

The $\overline{BUSY}$ output, shown in figure 6, utilises a passive pullup for CMOS/TTL compatibility



The data outputs have 3-state buffers, an equivalent circuit of which is shown in figure 7. Whilst the RD input is low both output transistors are turned off and the output is in a high impedance state. When RD is high the data output will assume the appropriate logic state (0 or 1).

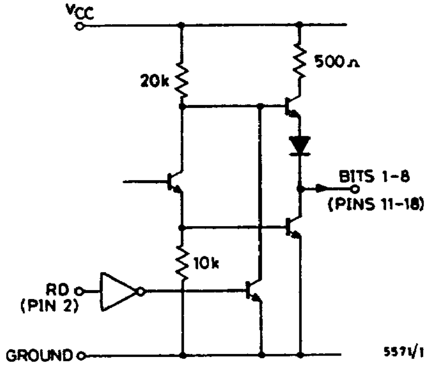


Fig. 7. Equivalent Circuit of Data Outputs

A test circuit and timing diagram for the output enable/disable delays are given in figure 8.

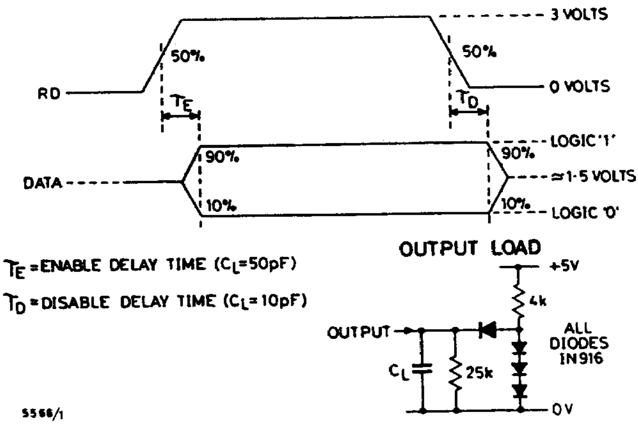


Fig. 8. Output Enable/Disable Waveforms

ANALOGUE CIRCUITS

D to A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in figure 9. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1 millivolt).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$\text{D to A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D to A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of V_{OS} is typically 2 mV for the ZN427E-8 (4 mV, ZN427J-8). This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (8 μV/°C) the effect on accuracy will be negligible.

The D to A output range can be considered to be 0-$V_{REF\ IN}$ through an output resistance R (4kΩ)

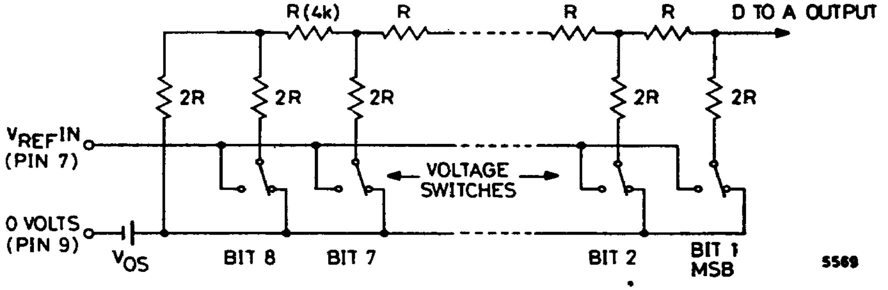


Fig. 9. R2-R Ladder Network

REFERENCE

(a) Internal Reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 10). A resistor (R_{REF}) should be connected between pins 8 and 10. The recommended value of 390Ω will supply a nominal reference current of (5.0 -2.5) /0.39 = 6.4mA. A stabilising/decoupling capacitor, C_{REF} (4μ7), is required between pins 8 and 9. For internal reference operation $V_{REF\ OUT}$ (Pin 8) is connected to $V_{REF\ IN}$ (Pin 7).

Up to five ZN427's may be driven from one internal reference, there being no need to reduce R_{REF}. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 3mA.

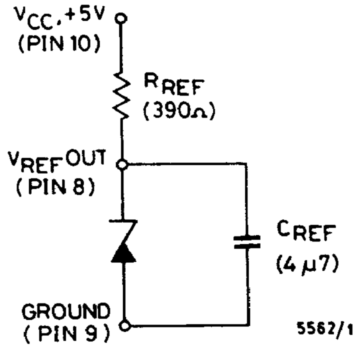


Fig. 10 Internal Voltage Reference

(b) External Reference

If required an external reference voltage in the range +1.5 to +3.0 volts may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$ where n is the number of converters supplied.

RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN427 should be derived from the same supply. The external reference can vary from +1.5 volts to +3.0 volts. The ZN427 will operate if $V_{REF\ IN}$ is less than +1.5 volts but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

COMPARATOR

The ZN427 contains a fast comparator, the equivalent input circuit of which is shown in Fig. 11.

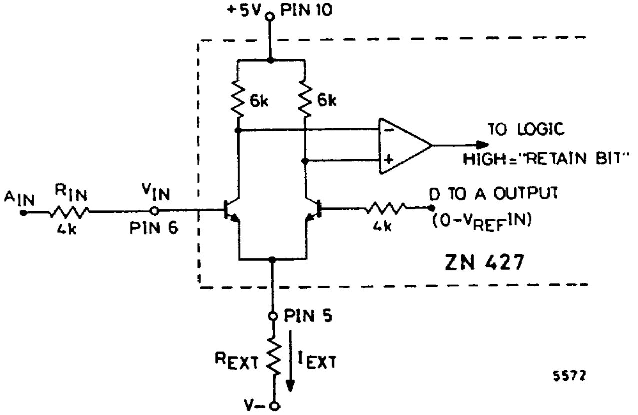


Fig. 11 Comparator Equivalent Circuit

The comparator derives the tail current, I_{EXT}, for its first stage from an external resistor, R_{EXT}, which is taken to a negative supply V−.

This arrangement allows the ZN427 to work with any negative supply in the range −3 to −30 volts. The ZN427 is designed to be insensitive to changes in I_{EXT} from 25μA to 150μA. The suggested nominal value of I_{EXT} is 65μA and a suitable value for R_{EXT} is given by $R_{EXT} = |V-|\,15k\Omega$.

V− (Volts)	R_{EXT} (±10%)
−3	47kΩ
−5	82kΩ
−10	150kΩ
−12	180kΩ
−15	220kΩ
−20	330kΩ
−25	390kΩ
−30	470kΩ

The output from the D to A converter is connected through the 4kΩ ladder resistance to one side of the comparator. The analogue input to be converted could be connected directly to the other comparator input (V_{IN}, Pin 6) but for optimum stability with temperature the analogue input should be applied through a source resistance (R_{IN} = 4kΩ) to match the ladder resistance.

ANALOGUE INPUT RANGES

The basic connection of the ZN427 shown in fig. 12 has an analogue input range 0 to $V_{REF\,IN}$, which, in some applications, may be made available from previous signal conditioning/scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by offsetting the analogue input range so that the comparator always sees a positive input voltage.

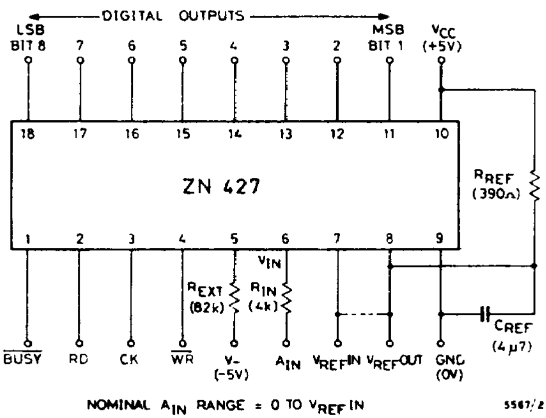


Fig. 12. External Components for Basic Operation

UNIPOLAR OPERATION

The general connection for unipolar operation is shown in figure 13.

The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the Analogue Input(A_{IN}) is at full scale. The resulting full scale range is given by:

$$A_{IN}\ FS = (1+\frac{R1}{R2}).\ V_{REF\ IN} = G.\ V_{REF\ IN}.$$

To match the ladder resistance R1//R2 ($\approx R_{IN}$) = 4kΩ.

The required nominal values of R_1 and R_2 are given by R_1 = 4G kΩ, $R_2 = \frac{4G}{G-1}$ kΩ.

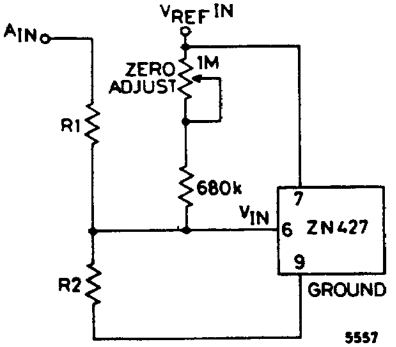


Fig. 13 Unipolar Operation - General Connection

Using these relationhips a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5 volts.

Input Range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

GAIN ADJUSTMENT

Due to tolerances in R_1 and R_2, tolerances in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least ±5% of its nominal value is suggested.

ZERO ADJUSTMENTS

Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 15mV applied to the comparator input, which corresponds to $+1\frac{1}{2}$ LSB with a 2.56 volt reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of $+\frac{1}{2}$ LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than $1\frac{1}{2}$ times $V_{REF\ IN}$.

Practical circuit values for +5V and +10V input ranges are given in fig. 14, which incorporate both zero and gain adjustments.

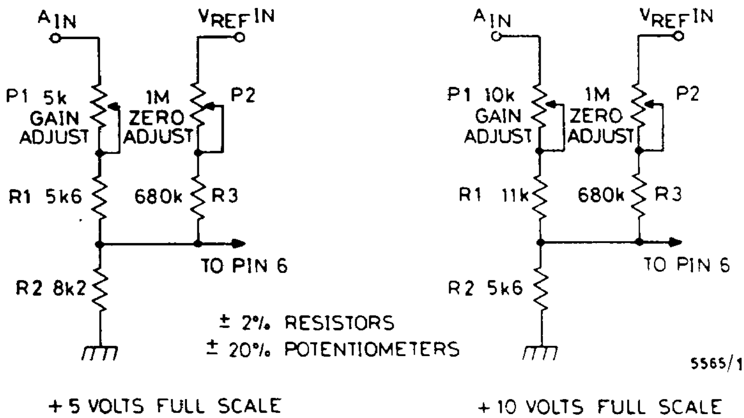


Fig. 14. Unipolar Operation - Component Values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

Apply full scale minus $1\frac{1}{2}$ LSB to A_{IN} and adjust gain until Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 1.

(iii) Apply $\frac{1}{2}$ LSB to A_{IN} and adjust zero until Bit 8 just flickers between 0 and 1 with all other bits at 0.

UNIPOLAR SETTING-UP POINTS

Input Range, +FS	$\frac{1}{2}$ LSB	FS $-1\frac{1}{2}$ LSB
+5V +10V	9.8 mV 19.5 mV	4.9707 volts 9.9414 volts

$$1\ \text{LSB} = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Analogue Input (A_{IN}) (Nominal code centre value)	Output Code (Binary)
FS −1 LSB	11111111
FS −2 LSB	11111110
¾ FS	11000000
½ FS + 1 LSB	10000001
½ FS	10000000
½ FS − 1 LSB	01111111
¼ FS	01000000
1 LSB	00000001
0	00000000

BIPOLAR OPERATION

For bipolar operation the input to the ZN427 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and V_{IN} (Fig. 15).

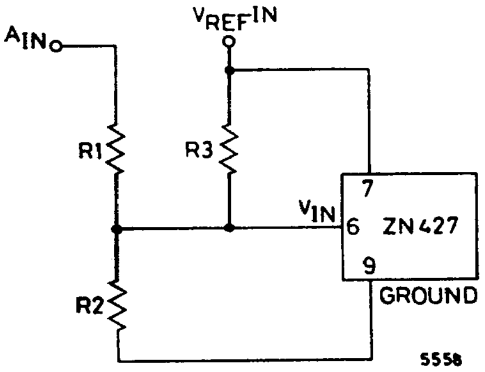


Fig. 15. Bipolar Operation - General Connection

When $A_{IN} = -FS$, V_{IN} needs to be equal to zero.

When $A_{IN} = +FS$, V_{IN} needs to be equal to $V_{REF\ IN}$.

If the full scale range is $\pm G$. $V_{REF\ IN}$ then $R_1 = (G - 1)$. R_2 and $R_1 = G$. R_3 fulfil the required conditions.

To match the ladder resistance $R_1/R_2/R_3$ $(=R_{IN}) = 4k\Omega$.

Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 8\ Gk\Omega$, $R_2 = 8G/(G - 1)k\Omega$, $R_3 = 8k\Omega$.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $+V_{REF\ IN}$) results if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5$ volts the nominal values of resistors for $\pm 5V$ and $\pm 10V$ input ranges are given in the following table.

Input Range	G	R_1	R_2	R_3
±5V ±10V	2 4	16 kΩ 32 kΩ	16 kΩ 10.66 kΩ	8 kΩ 8 kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig. 16.

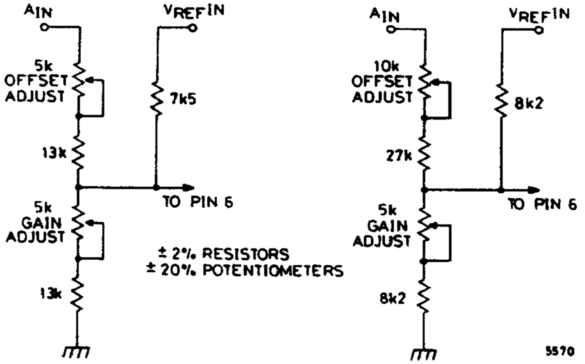


Fig. 16 Bipolar Operation - Component Values

Note that in the ±5V case R_3 has been chosen as 7.5 kΩ (instead of 8.2 kΩ) to obtain a more symmetrical range of adjustment using standard potentometers.

BIPOLAR ADJUSTMENT PROCEDURE

i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

ii) Apply $-(FS - \frac{1}{2}\ LSB)$ to A_{IN} and adjust offset until the Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.

iii) Apply $+(FS - 1\frac{1}{2}\ LSB)$ to A_{IN} and adjust gain until Bit 8 just flickers between 0 and 1 with all other bits at 1.

iv) Repeat step (ii).

BIPOLAR SETTING-UP POINTS

Input Range, ±FS	$-(FS - \frac{1}{2}\ LSB)$	$+(FS - 1\frac{1}{2}\ LSB)$
±5V ±10V	−4.9805V −9.9609V	+4.9414V +9.8828V

$$1\ LSB = \frac{2FS}{256}$$

BIPOLAR LOGIC CODING

Analogue Input (A_{IN}) (Nominal code centre value)	Output Code (Offset Binary)
+(FS − 1 LSB)	11111111
+(FS − 2 LSB)	11111110
+½ FS	11000000
+1 LSB	10000001
0	10000000
−1 LSB	01111111
−½ FS	01000000
−(FS − 1 LSB)	00000001
−FS	00000000

SINGLE 5 VOLT SUPPLY RAIL OPERATION

The ZN427 takes very little power from the negative rail and so a suitable negative supply can be generated very easily using a 'diode pump' circuit. The circuit shown in Fig. 17 works with any clock frequency from 10 kHz to 1 MHz and can supply up to five ZN427s.

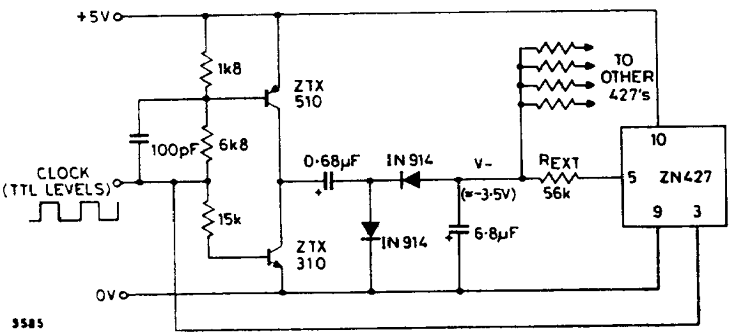
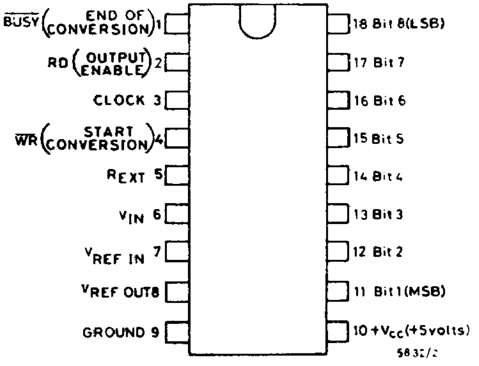
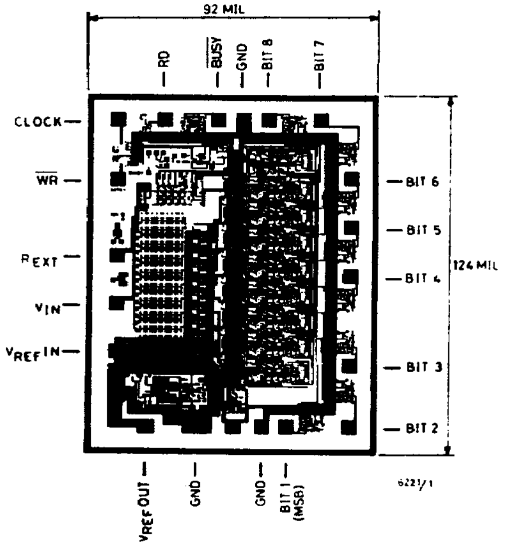


Fig. 17. Single 5 Volt Supply Operation

Pin Connections





Chip Dimensions and Layout

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	OPERATING TEMP. RANGE
ZN427E-8	Plastic	0°C to +70°C
ZN427J-8	Ceramic	–55°C to +125°C