PLESSEY
Semiconductors

T-51-09-08

ZN438E/J

8-BIT MICROPROCESSOR COMPATIBLE D-A CONVERTER

The ZN438 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus and a buffer amplifier to give a low analogue output impedance. The latch is transparent when $\overline{\text{ENABLE}}$ is low and the data is held when $\overline{\text{ENABLE}}$ is taken high.

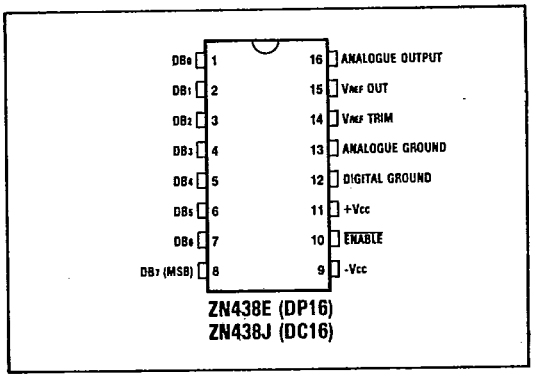
The ZN438 also contains a trimmable 2.5V reference which is internally connected to the R-2R ladder switches and to V_{REF} OUT.

FEATURES

- On-Chip High Speed Output Buffer Amplifier
- 1.25 microseconds Settling Time to ±0.5 LSB
- Trimmable Bandgap Reference
- Microprocessor, TTL and 5V CMOS Compatible
- Guaranteed Monotonicity over the Full Operating Temperature Range
- Commercial and Military Temperature Ranges

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN438E	0°C to +70°C	DP16
ZN438J	-55°C to +125°C	DC16



ZN438E (DP16)
ZN438J (DC16)

Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Supply voltage +Vcc	+7V
Supply voltage -Vcc	-9V
Logic input voltage	+Vcc
Operating temperature range	0°C to +70°C (ZN438E)
	-55°C to +125°C (ZN438J)
Storage temperature range	-55°C to +125°C
Analogue ground to digital ground	±200mV

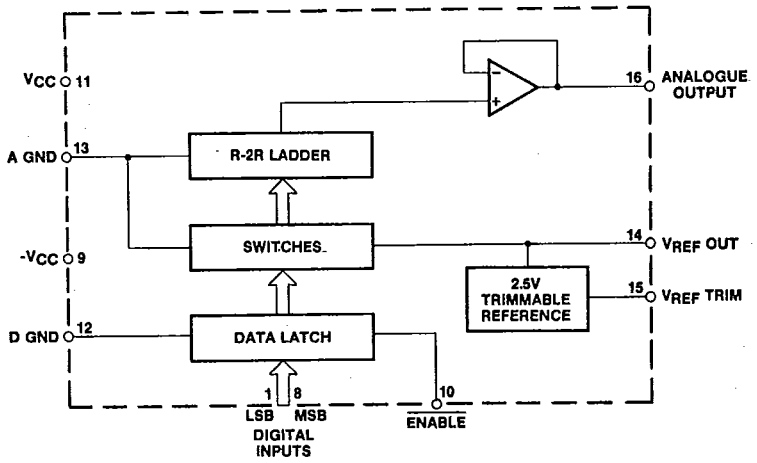


Fig.1 System diagram

ELECTRICAL CHARACTERISTICS (at $+V_{CC}=5V$, $-V_{CC}=-5V$, $T_{amb}=25°C$ with internal reference unless otherwise stated).

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Parameter	$T_{amb}=+25°C$			Over specified temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
D-A converter							
Resolution	8	–	–	8	–	Bits	
Accuracy	8	–	–	8	–	Bits	
Linearity error	–	–	±0.5	–	±0.5	LSB	
Differential linearity error	–	±0.5	–	–	±1	LSB	
Linearity error T.C.	–	±3	–	–	–	ppm/°C	
Differential linearity error T.C.	–	±6	–	–	–	ppm/°C	
Offset error	–	2	8	–	10	mV	
Offset error T.C.	–	±8	–	–	–	μV/°C	
Gain error	–	–	±0.5	–	–	LSB	With V_{REF} = 2.50V See note 1
Gain T.C.	–	60	–	–	150	ppm/°C	
Analogue output voltage	0	–	+2.7	0	+2.7	V	Note 2
Current	−3	–	+4	−3	+4	mA	$V_{out}=0$ to V_{ref}
Analogue output impedance	–	6	10	–	–	Ω	
Settling time to 0.5LSB							$V_{REF}=2.50V$ $C_{LOAD}=470pF$ $R_L=690Ω$
	–	1.25	–	–	–	μs	1LSB major transition
	–	2	–	–	–	μs	All bits ON to all bits OFF
	–	2	–	–	–	μs	All bits OFF to all bits ON

NOTE 1

For operation below −50°C the full-scale temperature coefficient may become significantly worse if V_{CC} is allowed to fall below 5V.

Note 2

In some cases the reference may be trimmed to give A_{out} greater than 2.7V. However, this should be avoided because the A_{out} may not be 8 bit accurate at voltages above this.

ELECTRICAL CHARACTERISTICS (Cont.)

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Parameter	$T_{amb} = +25°C$			Over specified temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
Internal voltage reference							
Output voltage	2.450	2.500	2.550	–	–	V	$R_L = 1.5K\Omega$ $C_L = 100nF$
Maximum trim range	–	±5	–	–	–	% of V_{ref}	$R_{TRIM} = 10K\Omega$
Output voltage T.C.	–	30	100	–	–	ppm/°C	
Reference current	1	–	5	1	5	mA	
Slope resistance	–	0.75	2	–	–	Ω	
Digital inputs							
High level input voltage	2	–	–	–	–	V	
Low level input voltage	–	–	0.8	–	–	V	
High level input current	–	–	60	–	–	μA	$V_{in} = 5.5V$ $V_{CC} = Max.$
High level input current	–	–	20	–	–	μA	$V_{in} = 2.4V$ $V_{CC} = Max.$
Low level input current	–	–	−5μA	–	–	μA	$V_{in} = 0.4V$ $V_{CC} = Max.$
Input clamp diode voltage	–	−1.5	–	–	–	V	$I_{in} = -8mA$
Enable pulse width t_W	100	–	–	–	–	ns	Refer to Fig. 7
Data set up time t_{DS}	150	–	–	–	–	ns	
Data hold time t_{DH}	10	–	–	–	–	ns	
Power supplies							
Supply voltage ($+V_{CC}$)	4.5	5	5.5	4.5	5.5	V	
Supply voltage ($-V_{CC}$)	−4.5	−5	−5.5	−4.5	−5.5	V	
Supply current ($+I_{CC}$)	–	35	–	–	–	mA	
Supply current ($-I_{CC}$)	–	12	–	–	–	mA	
Power consumption	–	235	–	–	–	mW	

D-A CONVERTER

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The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 2. Each 2R element is connected to 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

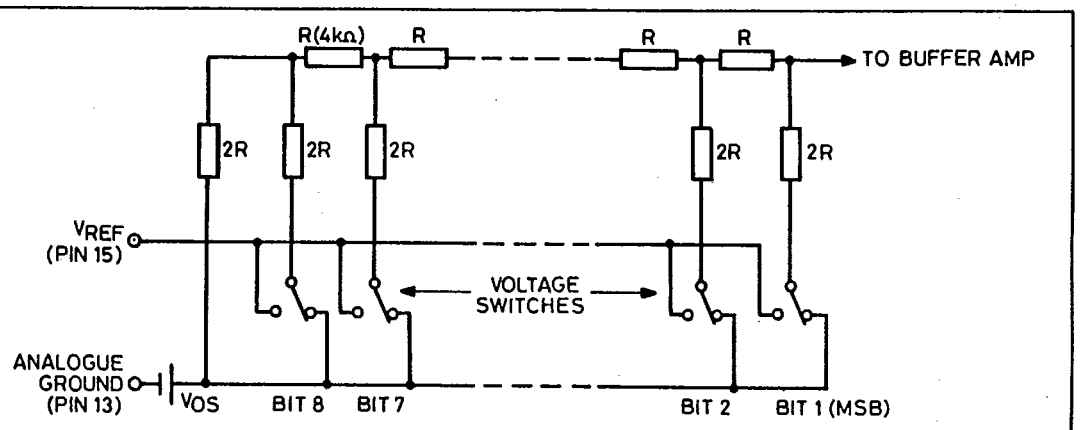

Fig. 2 The R-2R ladder network

$$\text{D-A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D-A from the data latch.

V_{OS} is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of V_{OS} is typically 1mV. This offset will normally be removed by the setting up procedure.

REFERENCE

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 3). A resistor (R_{REF}) should be connected between $+V_{CC}$ (pin 11) and pin 15. The recommended value of 1K5 will supply a nominal reference current of (5-2.5)/1500 = 1.7mA. A stabilising/decoupling capacitor $C_{REF} = 0.1\mu F$ is required between pins 15 and 13.

The reference voltage can be trimmed by ±5% with a 10K potentiometer (as shown in Fig. 4).

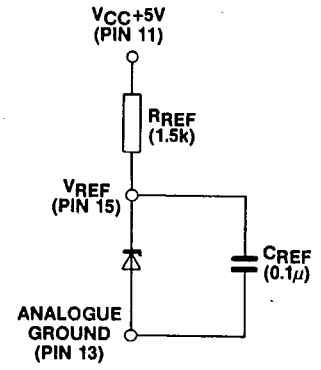

Fig. 3 Internal voltage reference

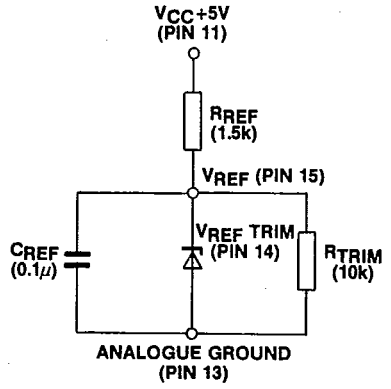

Fig. 4 Trimming circuit for the voltage reference

OPERATIONAL AMPLIFIER SECTION

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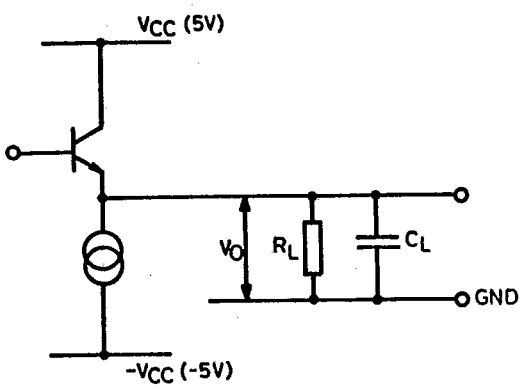

Fig. 5 Output stage

The D-A converter output is buffered by a unity gain, non-inverting amplifier with negligible offset error. Typically this buffer amplifier will develop 2.50V across an external load, and can drive capacitive loads of up to 470pF without a degredation of speed. The amplifier output can source 4mA and sink 3mA. The output stage of this amplifier consists of a bipolar transistor from the V_{CC} line and a current load to $-V_{CC}$ (the negative supply for the output amplifier). This output stage is shown in Fig. 5.

The power supply voltages can be increased, resulting in an improved performance in some parameters e.g. switching speed.

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the enable input is low the data inputs drive the D-A directly. When enable goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig. 6.

The ZN438 is provided with seperate analogue and digital ground connections. The circuit will operate correctly with as much as ±200mV between the two grounds.

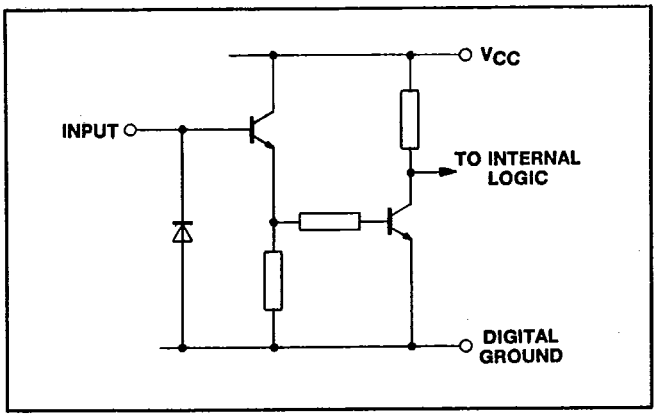

Fig. 6 Equivalent circuit of all inputs

TIMING AND CONTROL

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The ZN438 has input data latches to simplify connection to a microprocessor data bus. The enable control line is used to control the condition of the latches. If enable is low the latches become transparent and the D-A converter responds to the digital inputs. If enable is taken high then the latches retain the data which was present on the digital inputs just prior to enable assuming a high state. While enable is high the analogue output remains at the value corresponding to the data held in the latches.

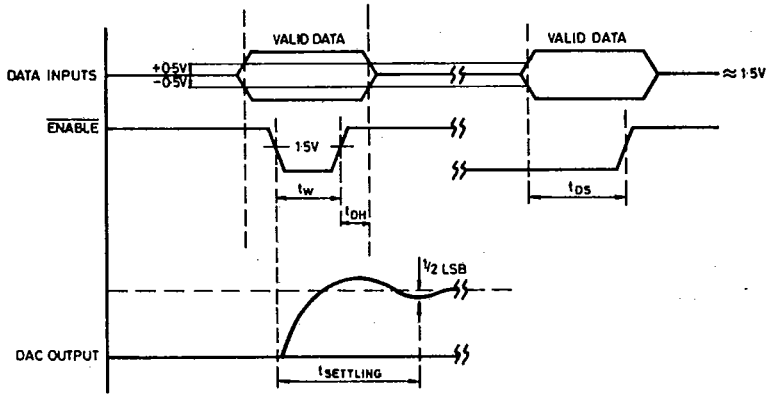
The function table is given in table 1 below.

Input data	$\overline{\text{Enable}}$	Latch output	Latch condition
0	0	0	Transparent
1	0	1	Transparent
0	⌐	0	Latching
1	⌐	1	Latching
X	1	Previous data	Latched

X = Don't care

⌐ = Low to high level transition

Table 1 ZN438 control logic function table



t_W = Enable pulse width
t_{DH} = Data hold time
t_{DS} = Data set-up time
$T_{SETTLING}$ = DAC output settling time to ±0.5LSB

Fig. 7 Timing diagram

GROUNDING

AC or transient voltages between analogue ground (pin 13) and digital ground (pin 12) can cause noise at the analogue output (pin 16). Digital systems are a source of noise which can be removed by connecting AGND and DGND together at the ZN438 or as close as possible to it. It is important that the voltage difference between AGND and DGND should not exceed 200mV.

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(1) UNIPOLAR OPERATION

The nominal output range of the ZN438 is 0V to (V_{REF} – 1LSB) where V_{REF} is typically 2.50V. A circuit diagram showing the minimum external components required to give this output range is shown in Fig. 8. The reference trim input is used to provide the necessary gain adjustment by allowing variations of the internal reference voltage by ±5%.

For unipolar output ranges greater than 2.50V an external amplifier is required. A general schematic diagram is shown in Fig. 9.

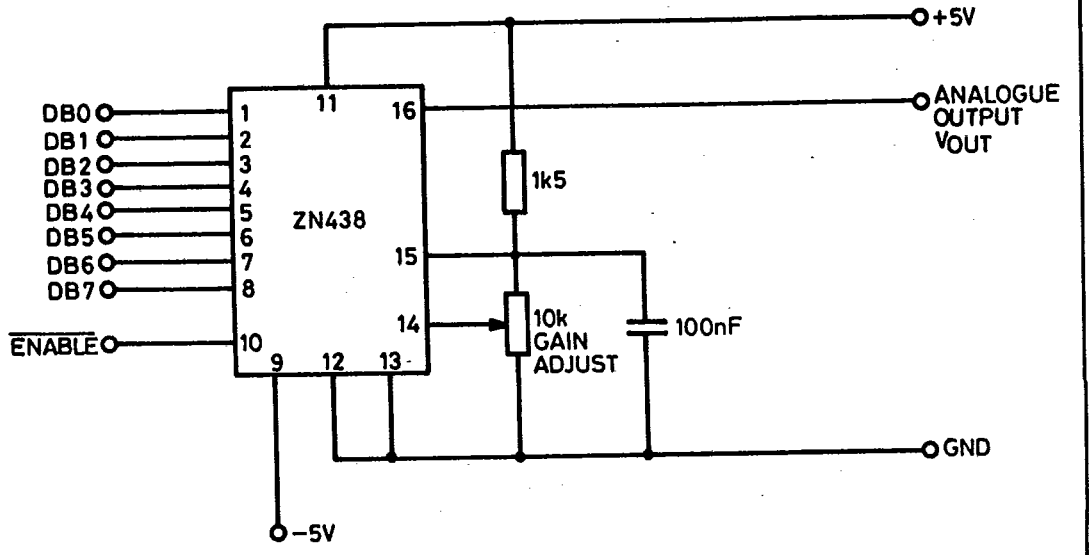

Fig. 8 Basic unipolar circuit diagram

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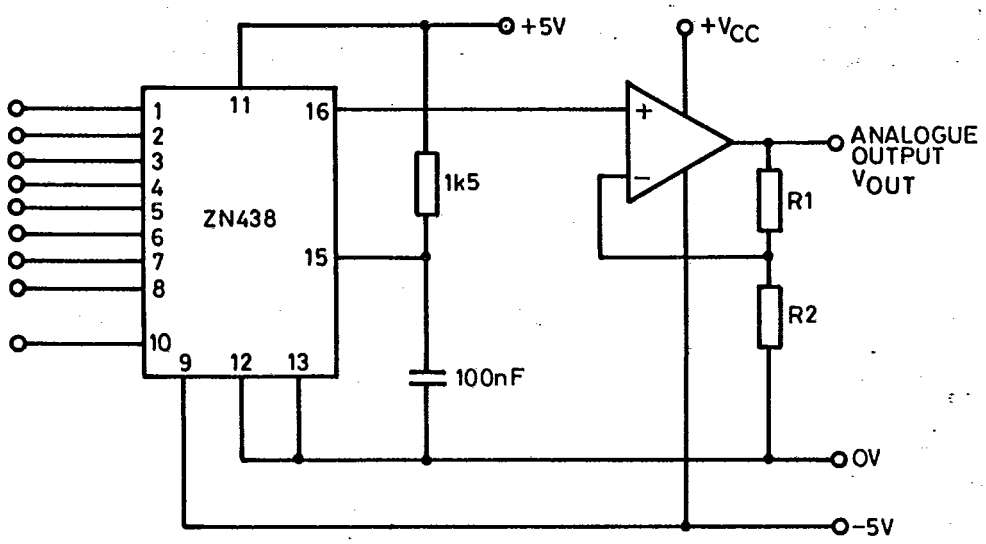

Fig. 9 Extended unipolar schematic diagram

The full-scale range of Fig. 9 is given by the equation:

$$V_{OUT\ FS} = \left(1 + \frac{R_1}{R_2}\right)(V_{REF} - 1LSB)$$
$$= G.(V_{REF} - 1LSB)$$

The circuit diagrams of Fig. 10 give typical component values for full-scale outputs of +5 and +10V. Zero offset adjustment is provided by use of the op-amp offset null capability. Gain adjustment is made by varying the value of R1.

The LF351 is a low cost JFET operational amplifier pin compatible with the industry standard 741. It features a high slew rate of 13 V/μs which gives a typical settling time for all bits on to all bits off (or vice versa) of 2μs for a 10V full-scale output. If a fast settling time is not required a 741 could be used as a direct replacement for the LF351. This would result in a typical settling time of 20μs for the conditions quoted above.

It can be seen from the gain equation that it is the relative and not the absolute value of the feedback resistors that is important. The values given here have been chosen to give minimum ringing on the output of the LF351 op-amp. As with all fast slew rate op-amps this can be a problem due to the minimal internal compensation used to achieve the fast slew rate. With lower slew rate amplifiers this will not be as much of a problem and hence the value of the feedback components could be increased if desired.

It should be noted that the V_{REF} trim potentiometer is no longer required as the gain adjustment is now provided by varying the op-amp feedback resistor R1.

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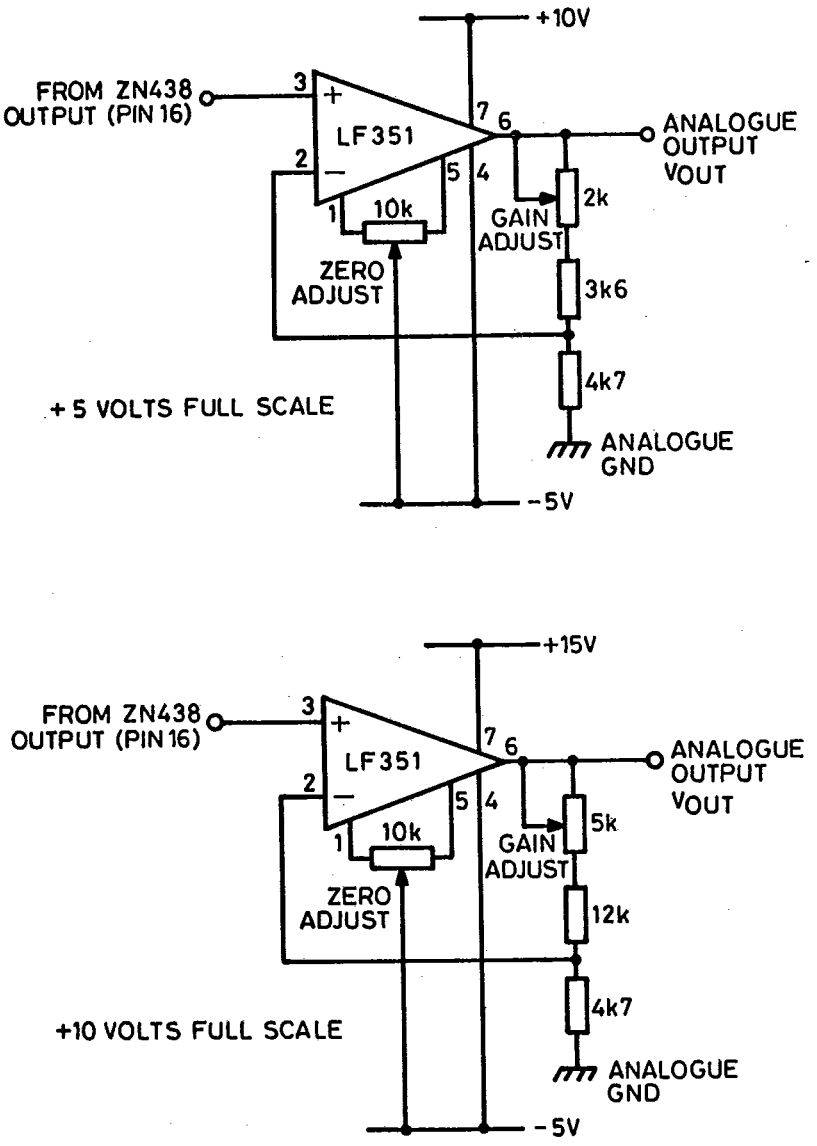

Fig. 10 Extended unipolar component values

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Unipolar adjustment procedure

(i) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust zero until $V_{OUT} = 0.0000V$. (Not applicable to Fig. 8 as no offset adjustment is available)

(ii) Set all bits ON (high) and adjust gain until $V_{OUT} = FS - 1LSB$.

Unipolar setting up points

Output range, +FS	LSB	FS - 1LSB
+2.50V	9.8mV	2.4902V
+5V	19.5mV	4.9805V
+10V	39.1mV	9.9609V

$$1LSB = \frac{FS}{256}$$

Unipolar logic coding

Input code (Binary)	Analogue output (Nominal value)
11111111	FS - 1LSB
11111110	FS - 2LSB
11000000	0.75FS
10000001	0.5FS + 1LSB
10000000	0.5FS
01111111	0.5FS - 1LSB
01000000	0.25FS
00000001	1LSB
00000000	0

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(2) BIPOLAR OPERATION

For bipolar operation the output from the ZN438 is offset by half full-scale by connecting a resistor between $V_{REF\ OUT}$ and the inverting input of the external amplifier. A general schematic diagram is shown in Fig. 11.

When the digital input to the ZN438 is zero its analogue output will be zero resulting in an output of −full-scale from the external amplifier. An input of all ones will give a ZN438 output of $+(V_{REF} - 1LSB)$ and a resulting amplifier output of +(full-scale −1LSB).

Practical circuit diagrams are given in Fig. 12 with typical component values for full-scale ranges of ±5 and ±10V. Note, the V_{REF} dropper resistor has been reduced from 1K5 to 1K1 to supply the amplifier feedback resistor current. Minus full-scale (offset) is set by adjusting R1 about its nominal value relative to R3. Plus full-scale (gain) is set by adjusting R2 relative to R1.

A bipolar output range of $\pm V_{REF}$ (which corresponds to the basic unipolar range 0 to V_{REF}) is obtained if $R_1 = R_3 = 3K9$ and $R_2 = \infty$.

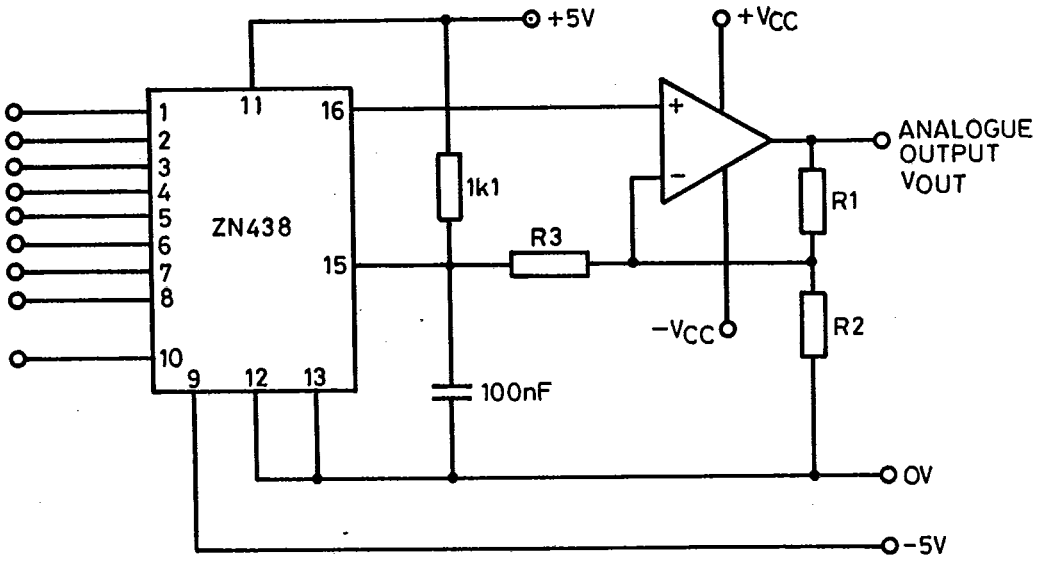

Fig. 11 Bipolar schematic diagram

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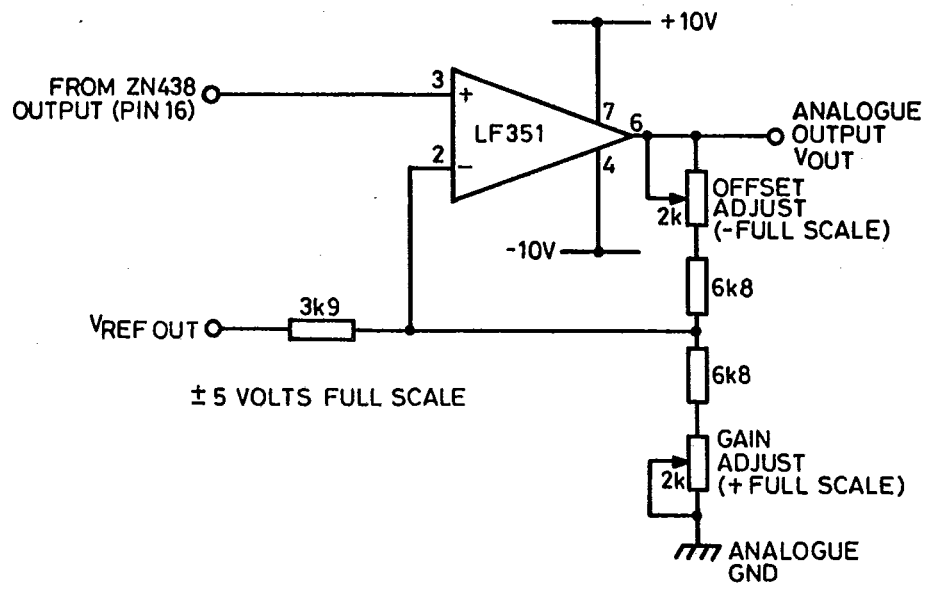

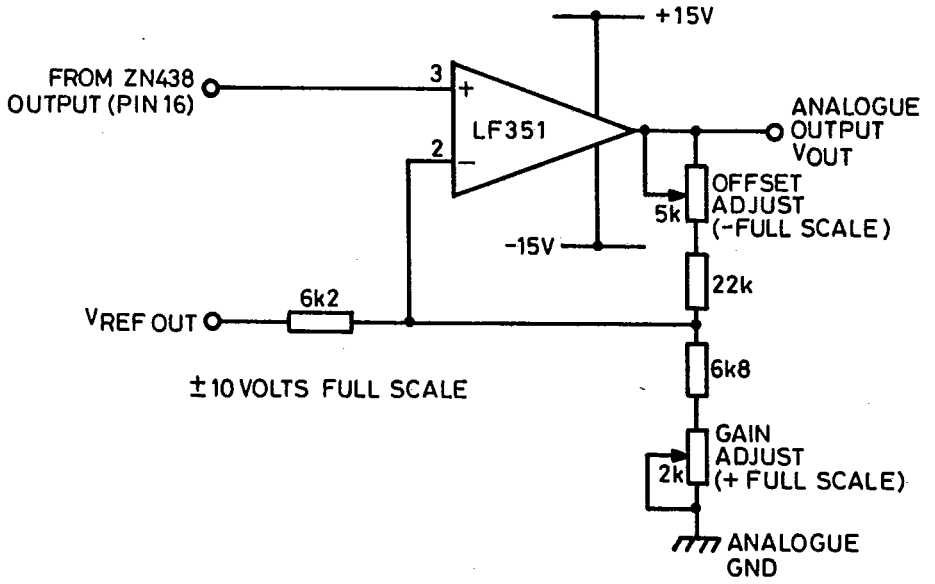

Fig. 12 Bipolar component values

Bipolar adjustment procedure

(i) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust offset until the amplifier output reads −full-scale.

(ii) Set all bits ON (high) and adjust gain until the amplifier output reads +(full-scale −1LSB).

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Bipolar setting up points

Output range, ±FS	LSB	−FS	+FS - 1LSB
±2.50V	19.5mV	−2.5000V	+2.4805V
±5V	39.1mV	−5.0000V	+4.9609V
±10V	78.1mV	−10.0000V	+9.9219V

$1LSB = \frac{2FS}{256}$

Bipolar logic coding

Input code (Offset binary)	Analogue output (Nominal value)
11111111	+(FS - 1LSB)
11111110	+(FS - 2LSB)
11000000	+0.5FS
10000001	+1LSB
10000000	0
01111111	−1LSB
01000000	−0.5FS
00000001	−(FS - 1LSB)
00000000	−FS