


PLESSEY
Semiconductors

T-74-05-01

ZN459, ZN459CP

ULTRA LOW NOISE WIDEBAND PREAMPLIFIER

FEATURES

- High Controlled Gain : 60 dB $\pm$ 1 dB typical
- Low Noise : 40 Ω Equivalent Noise Resistance, or 800 pV/ $\sqrt{\text{Hz}}$
- Wide Bandwidth : 15 MHz typical
- Low Supply Current : <3 mA from 5V

DESCRIPTION

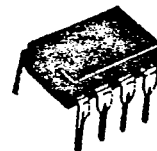
A versatile high grade a.c. pre-amplifier designed for applications requiring ultra low noise such as infra-red imaging and low noise wide band amplifiers e.g. microphone, acoustic emission, transducer bridge amplifier. The matching of open loop gain coupled with small physical size make the ZN459 series ideal for multichannel amplification.

ZN459

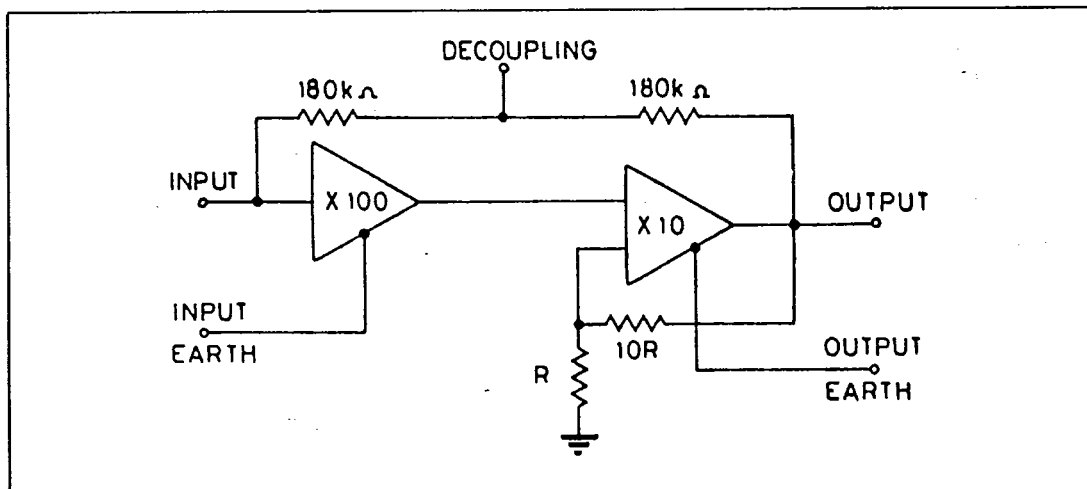


CM6

ZN459CP



DP8



ZN459 OUTLINE CIRCUIT

ABSOLUTE MAXIMUM RATINGS

PLESSEY SEMICONDUCTORS

Supply Voltage 6.0 Volts

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Operating Temperature Range:

for ZN459 -55 to +125°C

for ZN459CP 0 to +70 °C

Storage Temperature Range -55 to +125°C

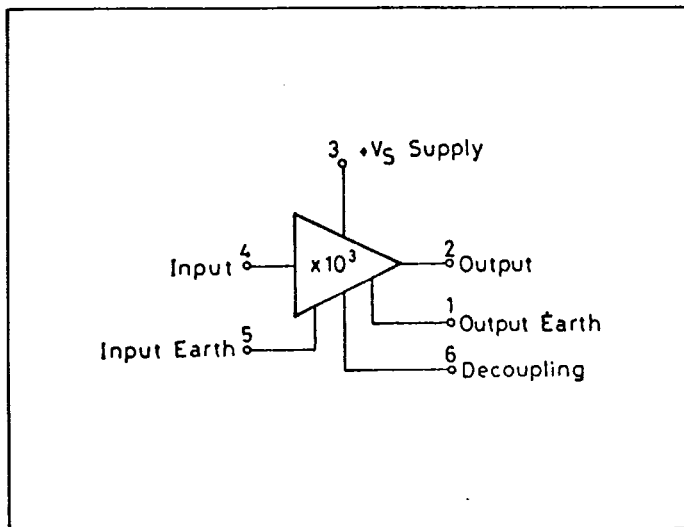
CHARACTERISTICS (at $V_{CC} = 5V$, $T_{amb} = 25^\circ C$).

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Current	2.0	2.5	3.0	mA	
Voltage Gain	59	60	61	dB	10 kHz
TC of Voltage Gain	—	-0.2	—	%/°C	
V_{CC} Coefficient of Voltage Gain	—	25	—	%/V	
Cut-off Frequency	—	15	—	MHz	3 dB down
Input Resistance	3.5	7	—	k Ω	10 kHz
Input Capacitance	—	80	—	pF	Note 1
Noise Resistance	—	40	—	Ω	$R_S = 0$
White Noise Voltage	—	800	1100	pV/ $\sqrt{Hz}$	$R_S = 0$
L.F. Spot Noise	—	3	—	nV/ $\sqrt{Hz}$	$R_S = 0$, $f = 25$ Hz
White Noise Current	—	1	—	pA/ $\sqrt{Hz}$	
Output Level	1.5	2.0	2.5	V	
Supply Voltage Coefficient of Output Level	—	0.34	—	V/V	
Output Current Limit	0.6	0.8	1.1	mA	Sink current
Total Harmonic Distortion	—	0.15	—	%	1 V_{pp} at 10 kHz
Output Resistance	—	75	—	Ω	10 kHz
Supply Rejection Ratio	—	42.5	—	dB	
Delay Time	—	20	—	ns	Small signal
Delay Time	—	40	—	ns	100 mV rms input
Positive Input Overdrive	—	10	—	mA	
Negative Input Overdrive	—	-5	—	V	

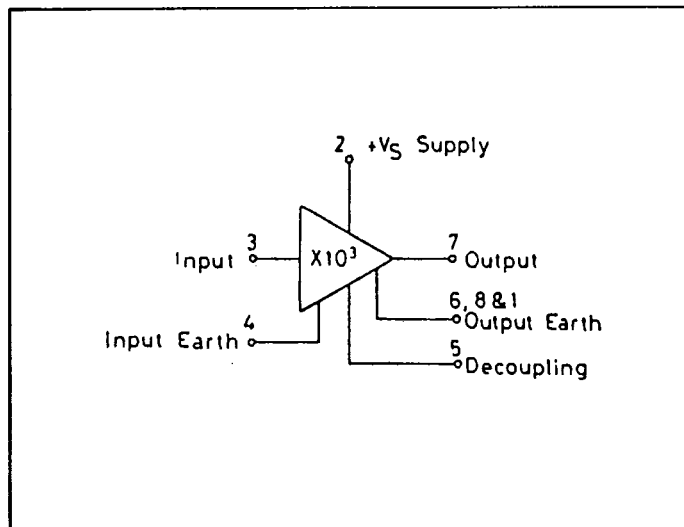
Note 1: In P.C.B. The Input Capacitance may be reduced to 25pF by screening between output and input.

PLESSEY SEMICONDUCTORS

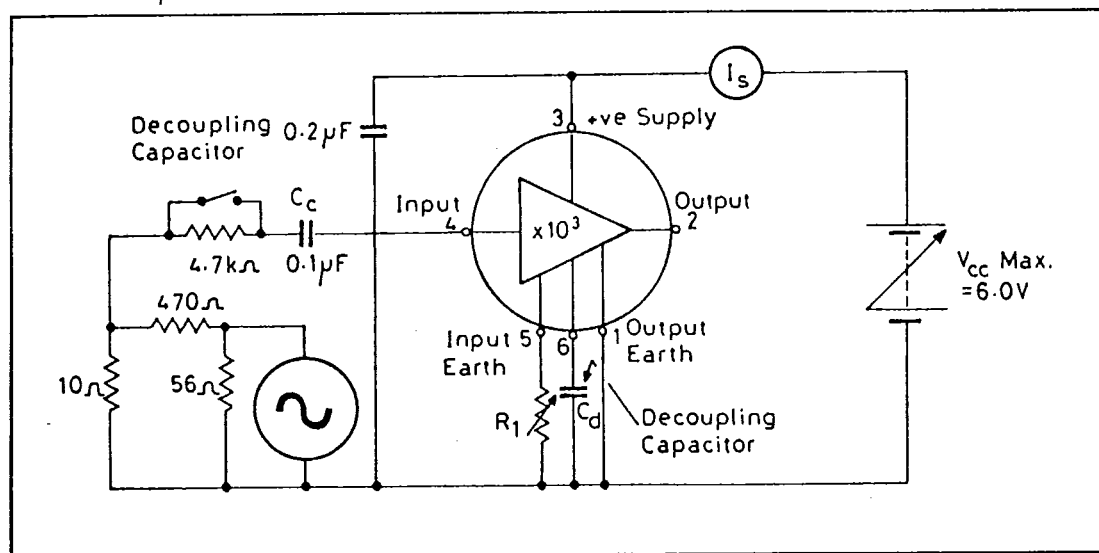
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PINNING CONFIGURATION - ZN459



PINNING CONFIGURATION - ZN459CP

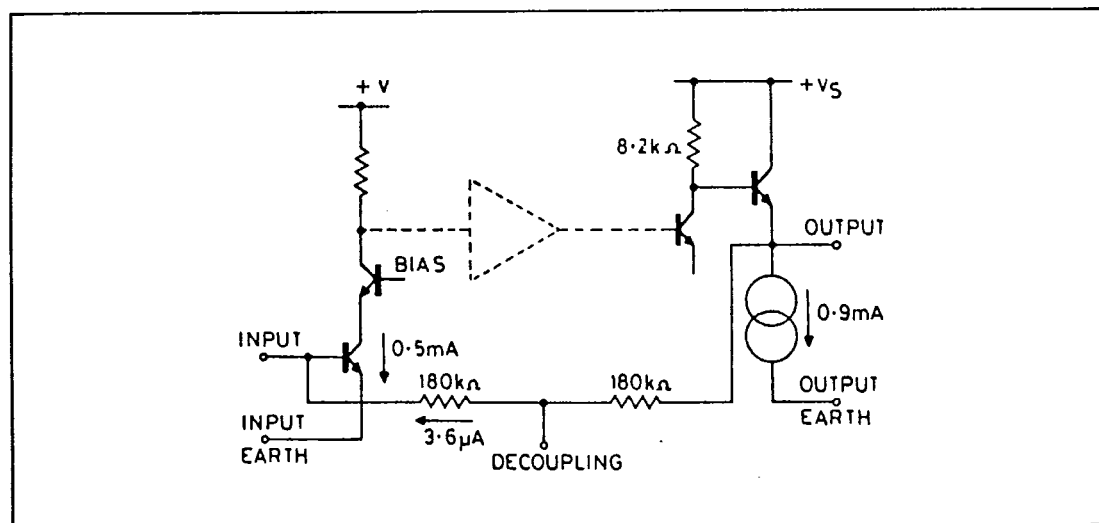


The input impedance may be increased at the expense of noise by including R_1 to vary the gain ($R_1 = 0$, gain = 10^3 ; $R_1 = 470\Omega$, gain = 10^2).

C_d is required to decouple the internal feedback loop and in order to obtain a flat frequency response make $C_d \geq C_c$.

The earth lead of the supply decoupling capacitor should be as close as possible to that of R_1 .

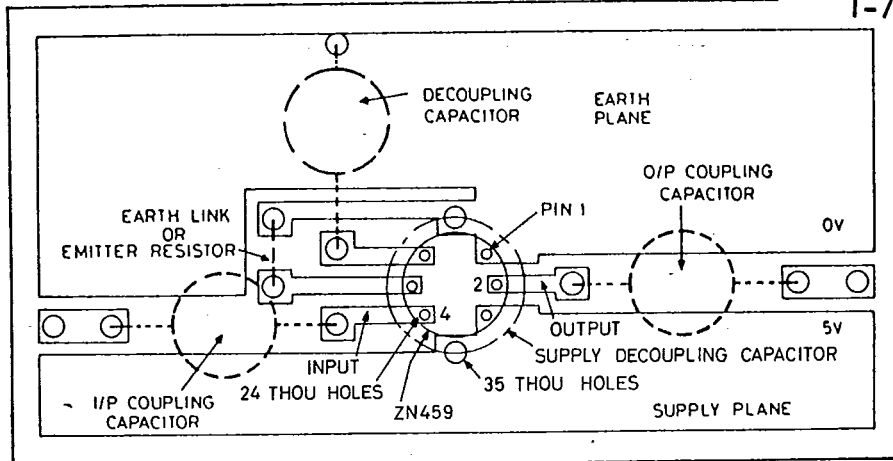
For optimum Common Mode Rejection connect a twisted pair between source and pins 4 and 5 of the device, and complete the earth return from source and ground.



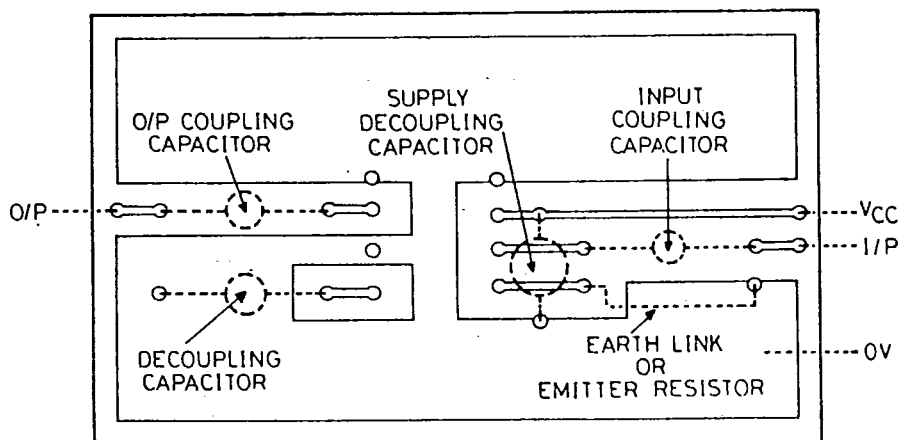
ZN459 INPUT AND OUTPUT CIRCUIT

PCB LAYOUT (ZN459) PLESSEY SEMICONDUCTORS

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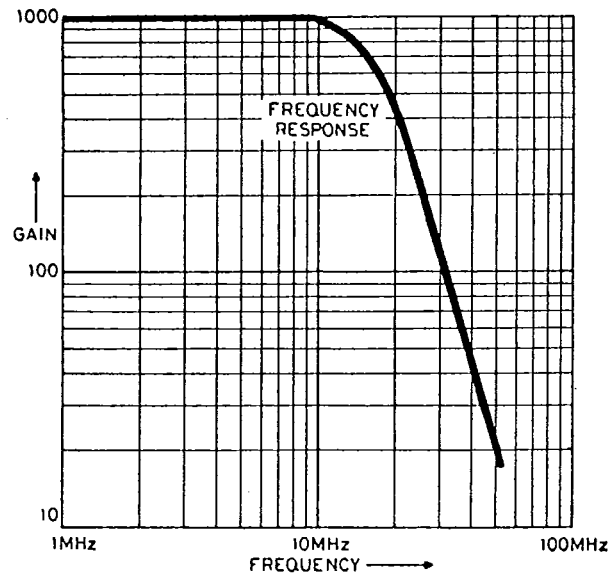
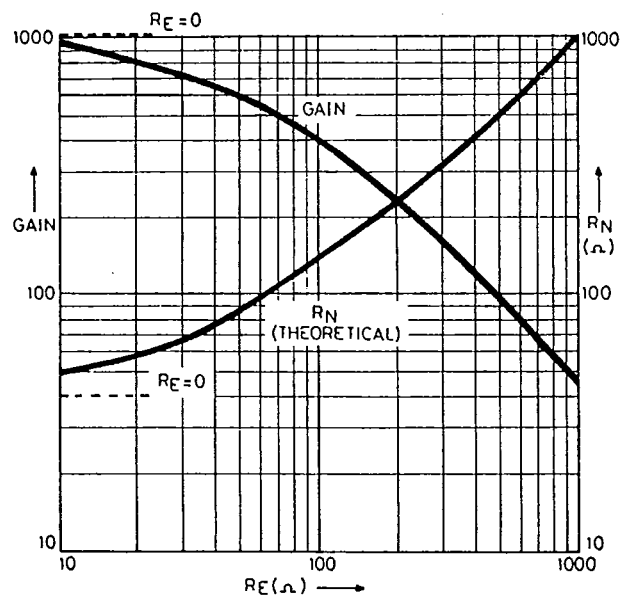
PCB LAYOUT (ZN459CP)

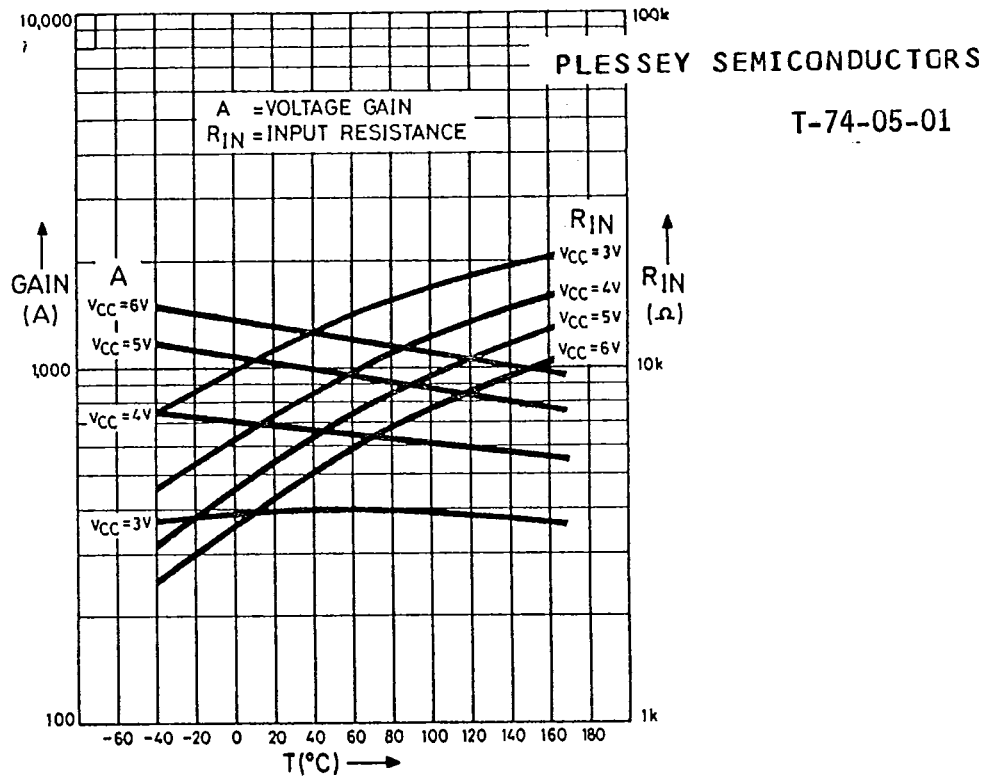


TYPICAL CHARACTERISTICS

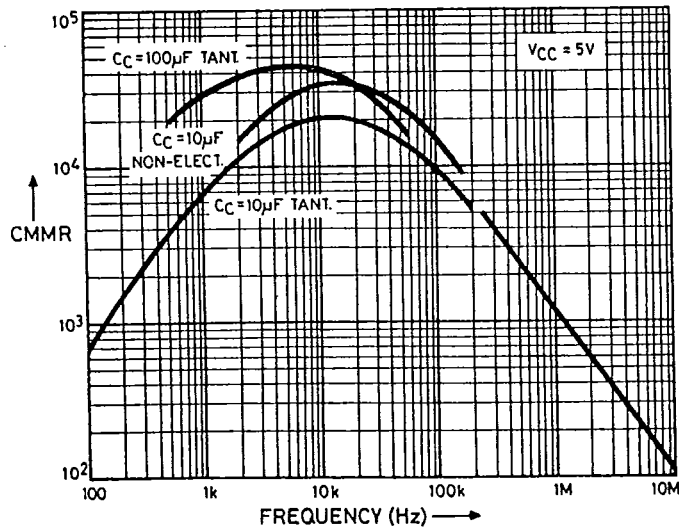
PLESSEY SEMICONDUCTORS

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GAIN V_S FREQUENCYGAIN AND NOISE RESISTANCE V_S EMITTER RESISTANCE



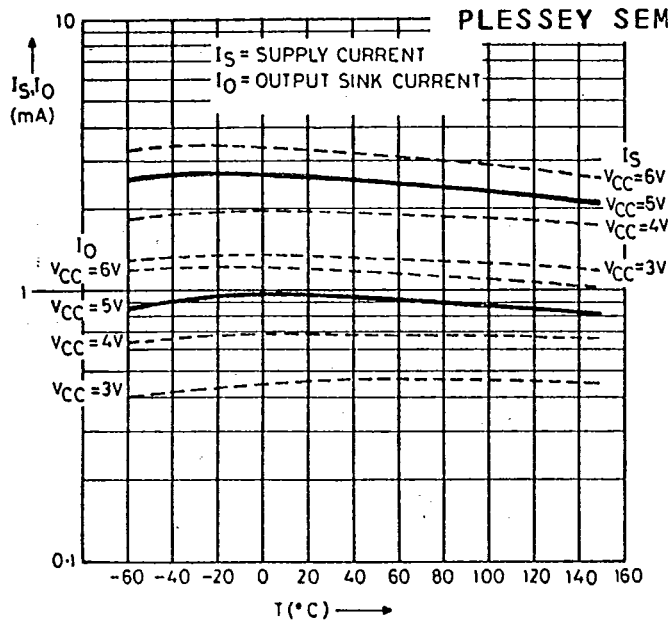
GAIN AND INPUT IMPEDANCE



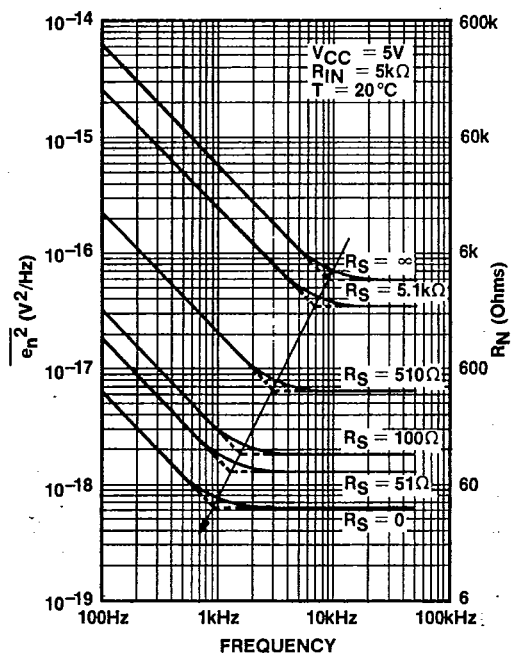
COMMON MODE REJECTION Vs FREQUENCY
(Measured between input earth and output earth)

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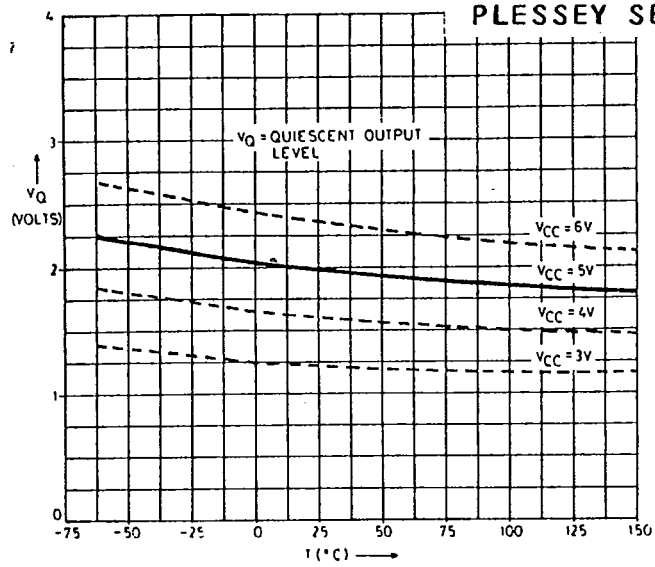
SUPPLY CURRENT AND OUTPUT SINK CURRENT



NOISE VOLTAGE

PLESSEY SEMICONDUCTORS

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QUIESCENT OUTPUT LEVEL