PLESSEY Semiconductors

ADVANCED PRODUCT INFORMATION

T-51-09-10

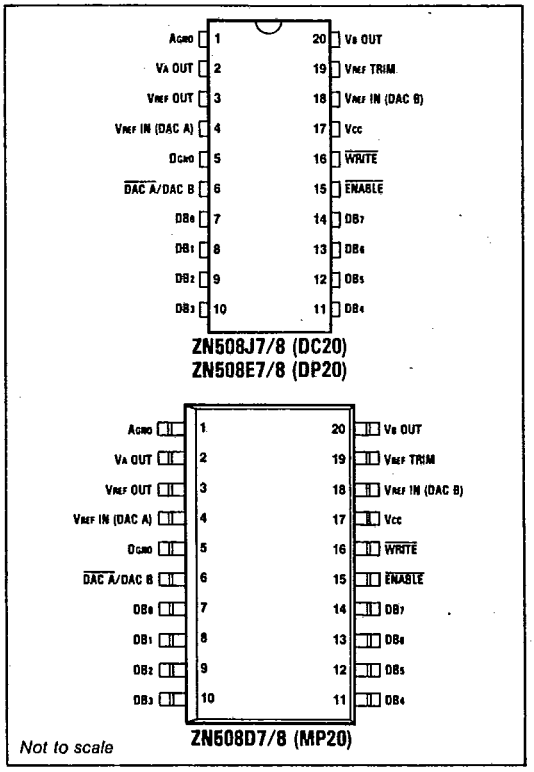
# ZN508

## DUAL 8-BIT MICROPROCESSOR COMPATIBLE D-A CONVERTER

The ZN508 is a monolithic dual 8-bit DAC designed to be easily interfaced to microprocessors. Integrated on-chip are two 8-bit DAC's, a 2.5V trimmable bandgap reference, separate $V_{REF}$ inputs and data latches for each DAC. The on-chip reference not only can be used to drive the two DAC's but can be also used as a system reference. A consequence of the two DAC's being fabricated on the same chip is excellent, inherent, DAC to DAC matching.

### FEATURES

- 800ns Voltge Settling Time
- 2.5V Trimmable Bandgap Reference
- Monotonic over Full Temperature Range
- Single +5V Supply
- Excellent DAC to DAC Matching
- Separate $V_{REF}$ IN for each DAC
- Commerical and Military Temperature Ranges




*Pin connections - top view*

### ORDERING INFORMATION

| Device type | Linearity error (LSB) | Operating temperature | Package |
|---|---|---|---|
| ZN508E7 | ±1 | -40°C to +85°C | DP20 |
| ZN508E8 | ±½ | -40°C to +85°C | DP20 |
| ZN508D7 | ±1 | -40°C to +85°C | MP20 |
| ZN508D8 | ±½ | -40°C to +85°C | MP20 |
| ZN508J7 | ±1 | -55°C to +125°C | DC20 |
| ZN508J8 | ±½ | -55°C to +125°C | DC20 |

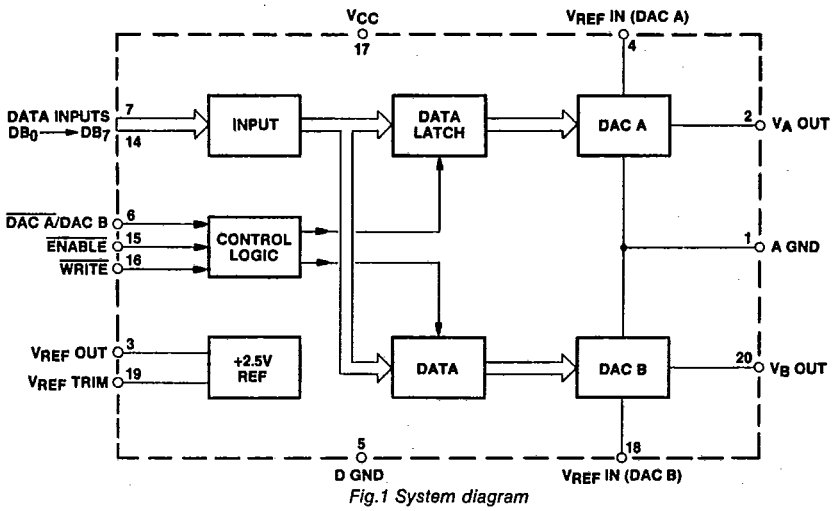



*Fig.1 System diagram*

## ABSOLUTE MAXIMUM RATINGS

Supply voltage $V_{CC}$ +7V
Max. voltage, logic and $V_{REF}$ input +Vcc
Operating temperture range
ZN508E and ZN508D -40°C to +85°C
ZN508J -55°C to 125°C
Storage temperature range -55°C to 125°C
Analog ground to digital ground ±200mV

T-51-09-10

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 25°C

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **ZN508-8** | | | | | |
| Linearity error | | | ±0.5 | LSB | |
| Differential linearity error | | | ±0.75 | LSB | |
| **ZN508-7** | | | | | |
| Linearity error | | | ±1.0 | LSB | |
| Differential linearity error | | | ±1.0 | LSB | |
| **All types** | | | | | |
| Linearity error TC | | ±3 | | ppm/°C | |
| Differential non-linearity TC | | ±6 | | ppm/°C | |
| Offset voltage ZN508E | | 2 | 5 | mV | All bits OFF |
| ZN508D | | 2 | 5 | mV | All bits OFF |
| ZN508J | | 2 | 5 | mV | All bits OFF |
| Offset voltage TC | | ±3 | | ppm/°C | |
| Full scale output | 2.545 | 2.550 | 2.555 | V | External reference $V_{REF}$ IN = 2.560V, all bits ON |
| Full scale output TC | | 2 | | ppm/°C | |
| Analog output resistance | | 4 | | kΩ | |
| External reference voltage | 0 | | 3.0 | V | |
| Settling time to 0.5 LSB | | 800 | | ns | 1 LSB major transition (Note 1) |
| | | 1.25 | | µs | All bits ON to OFF or OFF to ON (Note 1) |
| Supply voltage ($V_{CC}$) | 4.5 | 5.0 | 5.5 | V | |
| Supply current | | 36 | | mA | |
| Power consumption | | 180 | | mW | |
| DC supply rejection | | -57 | | dB | $\Delta V_{CC}$ = 250µV p-p f ≤ 50kHz |
| Digital to analog glitch impulse | | | | nV-s | 00000000 11111111 |
| Channel to channel isolation | | | | | |
| $V_{REF\,A}$ to Out B | | -82 | | dB | f ≤ 50kHz |
| $V_{REF\,B}$ to Out A | | -82 | | dB | |
| **Internal voltage reference** | | | | | |
| Output voltage | | 2.5 | | V | |
| Slope impedance | | 1 | | Ω | |
| $V_{REF}$ OUT TC | | 50 | | ppm/°C | |
| Reference current | 1 | | 15 | mA | |
| **Logic** | | | | | |
| (over specified operating temperature range) | | | | | |
| High level input voltage $V_{IH}$ | 2.0 | | | V | |
| Low level input voltage $V_{IL}$ | | | 0.8 | V | |
| High level input current $I_{IH}$ | | | 20 | µA | $V_{IN}$ = 2.4, Vcc = 5.5V |
| | | | 320 | µA | $V_{IN}$ = 5.5, Vcc = 5.5V |
| Low level input current $I_{IL}$ | | | -310 | µA | $V_{IN}$ = 0.4V, Vcc = 5.5V |

T-51-09-10

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Switching characteristics** | | | | | |
| Chip select to write set up time $t_{CS}$ | 150 | | | ns | |
| Chip select to write hold time, $T_{CH}$ | 10 | | | ns | |
| DAC select to write set up time $t_{AS}$ | 150 | | | ns | |
| DAC select to write hold time $t_{AH}$ | 10 | | | ns | |
| Data valid to write set up time $t_{DS}$ | 100 | | | ns | |
| Data valid to write hold time $t_{DH}$ | 50 | | | ns | |
| Write pulse width $t_{WR}$ | 150 | | | ns | |

NOTE
1. $R_L$ = 10 Megohms $C_L$ = 10pF.

## D-A CONVERTER

The converters are of the voltage switching type and use an R-2R ladder network as shown in Fig.2. Each 2R element is connected to 0V or $V_{REF}$ IN by transistor voltage switches specially designed for low offset voltage (<1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

Analog output $= \frac{n}{256} (V_{REF} IN - V_{OS}) + V_{OS}$

where n is the digital input to the D-A from the data latch.

$V_{OS}$ is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of $V_{OS}$ is typically 1mV. This offset will normally be removed by the setting up procedure (see Operating Notes) and because the offset temperature coefficient is low (±6μV/°C) the effect on accuracy is negligible.

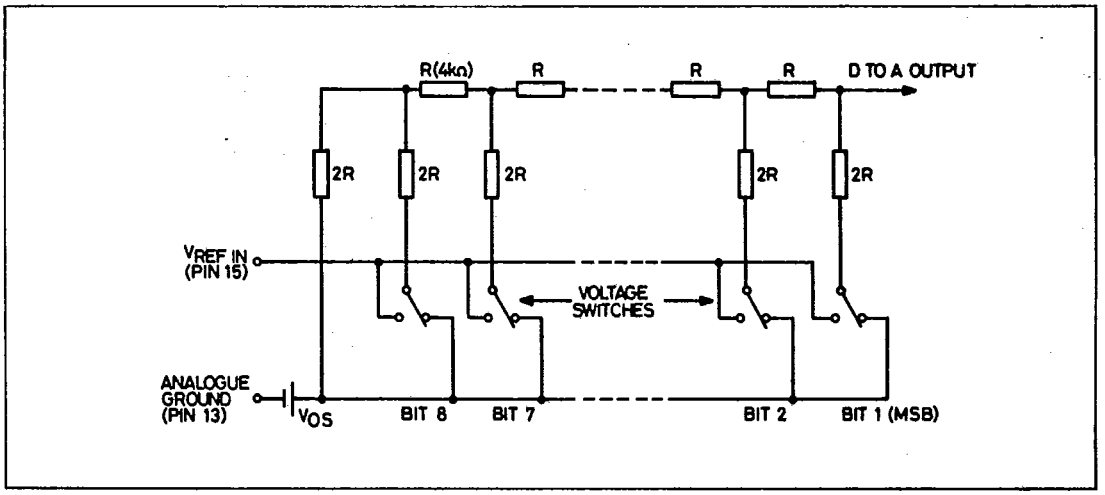



*Fig.2 The R-2R ladder network*

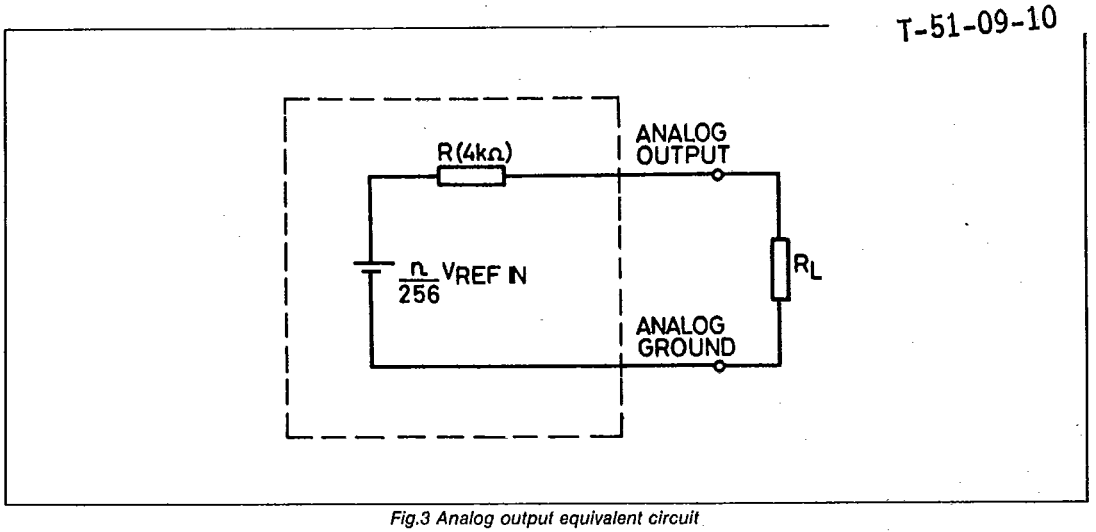



*Fig.3 Analog output equivalent circuit*

Fig.3 shows an equivalent circuit of the outputs (ignoring Vos). The output resistance R has a temperature coefficient of +0.2% per °C.
The gain drift due to this is $\frac{0.2R}{R + R_L}$ % per °C

RL should be chosen to be as large as possible to make the gain drift small. As an example if $R_L = 400k\Omega$ then the gain drift due to the TC of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN508 outputs can be buffered by amplifiers (see Operating Notes).

## REFERENCE

### 1. Internal Reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig.3). A resistor ($R_{REF}$), should be connected between +Vcc (pin 11) and pin 15. The recommended value of 1.5k will supply a nominal reference current of (5-2.5)/1500 = 1.7mA.
The reference voltage can be trimmed by ±5% with a 10k potentiometer (as shown in Fig.5).

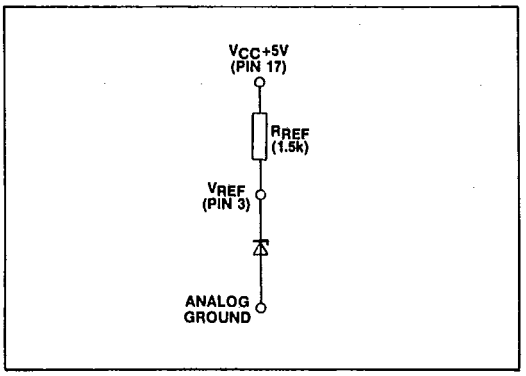



*Fig.4 Internal voltage reference*

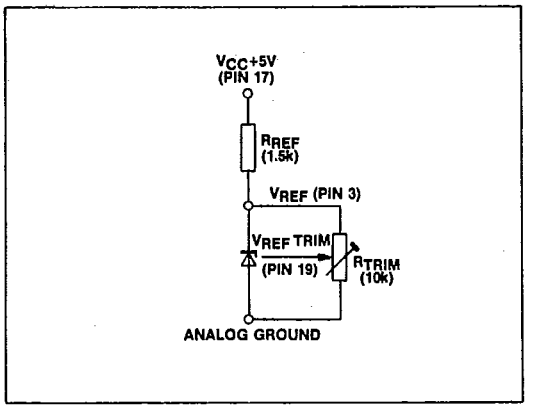



*Fig.5 Trimming circuit for the voltage reference*

### 2. External Reference

If required an external reference voltage may be connected to $V_{REF}$ IN. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

$V_{REF}$ IN can be varied from 0 to +3V for ratiometric operation. The ZN508 is guaranteed monotonic for $V_{REF}$ IN above 2V.

## LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. Both DAC A and DAC B share an internal data bus and an 8-bit input port. The DAC to be loaded with new data is chosen by $\overline{\text{DAC A}}$/DAC B select pin; DAC A when the input is low and DAC B when the input is high. When $\overline{\text{ENABLE}}$ and $\overline{\text{WRITE}}$ are both low the DAC selected is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to the data presented to the input port. The data is then latched when either $\overline{\text{ENABLE}}$ or $\overline{\text{WRITE}}$ are taken high.

| $\overline{\text{DAC A}}$/DAC B | $\overline{\text{CS}}$ | $\overline{\text{WR}}$ | DAC A | DAC B |
|---|---|---|---|---|
| L | L | L | WRITE | HOLD |
| H | L | L | HOLD | WRITE |
| X | H | X | HOLD | HOLD |
| X | X | H | HOLD | HOLD |

*Table 1 Logic truth table*

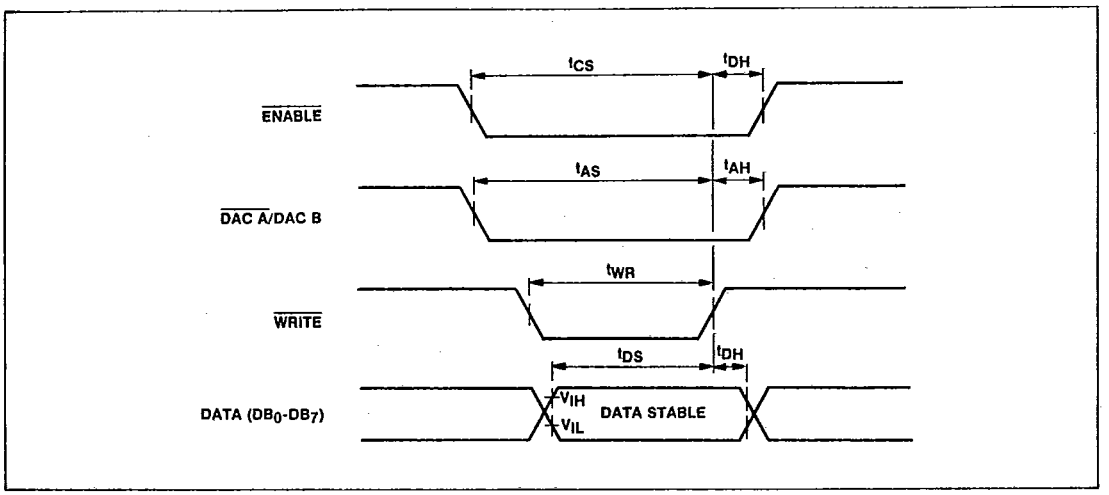



*Fig.6 Logic timing diagram*

## OPERATING NOTES

In some applications the standard 0 to $V_{REF}$ IN output voltage range and drive capability are not suitable, and other output ranges, both unipolar and bipolar are required.

To maintain flexibility two types of operational amplifier are illustrated; the industry standard 741 and a low cost pin-compatible alternative with a JFET input, the LF351. The LF351 features a high slew rate of 13V/$\mu$s, which gives a faster potential settling time than the 741. To keep drift to a minimum when using the 741, the external range setting resistors are calculated to match them to the 4kΩ ladder output impedance. This is not a consideration with the LF351, as the input offset current change with temperature is negligible for the impedances concerned. The resistor values for the LF351 were chosen to keep the output ringing to a minimum; a problem sometimes encountered with high slew rate op-amps. It is only the relative and not the absolute values of these resistors which set the range, and therefore can be changed as long as their ratios remain the same.

### Unipolar Operation

The general scheme for unipolar operation is shown in Fig.6 and is suitable for amplifiers with input bias currents less than 1.5$\mu$A.

The resulting full scale range is given by

$$V_{OUT}\,FS = 1 + \frac{R1}{R2}\,(V_{REF}\,IN - 1\,LSB)$$

$$= G\,(V_{REF}\,IN) - 1\,LSB)$$

The impedance at the inverting input is R1/R2 and for low drift with temperature (741 only), this parallel combination should be equal to the ladder resistance (4kΩ).

The required nominal values of R1 and R2 are therefore given by R1 = 4GkΩ and R2 = 4G/(G-1)kΩ.

Using these relationships a table of nominal resistance values for R1 and R2 can be constructed for $V_{REF}$ IN = 2.5V (Table 2). For gain setting R1 is adjusted about its nominal value. Practical circuit realisations for +5V and +10V output ranges are given in Figs. 8 and 9.

| Output range | G | R1 | R2 |
|---|---|---|---|
| +5V | 2 | 8kΩ | 8kΩ |
| +10V | 4 | 16kΩ | 5.33kΩ |

*Table 2 Nominal values for R1 and R2*

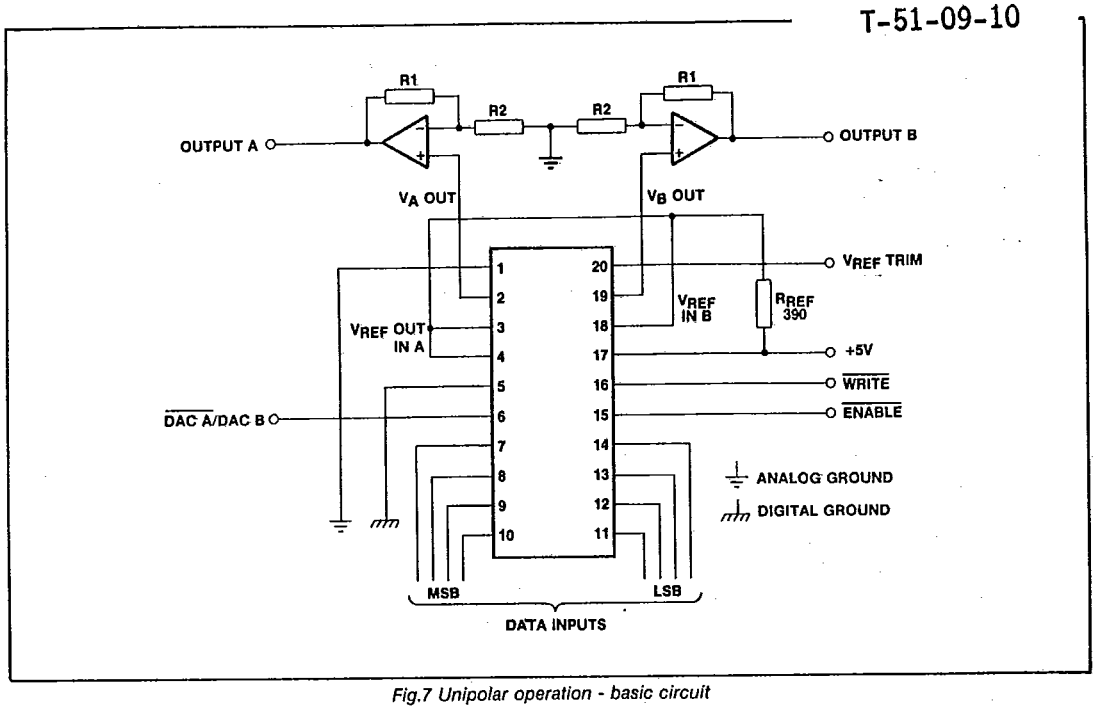



*Fig.7 Unipolar operation - basic circuit*

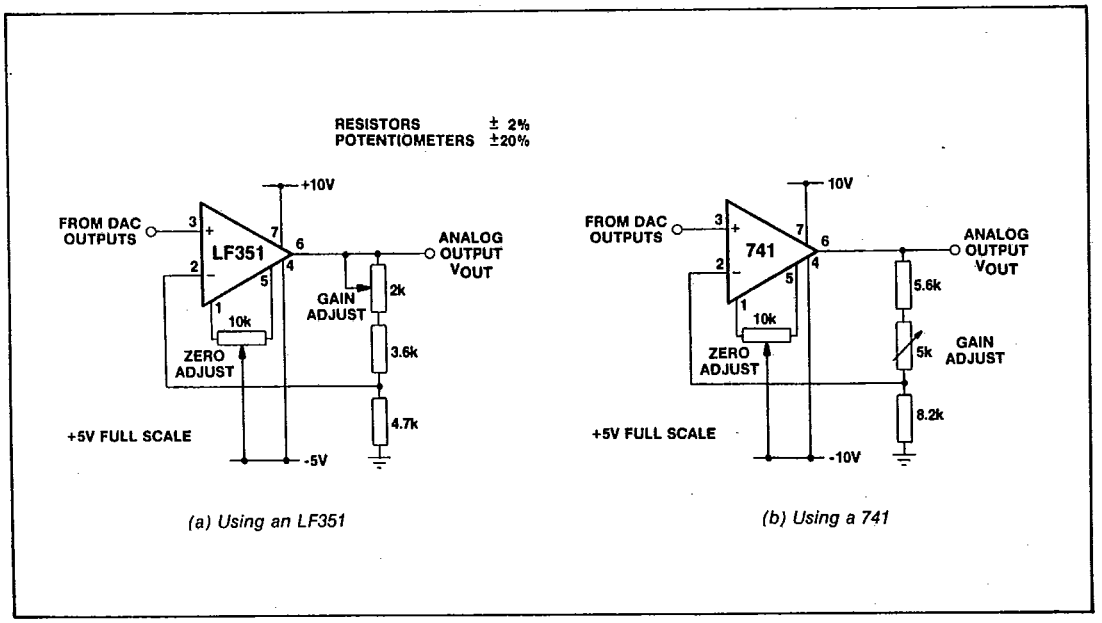



*Fig.8 +5V full scale unipolar operation - component values*

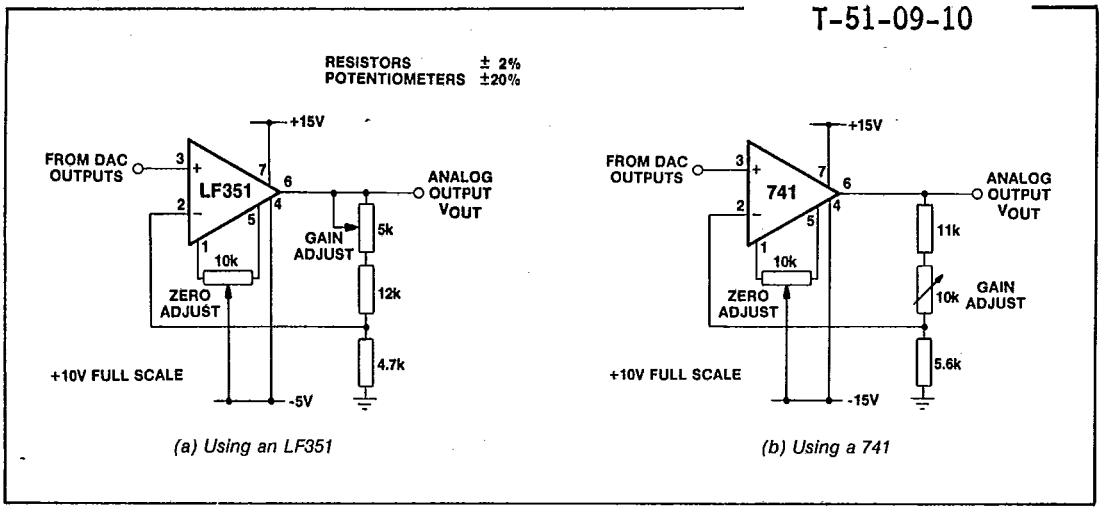



*Fig.9 +10V full scale unipolar operation - component values*

### Unipolar Adjustment Procedure

1. Set all bits to OFF (low) with $\overline{\text{ENABLE}}$ low and adjust zero until $V_{OUT}$ = 0.0000V.

2. Set all bit ON (high) and adjust gain until $V_{OUT}$ = FS - 1 LSB.

| Output range, +FS | LSB | FS - 1 LSB |
|---|---|---|
| +5V | 19.5mV | 4.9805V |
| +10V | 39.1mV | 9.9609V |

$1\ \text{LSB} = \frac{\text{FS}}{256}$

*Table 3 Unipolar setting up points*

| Input code (Binary) | Analog output (nominal value) |
|---|---|
| 11111111 | FS - 1 LSB |
| 11111110 | FS - 2 LSB |
| 11000000 | ¾ FS |
| 10000001 | ½ FS + 1 LSB |
| 10000000 | ½ FS |
| 01111111 | ½ FS - 1 LSB |
| 01000000 | ¼ FS |
| 00000001 | 1 LSB |
| 00000000 | 0 |

*Table 4 Unipolar logic coding*

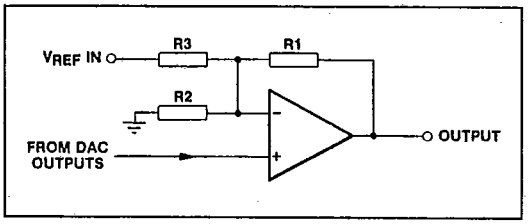



*Fig.10 Bipolar operation*

### Bipolar Operation

For bipolar operation the output from the ZN508 is offset by half full scale by connecting a resistor R3 between $V_{REF}$ IN and the inverting input of the buffer amplifier (Fig.10).

When the digital input to the ZN508 is zero the analog output is zero and the amplifier output should be - full scale. An input of all ones to the D-A will give a ZN508 output of $V_{REF}$ IN - 1 LSB and an amplifier output of + full scale. When using the 741, the parallel combination of R1, R2 and R3 should match the 4kΩ ladder resistance.

The nominal values of R1, R2 and R3 which meet these conditions are given by

R1 = 8GkΩ, R2 = 8G/(G-1)kΩ and R3 = 8kΩ,

where the resultant output range is ±G $V_{REF}$ IN.

A binary output range of ±$V_{REF}$ IN (which corresponds to the basic unipolar range 0 to $V_{REF}$ IN) is obtained if R1 = R3 = 8kΩ and R2 = ∞.

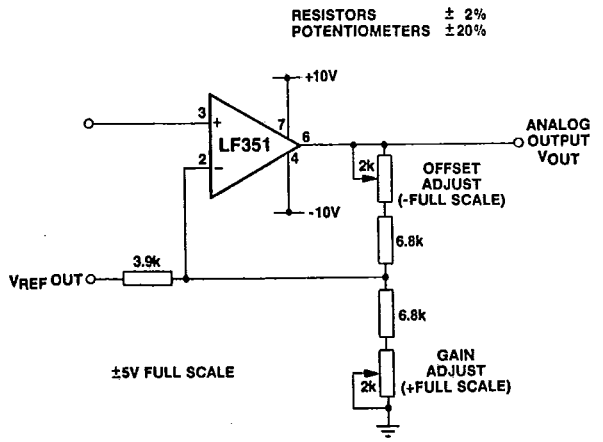
Assuming that $V_{REF}$ IN = 2.5V the nominal values of resistors for ±5V and ±10V output ranges are given in Table 5.

| Output range | G | R1 | R2 | R3 |
|---|---|---|---|---|
| +5V | 2 | 16kΩ | 16kΩ | 8kΩ |
| ±10V | 4 | 32kΩ | 10.66kΩ | 8kΩ |

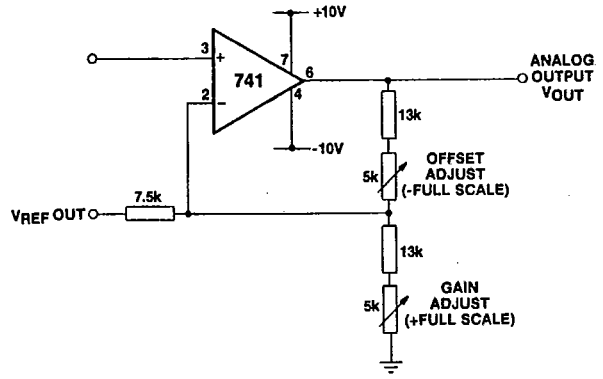
*Table 5*

Minus full scale (offset) is set by adjusting R1 about its nominal value relative to R3. Plus full scale (gain) is set by adjusting R2 relative to R1.

Practical circuit realisations are given in Figs. 11 and 12. Note that in the ±5V case (741 only), R3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to give a more symmetrical range of adjustment using standard potentiometers.




*(a) Using an LF351*




*(b) Using a 741*

*Fig. 11 ±5V full scale bipolar operation - component values*

T-51-09-10

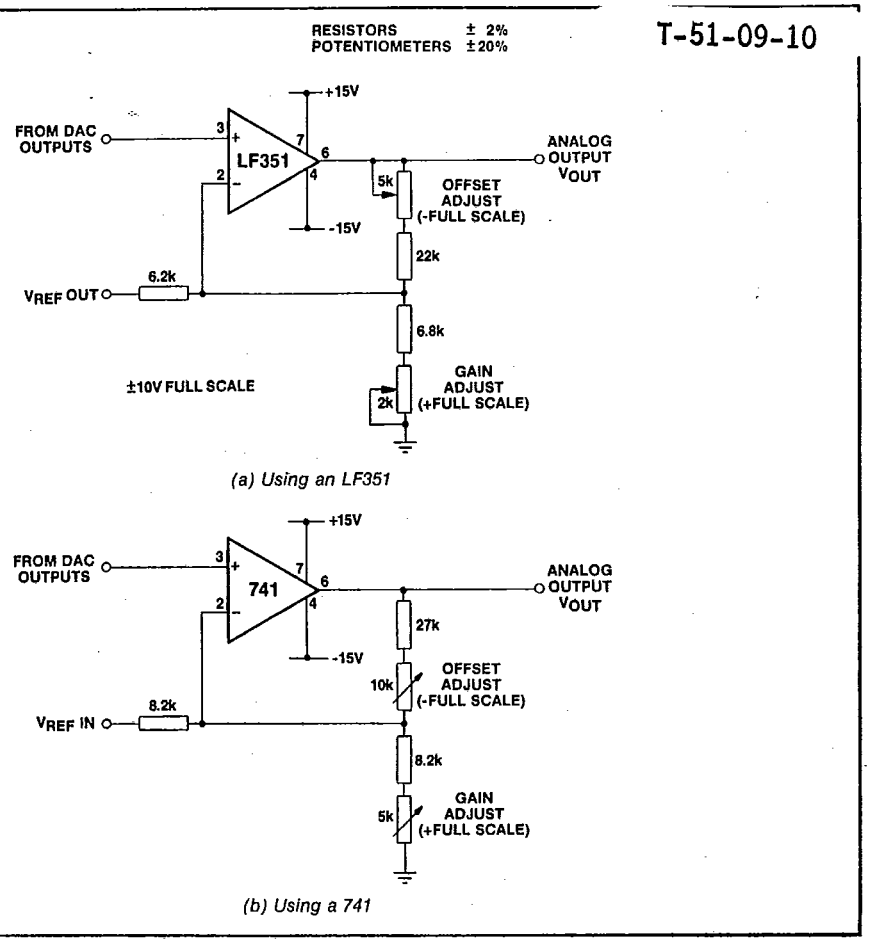



*Fig.12 ±10V full scale bipolar operation - component values*

### Bipolar Adjustment Procedure

1. Set all bits to OFF (low) with $\overline{\text{ENABLE}}$ low and adjust offset until the amplifier output reads - full scale.

2. Set all bits ON (high) and adjust gain until the amplifier output reads + (full scale - 1 LSB).

| Input range, ±FS | LSB | -FS | +(FS - 1 LSB) |
|---|---|---|---|
| ±5V | 39.1mV | -5.0000V | +4.9609V |
| ±10V | 78.1mV | -10.0000V | +9.9219V |

$$1\ \text{LSB} = \frac{2FS}{256}$$

*Table 6 Bipolar setting up points*

| Input code (offset binary) | Analog output (nominal value) |
|---|---|
| 11111111 | +(FS - 1 LSB) |
| 11111110 | +(FS - 2 LSB) |
| 11000000 | +½ FS |
| 10000001 | +1 LSB |
| 10000000 | 0 |
| 01111111 | -1 LSB |
| 01000000 | -½ FS |
| 00000001 | -(FS - 1 LSB) |
| 00000000 | -FS |

*Table 7 Bipolar logic coding*