2354-1.0

ZN682/3, ZN684/5, ZN688/9

2/4/8-CHANNEL 8-BIT MICROPROCESSOR COMPATIBLE ADCs

(ZN688/9 supersede ZN538/9 designs)

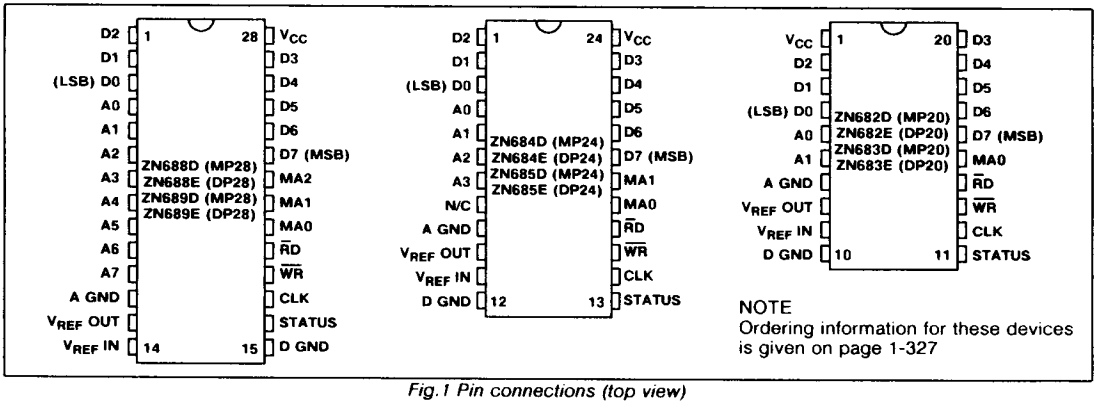
These integrated circuits are a set of 2, 4 and 8-channel, 8-bit analog to digital converters, designed to interface easily to most popular microprocessors.

Each consists of an 8-bit successive approximation A-D converter, a 2, 4 or 8-channel multiplexer, clock generator, 2.5V bandgap reference, control logic and double buffered latches with 3-state outputs. The address bus ($MA_0 \rightarrow MA_n$) is used to select the channel on which the next conversion is to be performed.

The devices are offered in two linearity options: ±0.5LSB (ZN682/4/8) or ±1.0 LSB (ZN683/5/9). All operate over the temperature range -40°C to +85°C from a single +5V supply and are available in a choice of surface mount or plastic DIL packages

FEATURES

- Choice of Linearity: ±0.5LSB or ±1LSB
- 8 µs Conversion Time
- Choice of 2,4 or 8 Analog Inputs
- Continuous Conversion on Specified Channel
- Sub-100ns Access Time
- Operates from Single +5V Supply
- On-Chip Bandgap Reference
- On-Chip Overdrivable Clock Oscillator
- Microprocessor/TTL/CMOS Compatible
- ROM Type Operation



NOTE
Ordering information for these devices is given on page 1-327

Fig.1 Pin connections (top view)

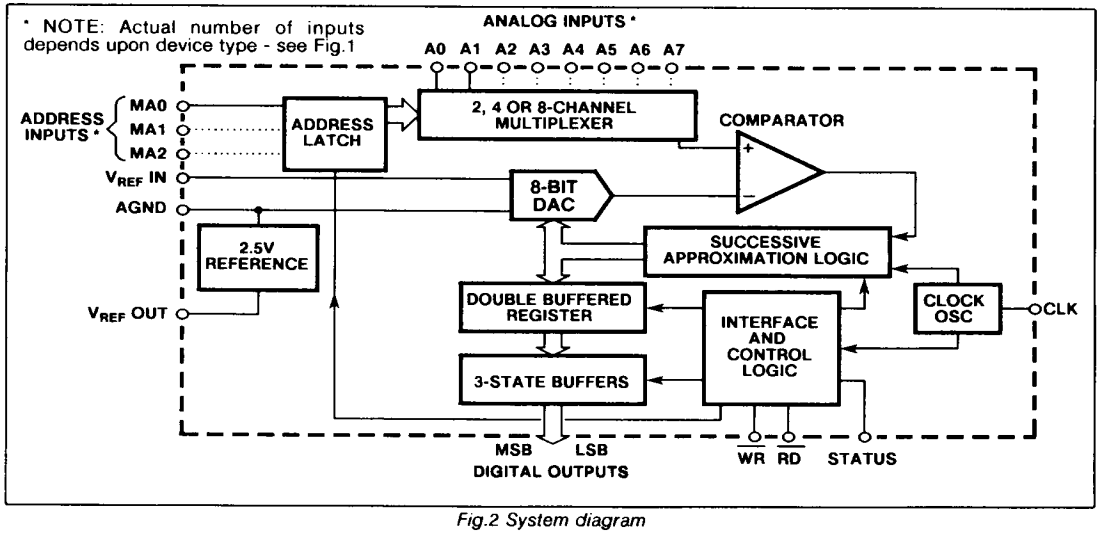


Fig.2 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
Voltage, logic and V_{REF} inputs	V_{CC}
Operating temperature range	-40°C to +85°C
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 5V, T_{amb} = +25°C, f_{CLK} = 1.0MHz

Characteristic	Value					Units	Conditions
	T_{amb} = +25°C			Over specified temp. range			
	Min.	Typ.	Max.	Min.	Max.		
ZN688/4/2							
Linearity error			±0.5		±0.5	LSB	
Differential linearity error			±0.75		±0.75	LSB	
ZN689/5/3							
Linearity error			±1		±1	LSB	
Differential linearity error			±1		±1	LSB	
ALL TYPES							
Zero transition (00000000 → 00000001)		13				mV	External reference = 2.56V
Full-scale transition (11111110 → 11111111)		2.540				V	
Linearity temperature coefficient			±3 typ			ppm/°C	External reference = 2.56V
Differential linearity temperature coefficient			±6 typ			ppm/°C	
Gain temperature coefficient			±10 typ			ppm/°C	
Offset temperature coefficient			±7 typ			ppm/°C	
Resolution	8					bits	
Conversion time	8					µs	Per channel
Supply voltage	4.5	5.0	5.5	4.5	5.5	V	
Supply current		40	55			mA	Outputs in high impedance state
Power consumption		200	275			mW	
Reference input range	2.0	2.0	3.0			V	
MULTIPLEXED INPUTS							
Input current		-106				µA	V_{IN} = 0V, V_{REF} = 2.56V
Input resistance		24				kΩ	
Input voltage (Max.)	-0.5		+3.5	-0.5	+3.5	V	
Input voltage (operational)	0		V_{REF}	0	V_{REF}	V	

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Value					Units	Conditions
	T_{amb} = +25°C			Over specified temp. range			
	Min.	Typ.	Max.	Min.	Max.		
INTERNAL VOLTAGE REFERENCE							
Output voltage		2.58				V	
Output voltage tolerance			±3			%	
Slope impedance		0.5	2			Ω	
Reference current	0.75		5.2	0.75	5.2	mA	
Output voltage temperature coefficient		70				ppm/°C	
CLOCK							
Maximum on-chip clock frequency		1.0				MHz	C_{CK} = 220pF typ. (Fig.7)
Clock frequency temperature coefficient		-0.125				%/°C	
Maximum external clock frequency	1.0			1.0		MHz	
Clock pulse width	250					ns	
High level I/P voltage V_{IH}	3.5			3.5		V	
Low level I/P voltage V_{IL}			0.8		0.8	V	
High level I/P current I_{IH}		750				μA	V_{CC} = +5.5V, V_{IN} = +3.5V
Low level I/P current I_{IL}		-880				μA	V_{CC} = +5.5V, V_{IN} = 0.8V
Supply rejection		3.0				%/V	
LOGIC $\overline{RD}$ INPUT							
High level I/P voltage V_{IH}	2.4			2.4		V	
Low level I/P voltage V_{IL}			0.8		0.8	V	
High level I/P current I_{IH}		350				μA	V_{CC} = +5.5V, V_{IN} = +5.5V
		90				μA	V_{CC} = +5.5V, V_{IN} = +2.4V
Low level I/P current I_{IL}		-80				μA	V_{CC} = +5.5V, V_{IN} = +0.4V
LOGIC $\overline{WR}$ INPUT							
High level I/P voltage V_{IH}	2.4			2.4		V	
Low level I/P voltage V_{IL}			0.8		0.8	V	
High level I/P current I_{IH}		160				μA	V_{CC} = +5.5V, V_{IN} = +5.5V
		40				μA	V_{CC} = +5.5V, V_{IN} = +2.4V
Low level I/P current I_{IL}		-25				μA	V_{CC} = +5.5V, V_{IN} = +0.4V

ORDERING INFORMATION

Operating temperature, all variants = –40°C to +85°C

Device type	Number of analog inputs	Linearity error (LSB)	Package
ZN682D	2	±0.5	MP20
ZN682E	2	±0.5	DP20
ZN683D	2	±1.0	MP20
ZN683E	2	±1.0	DP20
ZN684D	4	±0.5	MP24
ZN684E	4	±0.5	DP24
ZN685D	4	±1.0	MP24
ZN685E	4	±1.0	DP24
ZN688D	8	±0.5	MP28
ZN688E	8	±0.5	DP28
ZN689D	8	±1.0	MP28
ZN689E	8	±1.0	DP28

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Value					Units	Conditions
	T_{amb} = +25°C			Over specified temp. range			
	Min.	Typ.	Max.	Min.	Max.		
LOGIC ADDRESS INPUT MA0, MA1, MA2							
High level I/P voltage V_{IH}	2.0			2.0		V	
Low level I/P voltage V_{IL}			0.8		0.8	V	
High level I/P current I_{IH}		170				μA	V_{CC} = +5.5V, V_{IN} = +5.5V
		45				μA	V_{CC} = +5.5V, V_{IN} = +2.4V
Low level I/Pcurrent I_{IL}		-20				μA	V_{CC} = +5.5V, V_{IN} = +0.4V
DATA AND STATUS OUTPUTS							
High level O/P voltage V_{OH}	2.4			2.4		V	$I_{OH\ MAX}$
Low level O/P voltage V_{OL}			0.4		0.4	V	$I_{OL\ MAX}$
High level O/P current I_{OH}			-1.2			mA	
Low level O/Pcurrent I_{OL}			4.0			mA	
Three-state disable O/P leakage current			2.0			μA	V_{OUT} = 0.4V
(Data O/P only)			2.0			μA	V_{OUT} = 2.4V
TIMING INFORMATION							
3-state enable/disable delay times:							
t_{E1}		65	80		95	ns	
t_{E0}		40	55		70	ns	
t_{D1}		50	65		80	ns	
t_{D0}		65	80		95	ns	
Write pulse width	50					ns	
$\overline{WR}$ I/P low to Status O/P high		105	140			ns	
Read pulse width	80					ns	
$\overline{RD}$ I/P high to Status O/P high		90	105		125	ns	
Address set-up time	10					ns	To $\overline{WR}$ high
Address hold time	10					ns	After $\overline{WR}$ high

GENERAL CIRCUIT DESCRIPTION

The ZN682/4/8 accepts 2/4/8 analog inputs and by using a 1/2/3 bit address can be programmed to convert on the required channel. Each channel can be converted to an 8-bit binary word using the successive approximation technique, with the word being loaded into the Result Latch. Pulsing WR low loads the address into the Address Latch and selects the appropriate channel, the Status output goes high to indicate the start of the conversion and the DAC input MSB is set.

The output of the DAC is compared to the unknown analog signal by means of the comparator. If the analog input is larger, the MSB is left set and if not the MSB is cleared. On the second clock pulse the sequence is repeated for the next most significant bit and so on until all eight bits have been compared. On the 8th negative clock edge Status goes low, indicating that the conversion is complete, and the Result Latch is updated.

Taking $\overline{RD}$ low enables the 3-state outputs, allowing the data to be read. Double buffered latches on chip allow the outputs to be enabled at any time, irrespective of the conversion status and so valid data will always be presented to the data bus. This data will be the result of the most recent conversion, therefore $\overline{RD}$ can be completely asynchronous with respect to Status.

CONVERSION TIMING

The device will accept a low-going convert pulse ($\overline{WR}$) which can be completely asynchronous with respect to the clock and will produce valid data 8 or 9 clock pulses later, depending on the relative timing of the clock and $\overline{WR}$. Timing diagrams for a typical conversion sequence are shown in Fig.3.

The converter is cleared by taking $\overline{WR}$ low, which sets the MSB of the DAC, sets Status and resets all other bits. While $\overline{WR}$ is low, the address latches are transparent and converter operation is inhibited. The $\overline{WR}$ pulse can be as short as 50ns; however the MSB must be allowed to settle for at least 1.0μs before the MSB decision is made. To ensure the this criterion is met even with short write pulses, the conversion starts at the next negative clock edge after the positive edge of $\overline{WR}$. This ensures that the MSB is allowed to settle for at least a full clock period or 1μs at the maximum clock frequency.

The Status output goes low at the end of the conversion, indicating that new data is available. Having completed the first conversion the device will immediately begin another and will continue to convert on the channel in the address latch until a new channel is selected and conversion re-started by pulsing $\overline{WR}$ low. Note that conversion can only be inhibited by holding $\overline{WR}$ low.

The double buffering on the 3-state data outputs gives extra flexibility, allowing the $\overline{RD}$ input to operate asynchronously with repect to Status and always produce valid data. Note that $\overline{RD}$ cannot be tied low as it would prevent the Result Latches from updating at the end of the conversion.

INTERRUPT DRIVEN MODE

The device can also be used in an interrupt driven mode by using the Status output. A $\overline{WR}$ pulse initiates a conversion, sending Status high. The high to low transition of Status, indicating the end of conversion, can be used as an interrupt signal by the microprocessor, i.e.,to inform the microprocessor that a conversion has been completed. On receiving the interrupt, the microprocessor sends an $\overline{RD}$ pulse to take in the new data. On the rising edge of the $\overline{RD}$ pulse internal logic sets the Status output high, hence removing the interrupt signal. This can be seen in Fig.3a by refering to the 'Status (with $\overline{RD}$)' waveform.

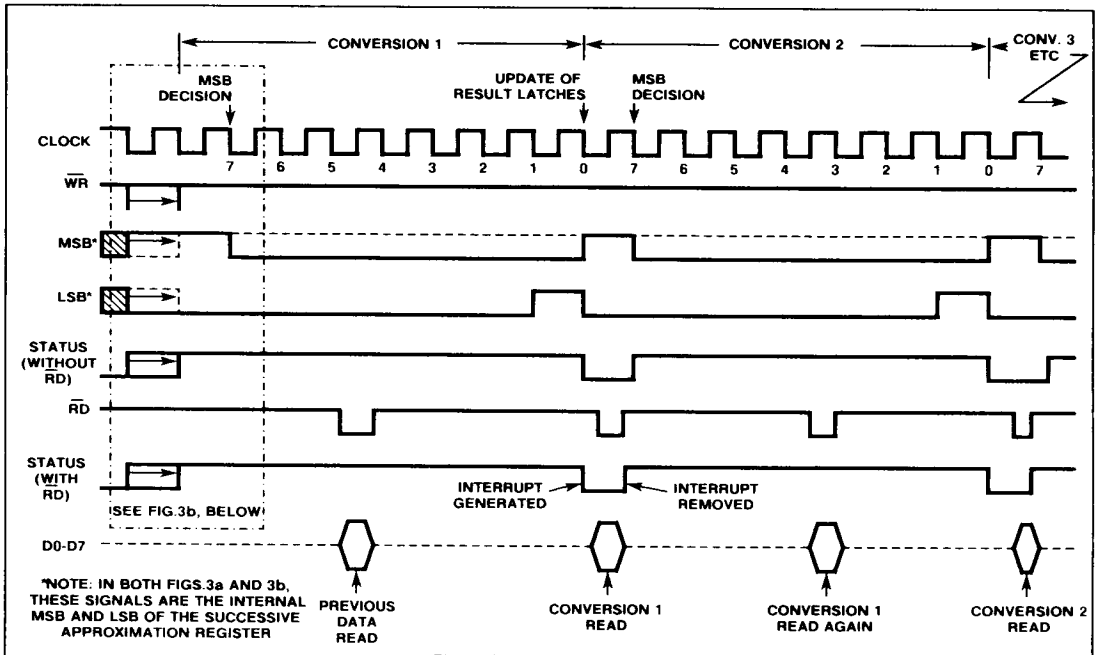


Fig.3a Main timing diagram

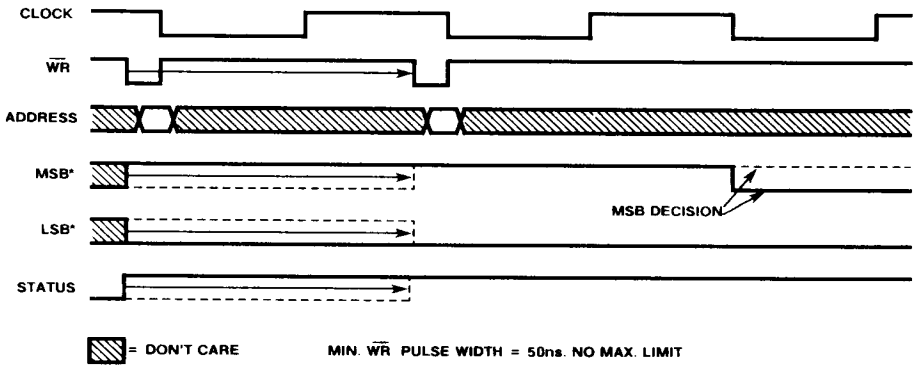


Fig.3b Expanded inset

Fig.3 Timing digram

DATA OUTPUTS

The data outputs are provided with 3-state buffers to allow connection to a common data bus.An equivalent circuit is shown in Fig.4. While the $\overline{RD}$ input is high both output transistors are off and the device presents only a high impedance load to the bus. When $\overline{RD}$ is low the data outputs will assume the logic states present on the outputs of the double buffered register.

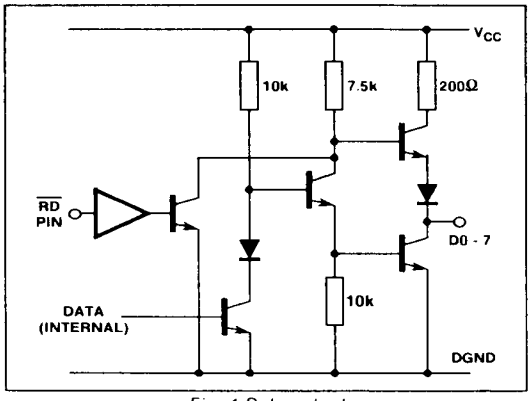


Fig. 4 Data outputs

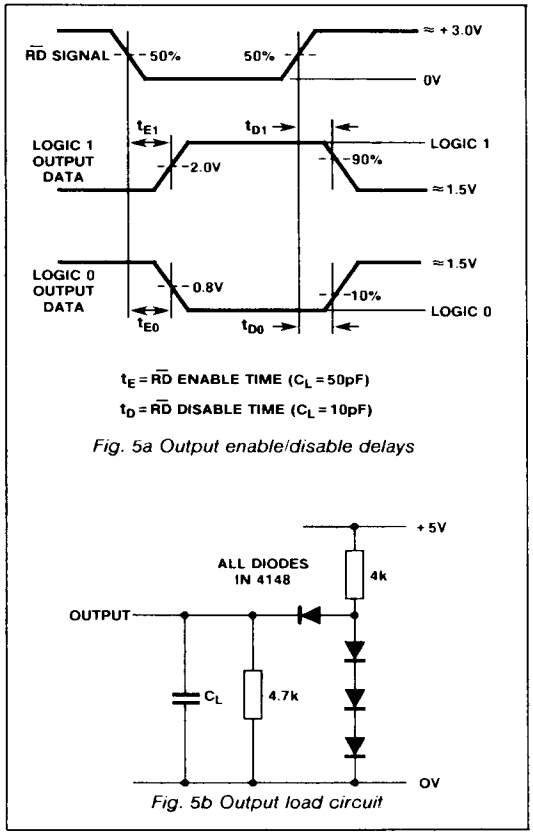


Fig. 5a Output enable/disable delays

Fig. 5b Output load circuit

A test circuit and timing diagram for the input/output delays are given in Fig.5.

The Status output uses the same active pull-up as the data outputs for CMOS/TTL compatibility.

ON-CHIP CLOCK

The on-chip clock operates with only a single external capacitor connected between the clock pin and ground as shown in Fig.6a. A graph of typical oscillator frequency versus capacitance is given in Fig.7. The oscillator frequency may be trimmed by means of an external resistor in series with the capacitor as shown in Fig.6b. A graph of typical oscillator frequency versus resistance and capacitance is given in Fig.8. The oscillator may be overdriven with an external clock signal from a TTL or CMOS gate as shown in Fig. 6c.

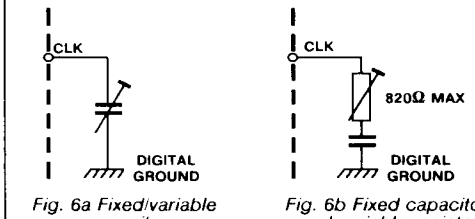


Fig. 6a Fixed/variable capacitor

Fig. 6b Fixed capacitor and variable resistor

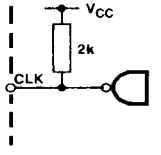


Fig. 6c External TTL or CMOS drive

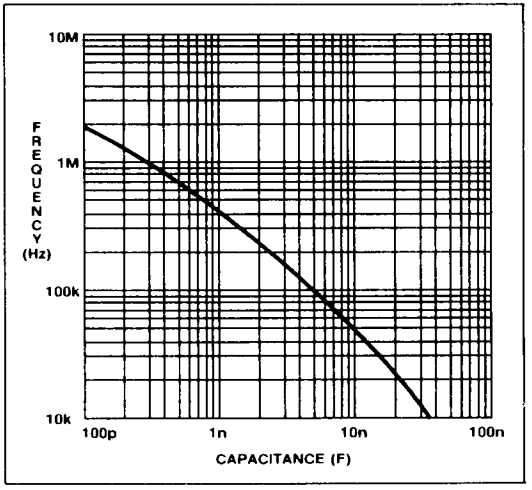


Fig.7 Clock frequency v. capacitance

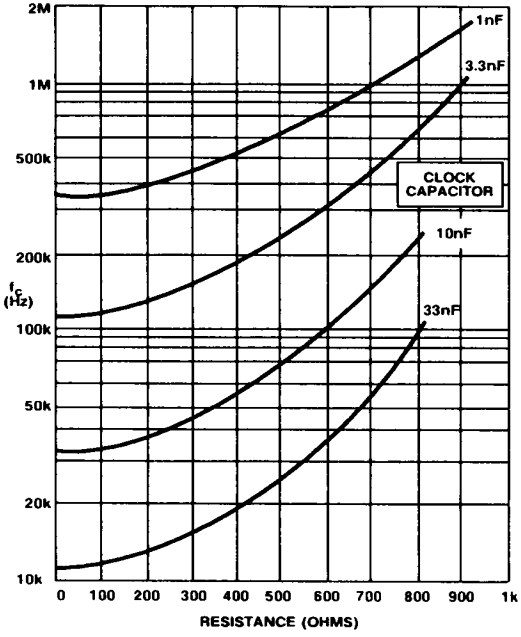


Fig.8 Clock frequency v. resistance and capacitance

ANALOG CIRCUITS

Reference

(a) Internal reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig.9). A resistor (R_{REF}) should be connected between V_{CC} and $V_{REF\ OUT}$ and a decoupling capacitor , C_{REF} (0.47μF), is required between $V_{REF\ OUT}$ and AGND. For internal reference operation, $V_{REF\ OUT}$ is connected to $V_{REF\ IN}$.

A suitable current to drive one ZN68X is nominally 2mA and will be supplied by an R_{REF} of:

$$(5\text{-}2.56) / 2 \times 10^{-3} = 1.2k\Omega$$

If the reference is required to drive more than one ZN68X then the reference current can be increased e.g., an R_{REF} of 470Ω will supply a nominal reference current of:

$$(5\text{-}2.56) / 470 = 5.2mA$$

and this may be used to drive up to three ZN68Xs from just one internal reference. This useful feature saves power and gives excellent gain tracking between the converters.

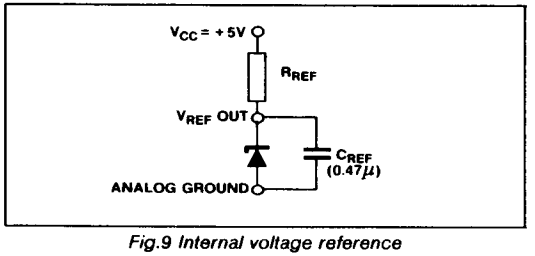


Fig.9 Internal voltage reference

Alternatively, with R_{REF} = 680Ω the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 1.5mA.

(b) External reference

If required, an external reference in the range +2.0V to +3.0V may be connected to $V_{REF\ IN}$. The slope resistance of such a reference should be less than 2.5Ω /n, where n is the number of converters supplied.

Ratiometric Operation

If the output from a transducer varies with its supply then an external reference for the ZN68X should be derived from the same supply. Again, this external reference can vary from +2.0V to +3.0V.

Analog Inputs

The equivalent circuit for each analog input is shown in Fig.10.

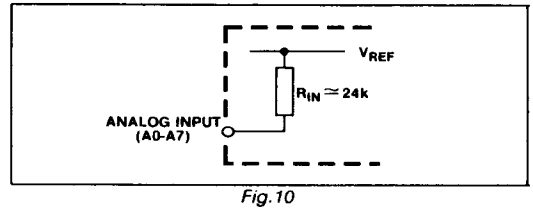


Fig.10

D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig.11. Each element is connected to either 0V or $V_{REF\ IN}$ by by transistor voltage switches specially designed for low voltage offset (1mV typ.).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$DAC\ output = (n/256) \times (V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the DAC from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (±7ppm/°C) the effect on accuracy will be negligible.

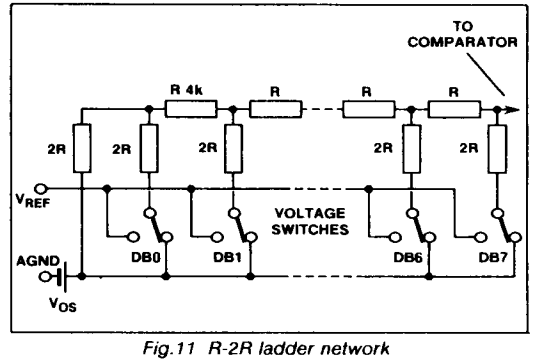


Fig.11 R-2R ladder network