PLESSEY
Semiconductors

T-51-10-05

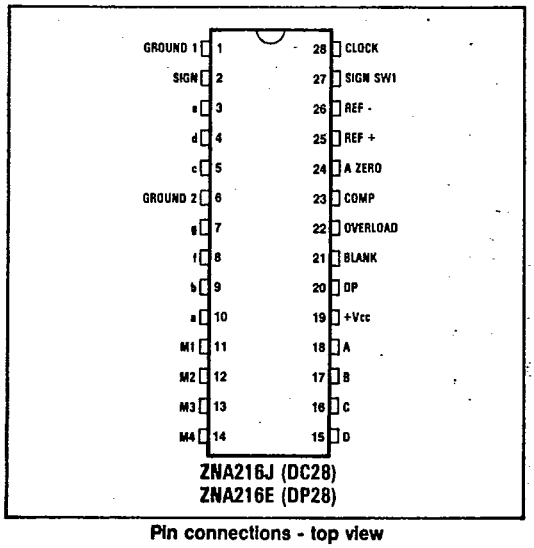
ZNA216

LOW POWER 3¾ DIGIT DVM INTEGRATED CIRCUIT

The ZNA216 DVM IC is a versatile DVM system component which contains all the control logic necessary to construct a dual-slope digital voltmeter, whilst leaving the designer free to configure the analogue circuitry to his own requirements.

The IC has multiplexed data outputs, both in BCD format and in seven-segment format for direct drive of LED displays. A number of useful features are incorporated into the device, including leading zero blanking of the display, flashing overrange indication and an auto zero facility which removes the need for manual zero adjustment.

Apart from the more obvious applications of DVM and DPM the IC can be used to construct any other instrument where an analogue input from, say, a transducer is to be converted into a digital reading, for example a digital thermometer. The ZNA216 may also be used as an A-D converter in single-channel data acquisition systems, or to interface to a microprocessor system.

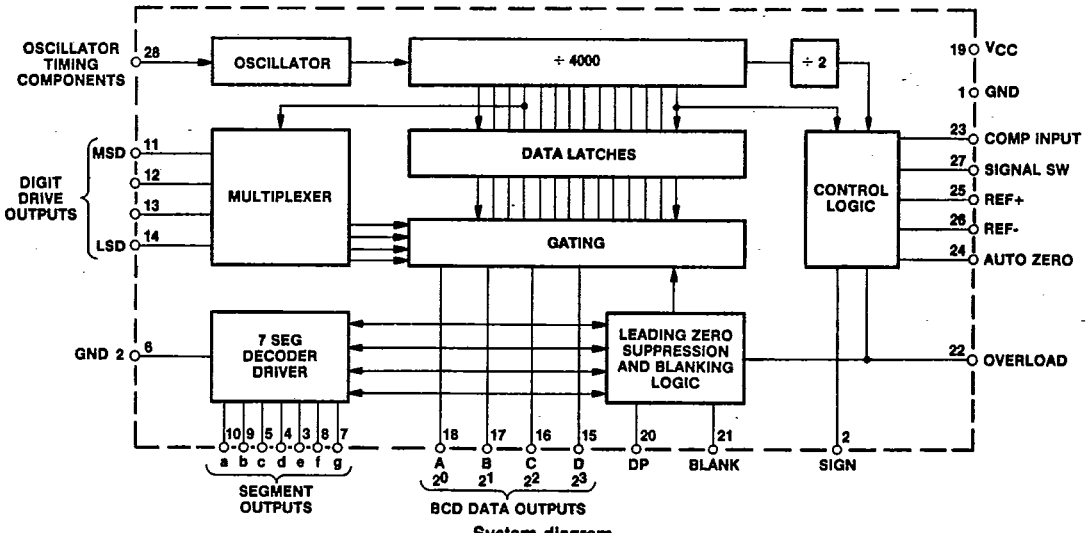


ZNA216J (DC28)
ZNA216E (DP28)

Pin connections - top view

FEATURES

- 3¾ Digit Display (±3999 Max. Reading)
- Automatic Zero Adjustment with 1μV/°C Temperature Coefficient
- Seven-Segment Outputs for Direct Drive of LED Displays
- BCD Outputs
- Automatic Polarity Detection and Indication
- Flashing Overload Indication, Separate Overload Output
- Blanking Input, e.g. For Low Battery Indication
- Automatic Blanking of Display Leading Zeros
- On-Chip Clock, may be Externally Synchronised
- TTL and CMOS Compatible
- Single +5V Supply
- Pinning Optimised for Easy PCB Layout



System diagram

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PINNING AND FUNCTIONAL DETAILS

Pin No.	Name	Function
1	Gnd 1	Supply 0 volts
2	Sign	Open collector output, goes low when −ve input voltage is being measured.
3	e	Open collector segment output, goes low when segment is on.
4	d	Segment output as above.
5	c	Segment output as above.
6	Gnd 2	0 volt supply for segment drivers, must be connected to pin 1.
7	g	Segment output as above.
8	f	Segment output as above.
9	b	Segment output as above.
10	a	Segment output as above.
11	M1	Digit drive output, goes low for the most significant digit to be displayed, first in digit scan sequence.
12	M2	Digit drive output, goes low for the second most significant digit to be displayed, second in digit scan sequence.
13	M3	Digit drive output, goes low for the third most significant digit to be displayed, third in digit scan sequence.
14	M4	Digit drive output, goes low for the least significant digit to be displayed, fourth in digit scan sequence.
15	D	2^3 BCD data output
16	C	2^2 BCD data output.
17	B	2^1 BCD data output.
18	A	2^0 BCD data output.
19	V_{CC}	Supply +5V.
20	DP	When this input is at logic 1, leading zeroes are blanked.
21	Blank	While this input is at logic 1, all segment outputs are off and all BCD data outputs are at logic 1.
22	Overload	If the integrator capacitor does not discharge before the counter reaches 4000, this output goes to logic 1.
23	Comp.	This input is connected to the output of the external comparator.
24	Azero	When this output is high, auto zero correction is applied to the integrator.

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Pin No.	Name	Function
25	Ref +	When this output is at logic 1, the +ve reference voltage is connected to the integrator
26	Ref −	When this output is at logic 1, −ve reference voltage is connected to the integrator.
27	Signal switch	When this output is at logic 1, the input voltage to be measured is connected into the integrator.
28	Clock	The external clock oscillator components are connected to this pin (see diagrams). Alternatively, this pin may be driven by an external signal. A measurement is made every 8000 clock periods. The counter toggles on −ve going clock edges and transfer to the latches occurs at the first +ve going clock edge after comparison has been made which avoids false triggering from the integrator output. Maximum clock frequency 50kHz.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7.0V
Operating temperature	0 to +70°C
Storage temperature	−55 to +125°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 0 to +70°C, V_{CC} = 5V unless otherwise specified).

Parameter		Min.	Typ.	Max.	Units	Test conditions
Supply voltage		4.5		5.5	V	
Supply current				20	mA	
Low level input voltage	All inputs			0.8	V	
Low level input current	All inputs			−4	μA	V_{in} = 0V
Input clamp diode voltage	All inputs			−1.5 V_{CC} +1.5	V V	I_{in} = −12mA I_{in} = 10mA
High level input voltage	Oscillator RC input	2.5			V	
	All other inputs	2.0			V	
High level input current	Oscillator RC input			100	μA	V_{in} = 2.5V
	All other inputs			4	μA	V_{in} = 5.0V
Low level output voltage	a,b,c,d,e,f,g			0.8	V	I_{sink} = 20mA
	Sign			0.4	V	I_{sink} = 5mA
	Overload, Ref+, Ref−, azero, signal switch, a,b,c,d,M1,M2,M3,M4			0.4	V	I_{sink} = 1.6mA
High level output voltage	Overload, Ref+, Ref−, azero, signal switch, a,b,c,d,M1,M2,M3,M4	2.4			V	I_{out} = 10μA
			V_{CC} −0.1		V	I_{out} = 0
High level output current	a,b,c,d,e,f,g, sign			−10	μA	V_{out} = 5.0V

Note: Although the oscillator and logic will function up to 50kHz, this is not recommended as the analogue circuitry becomes more critical.

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THE DUAL SLOPE SYSTEM

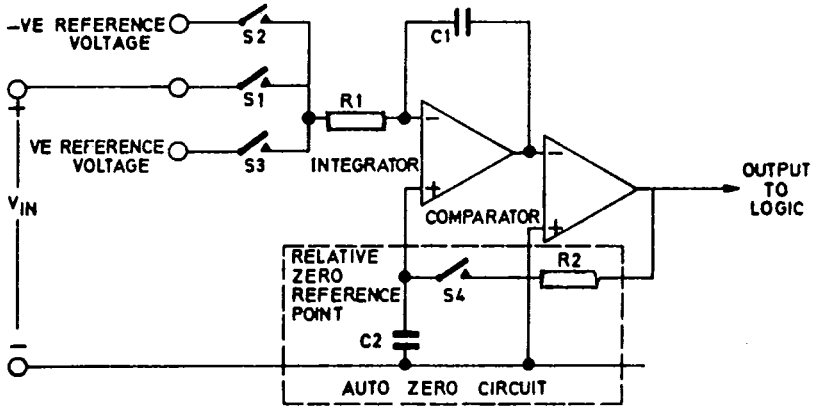

Fig. 1 Dual slope block diagram

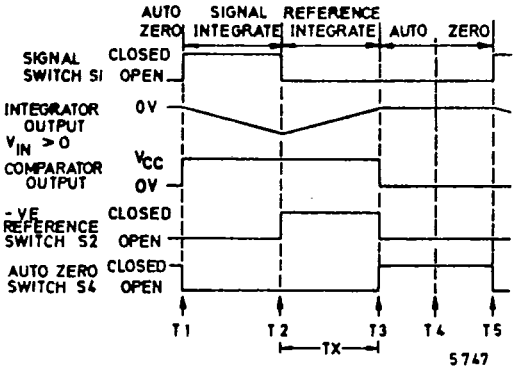

Fig. 2a Timing diagram for in-range input

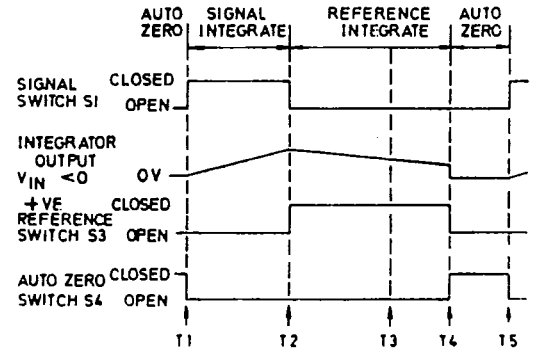

Fig. 2b Timing diagram for overrange input

Dual slope integration is a D.V.M. circuit technique designed to cancel out the effects of drift in circuit components. A block diagram of the analogue section of a dual-slope D.V.M. is shown in Fig. 1, whilst a timing diagram for its operation is shown in Fig. 2.

At time T_1, S1 is closed by the D.V.M. logic, connecting the input signal to the integrator until time T_2, which is 2000 clock periods after T_1. During this time the integrator output ramps positive or negative, depending on input voltage polarity, to a voltage

$$V_o = \frac{-V_{in}2000\ t_c}{R_1C_1}$$

where t_c is the clock period.

The polarity of the integrator output voltage during this period, and hence of the input voltage, is sensed by the comparator, whose output is connected to the control logic.

At time T_2, S1 is opened and, depending on the input voltage polarity, either S2 or S3 is closed. This connects a reference voltage of opposite polarity to V_{in} to the integrator input, so that the integrator output ramps back towards zero. The number of clock periods required for the integrator output to reach zero is counted by the D.V.M. counter. When the output reaches zero the comparator output changes state, S2 or S3 opens and the count is stopped. Since the second integration also takes place over a voltage V_o then,

$V_o = \frac{-V_{REF}\,nt_c}{R_1C_1}$ where n is the count at time T_3

but V_o also equals $\frac{-V_{in}\ 2000t_c}{R_1C_1}$

$$\text{thus } n = \frac{2000\ V_{in}}{V_{REF}}$$

R_1, C_1 and t_c have disappeared from this final equation, so the accuracy of the D.V.M. is unaffected by the long-term stability of these parameters. The only factors influencing accuracy are the stability of V_{REF} and variations in the 'on' resistance of the analogue switches S1 to S3. The former can be assured by careful choice of a reference source, e.g. the Plessey ZN423 or ZN458, whilst the effect of the latter can be minimised by making R_1 large compared to the on resistance of S1 to S3.

If V_{REF} is exactly 2V then $n = 1000\ V_{in}$, i.e. the count will be equal to the input voltage in millivolts. For the ZNA216 the maximum reading is 3999. If a count of 4000 occurs before the integrator output reaches zero, as shown in Fig. 2b, then S2 or S3 will open and the overrange output will go high.

In a practical D.V.M., it is unlikely that a reference voltage of exactly 2V will be available, or an input range other than 3.999V may be required. In this case a different resistor value (R_{REF}) will be used for the reference integration. The equation then becomes:

$$n = \frac{2000\ V_{in}.\ R_{REF}}{V_{REF}.\ R_1}$$

R_1 and R_{REF} should be high-stability types.

AUTO ZERO

Any offset voltage and bias current in the integrator will be integrated along with the input signal and since, for example, a 3,999V D.V.M. has a resolution of 1mV an offset of a few hundred microvolts can lead to errors in the least significant digit. Manual zero adjustment is time-consuming and has to be repeated frequently due to temperature drift.

The auto zero of the ZNA216 operates during the period T_3 to T_5, or T_4 to T_5 in the case of an overrange input. S4 is closed, S1, S2 and S3 are opened so that only the integrator offset voltage is integrated, thus causing the integrator output to drift either positive or negative. The integrator output is amplified by the comparator (which is nothing more than an extremely high gain amplifier) and this charges C2 via R2 to apply a voltage to the non-inverting input of the integrator. The polarity of this voltage is such as to null out the effects of integrator offset voltage and bias current and thus cancel integrator drift. Depending on comparator gain a zero error of a few hundred nanovolts may be achieved by this method.

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HUM REJECTION

Any mains hum pickup superimposed on the input signal will cause errors in the D.V.M. reading. However, if the period T_2-T_1 is made a multiple of the mains period then equal numbers of positive and negative half-cycles of the mains waveform will be integrated and will cancel each other out. For 50Hz mains T_2-T_1 should be 20ms or a multiple thereof, while for 60Hz mains T_2-T_1 should be 16.67ms or a multiple thereof.

Adjustment of the period T_2-T_1 is achieved by varying the frequency of the clock oscillator which controls the operation of the D.V.M.

DISPLAY MULTIPLEXING

The BCD and seven-segment data outputs are multiplexed, the data appearing in the sequence MSD to LSD. To identify which digit is present at the outputs at any time the four digit select outputs go low in turn, synchronous with the relevant digit appearing at the data outputs. The seven segment outputs can be used to drive the cathodes of a multiplexed common-anode LED display whilst the digit select outputs may be used to turn on digit drive transistors which activate each display digit in sequence.

DECIMAL POINT (ZERO BLANKING) INPUT

Before the start of each multiplex cycle a latch in the I.C. is set. This holds the display blanked until non-zero data appears at the BCD outputs, when the latch is reset and the display is unblanked. For example, if the MSD were non-zero the latch could reset immediatey the MSD appeared, so all four digits would be displayed. Conversely if the MSD were zero but the second digit were non-zero then the display would be blanked for the MSD and only three digits would appear. In this way leading zeroes in the display are suppressed. The LSD is always displayed whether zero or not.

The D.P. input can be used to override the zero blanking by taking this pin to logic '0'. This facility allows a correct display to be obtained when a decimal point is used.

For example, if the decimal point is to the left of the MSD then a low-going pulse to the D.P. input synchronous with the MSD output will cause all digits to the right of the decimal point to be displayed, whether zero or not. Thus, if the input voltage were, say .0056V then the display would be .0056. If the zero blanking were not overridden in this way the display would be .--56, which is clearly unsatisfactory.

OSCILLATOR CIRCUIT

The operation of the D.V.M. circuit is controlled by a clock oscillator, which provides drive for the counter, control logic and display multiplexing. Two external components, a resistor and a capacitor, are required to make the oscillator function. The oscillator temperature stability is typically $\pm 0.02\%$ per °C.

As mentioned earlier, the oscillator frequency should be chosen so that T_2-T_1 is a multiple of the mains period. It should not be chosen so low as to cause noticeable flicker in the display multiplexing, but on the other hand it should not be chosen too high or the design of the analogue circuitry becomes more critical.

The optimum oscillator frequency is 20kHz since this makes T_2-T_1 = 100ms which gives good hum rejection at either 50Hz or 60Hz. This frequency can be obtained by using the component values shown in Fig. 3. The potentiometer may be adjusted to give a frequency of 20kHz measured at pin 28, in which case a high impedance, low capacitance probe should be used to avoid loading the oscillator. Alternatively, the trimmer may be adjusted to give a frequency of 500Hz at any of the digit select outputs, when no special precautions are required.

If required the oscillator timing components may be omitted and the oscillator input may be driven by an external clock at TTL logic level.

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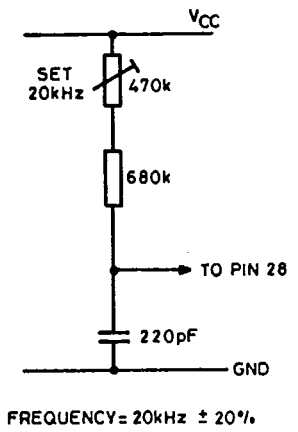

Fig. 3 Oscillator external components

INPUT AND OUTPUT CIRCUITS

Apart from the oscillator input (which is a Schmitt trigger type of circuit) all other inputs are as shown in Fig. 4a. All outputs are as shown in Fig. 4b, except for those designated as open-collector, which have no pull-up resistor.

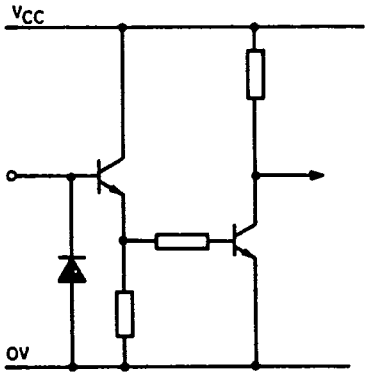

Fig. 4a Input circuit

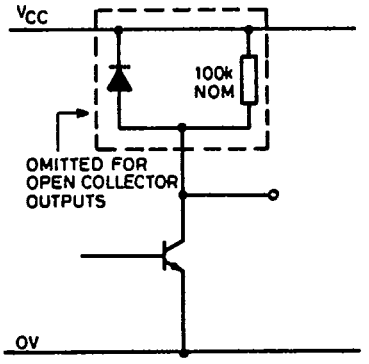

Fig. 5b Output circuit

DISPLAY DRIVING

The 20mA sink capability of the segment outputs allows common anode LED displays to be driven with a minimum of external components, as shown in Fig. 5. The segment current limit resistors should be chosen to give the desired segment current, allowing for the forward voltage drop of the LED, whilst the digit output resistors sould be chosen to give sufficient base current to saturate the digit drive transistors.

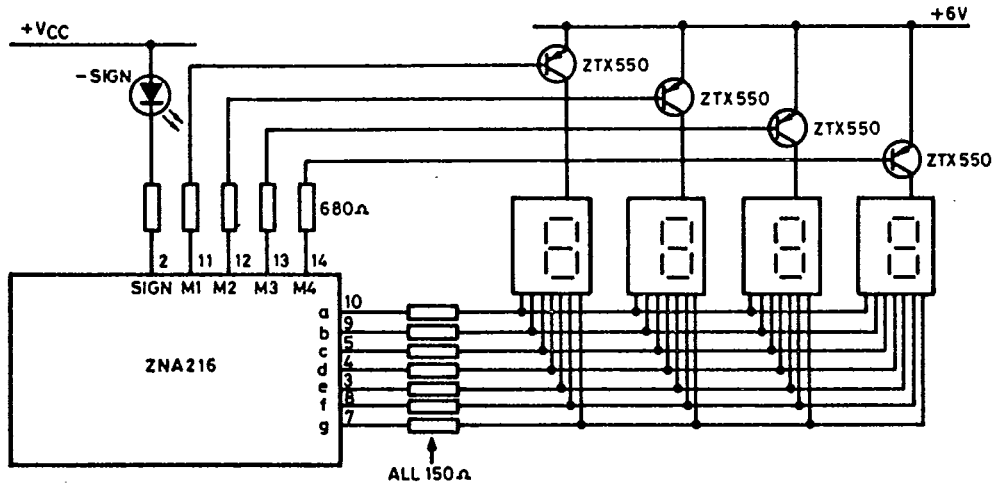

Fig. 5 Display drive circuit

OVERRANGE AND LOW BATTERY INDICATION

If the input voltage exceeds the full-scale range then the display will flash all 'eigths' and the overrange output, pin 22, will go high. Low battery indication may also be provided by the addition of the simple circuit shown in Fig. 6.

Whilst the battery voltage is above 4.4V T_1 will be turned on via R1 and R2. Below this voltage the base potential supplied by these resistors will be insufficient to turn on T_1 and it will then be turned on and off cyclically by the auto-zero output, causing the display to flash whatever reading is present.

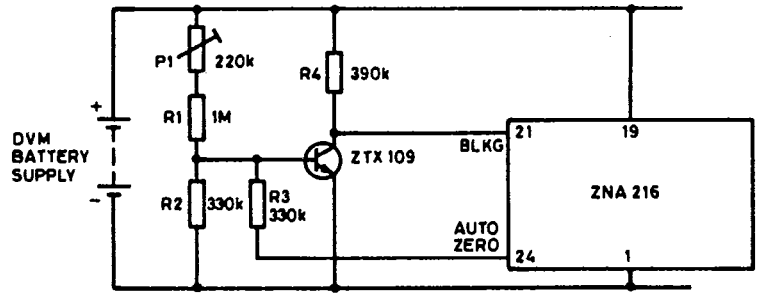

Fig. 6 Low battery indication

A PORTABLE D.V.M.

Fig. 7 shows the circuit of a battery-powered D.V.M. based on the ZNA216, which uses readily available components. ZN424 op-amps are used for the integrator and comparator, whilst bipolar silicon transistors are used for the analogue switches. The basic sensitivity of the instrument is 4V, and additional ranges of 40V and 400V are provided by means of an input attenuator. Printed circuit board and component layouts for the D.V.M. are given in Figs. 8a to 9b.

However, this circuit design should by no means be considered as immutable. Since the analogue circuitry is external to the ZNA216 it may be configured to suit the designer's needs to give higher input impedance, increased sensitivity etc.

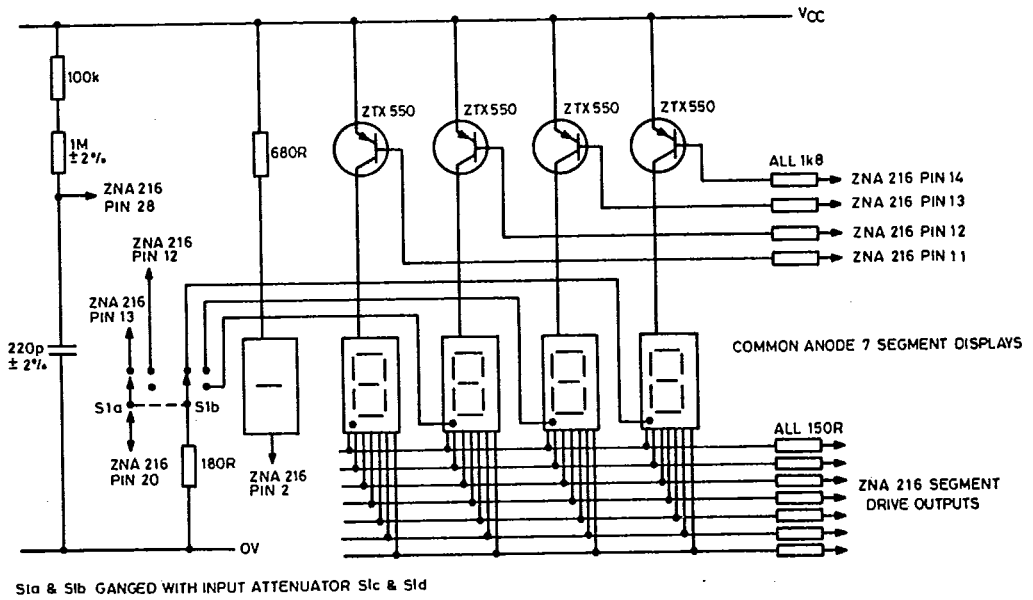

Fig. 7a Battery-powered D.V.M. circuit, display section

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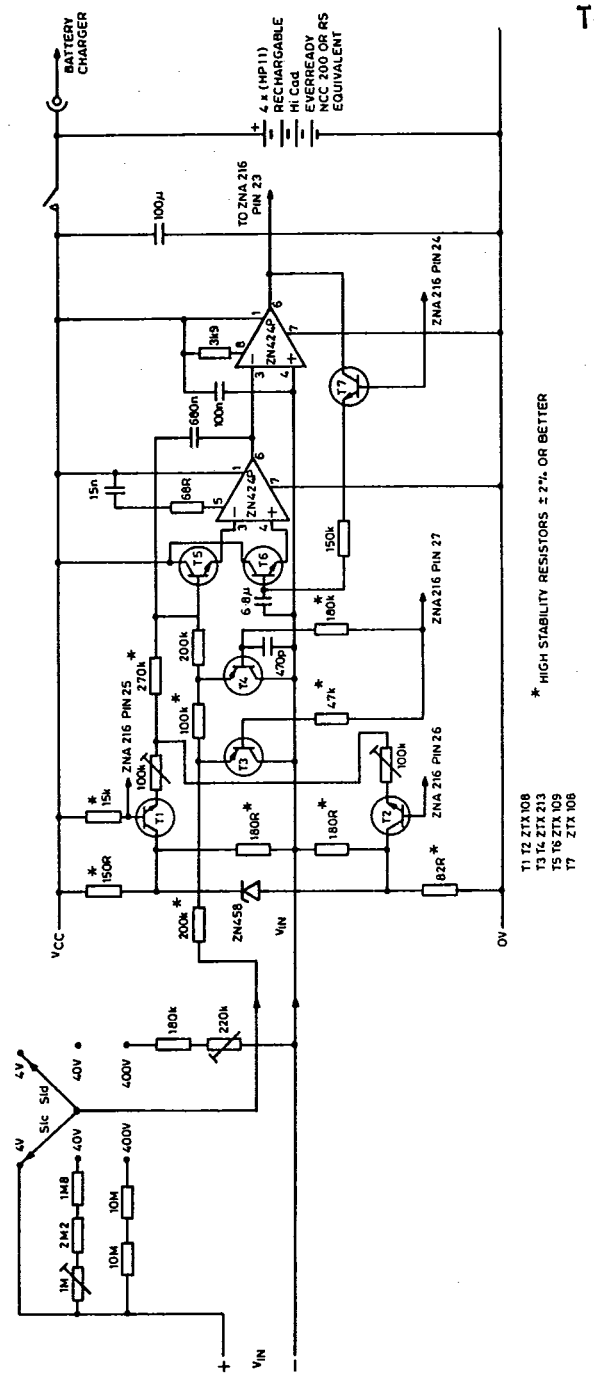

Fig. 7b Battery-powered D.V.M. circuit, analogue section

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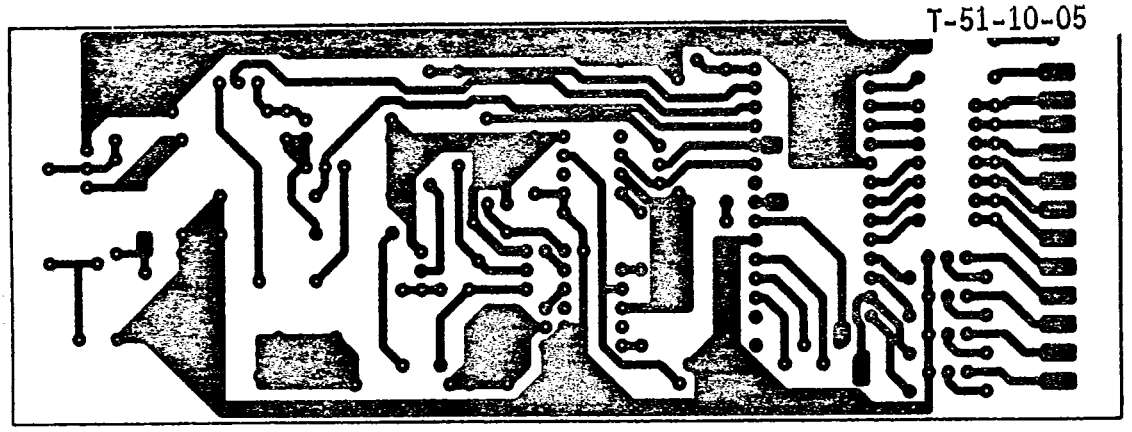

Fig. 8a D.V.M. Main board (1:1)

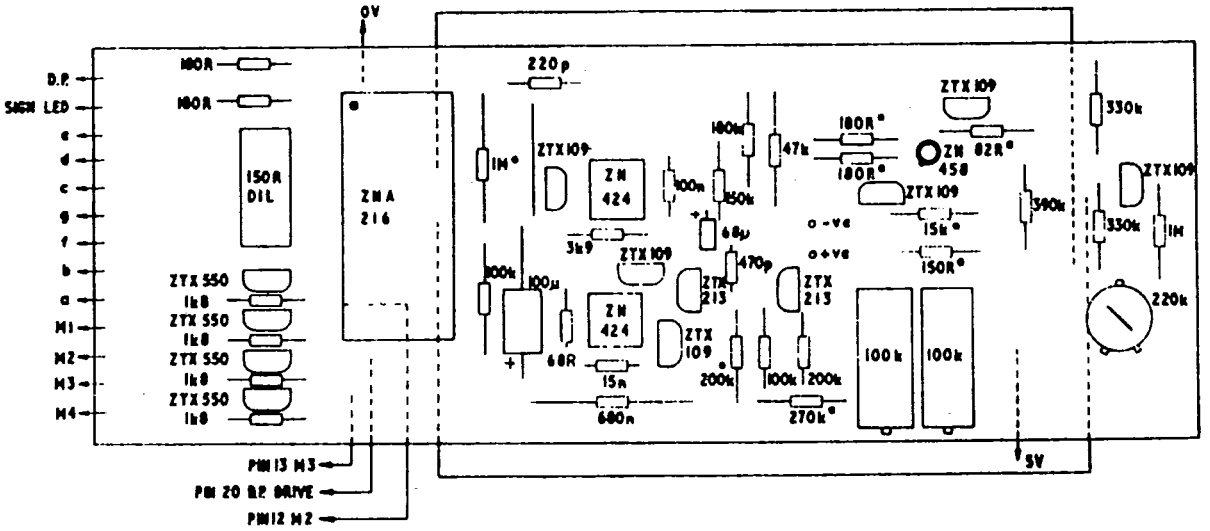

Fig. 8b Component layout for Fig. 8 (1:1)

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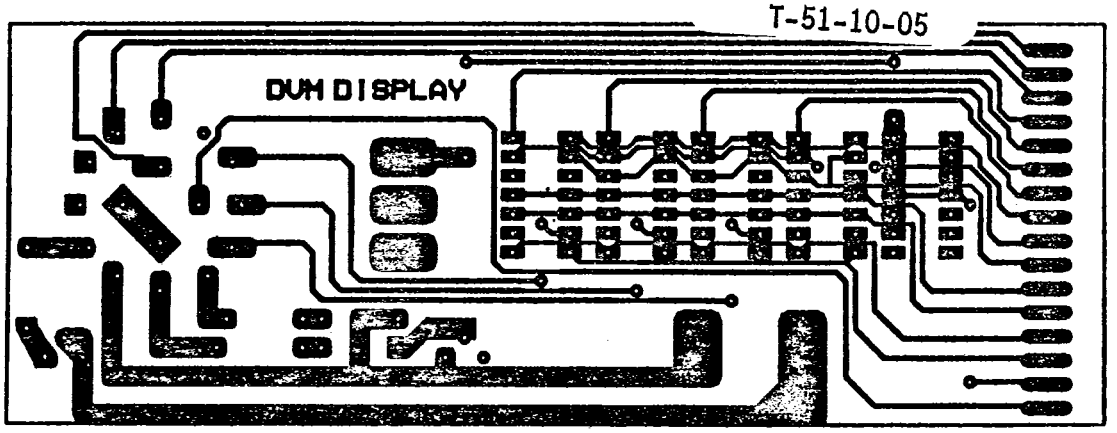

Fig. 9a D.V.M. display board (1:1)

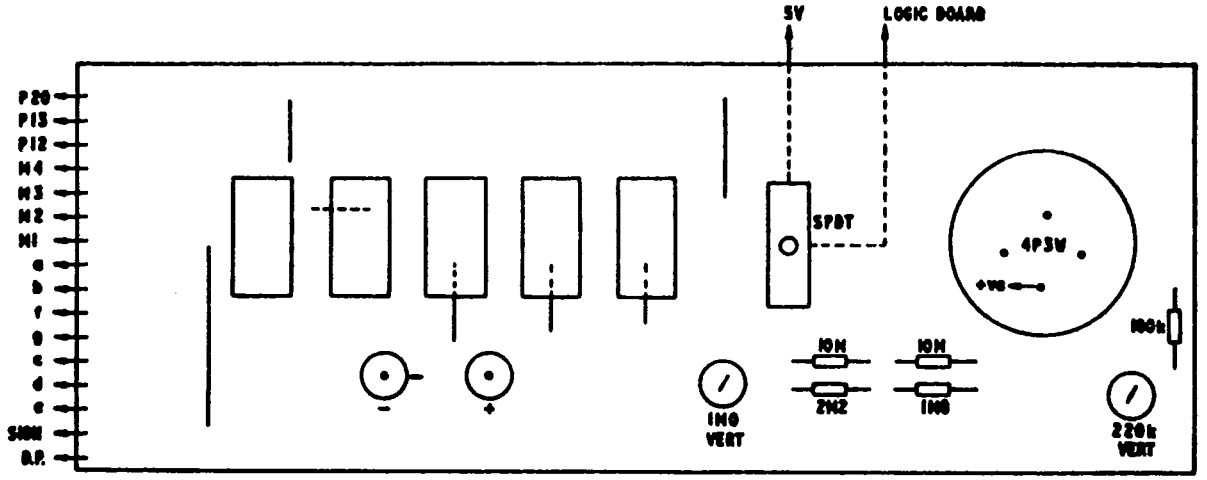

Fig. 9b Component layout for Fig. 9a (1:1)

MICROPROCESSOR INTERFACING

The ZNA216 may be used as a dual-slope A-D converter in data loggers and other data acquisition systems, where its 3¾ decade range offers a resolution comparable to a 13-bit binary ADC, but in a more convenient BCD format.

Fig. 10 is a block diagram which illustrates how the ZNA216 may be interfaced to an 8-bit microprocessor. The principle of operation is that the four multiplexed BCD digits of the ZNA216, plus the sign and overrange bits, are stored in four 4-bit latches so that they are available in parallel form. The contents of the latches can then be read into the microprocessor as two 8-bit words. The latches used are type 74173 which have three-state outputs for direct connection to the μP data bus. Data is clocked into the latches using the positive-going edge of the appropriate digit drive outputs.

The latches are treated as two memory locations by using an address decoder which is connected to their output enable pins. In this way data can be read out of the latches just as from any other memory locations. Once data is in the latches it may be read out whilst the ZNA216 performs the next measurement, thus eliminating any waiting time. The only time when data cannot be read out of the latches is just after the ZNA216 has completed a measurement. At this time the data in the internal latches of the ZNA216 will have been updated and the data in the 74173s may thus be changing. The data in the latches will be stable after two multiplexed cycles of the ZNA216 which is 4ms if a 20kHz clock is used.

Since the auto-zero output of the ZNA216 goes high when a measurement has been completed this output may be used as a BUSY signal. Data should not be read from the 74173 latches until at least 4ms after the auto-zero output has gone high.

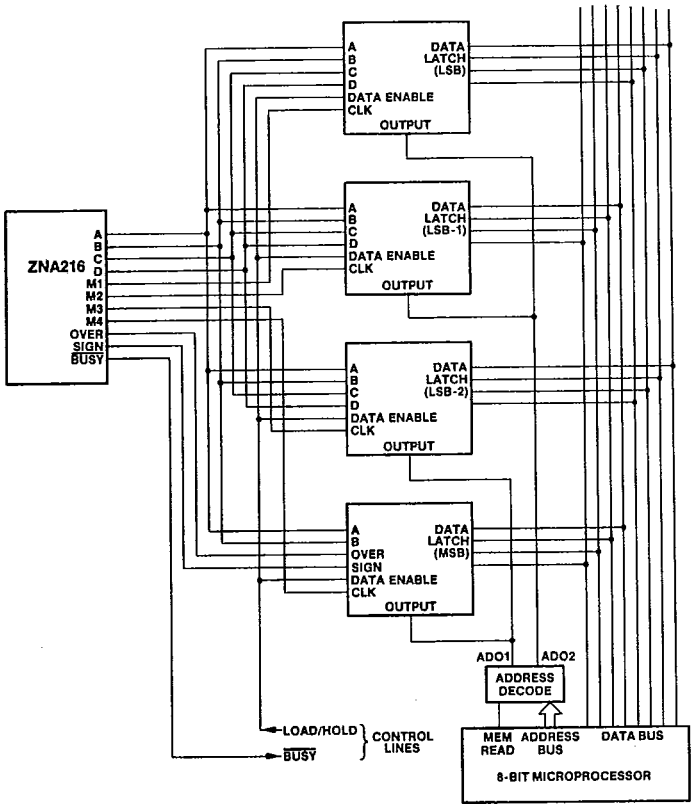

Fig. 10 Interfacing the ZNA216 to a microprocessor