

Read/Write Amplifier for FDD

BH6628AFS

The BH6628AFS is a 4-mode read/write IC designed for floppy disk drives and has an active filter that can be set according to transfer rate. Any of multiple write current settings can be selected, and inner edge/outer edge switching is done internally.

●Applications

Floppy disk drives (1MB, 1.6MB and 2MB)

●Features

- 1) Internal active filter with multiple settings that can be selected for multiple Q and f_0 .
- 2) Time domain filter that is internally switchable according to transfer rate.
- 3) Any of multiple write current settings can be selected, and inner track/outer track switching is done internally.

●Absolute maximum ratings ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	+7	V
Operating temperature range	T_{OPR}	0~+70	$^\circ\text{C}$
Storage temperature range	T_{STG}	-55~+125	$^\circ\text{C}$
Digital input voltage	V_I	-0.5~ $V_{CC}+0.3$	V
RW pin voltage	VRW	+15	V
LVS output voltage	$VLVS$	$V_{CC}+0.3$	V
ED pin voltage	VER	$V_{CC}+0.3$	V
Power dissipation	P_D	650 *	mW

* Reduced by 6.5mW for each increase in T_a of 1°C over 25°C .

●Recommended operating conditions ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V

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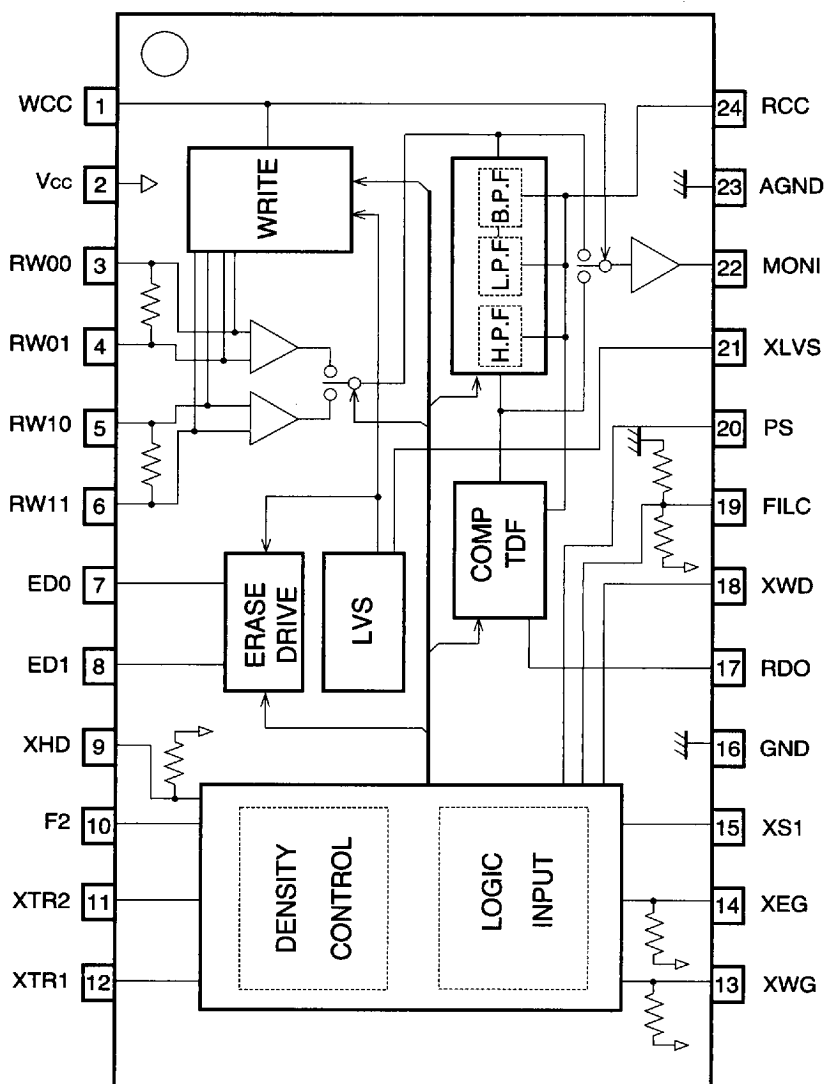
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FDD read/write amplifier

FDD/HDD

● Block diagram



(Note) The Vcc fret pattern must be short, and the impedance between Vcc and GND must be lowered sufficiently by inserting a pass conductor.

Pin No.	Name	Equivalent circuit	Function
1	WCC		For connecting the write current adjustment resistor Connect the write current adjustment resistor between this pin and Vcc. Setting this pin to the low level during reading switches MONI to differentiator output.
2	Vcc		Power supply pin
3	RW00		Active when SIDE0 and the read/write head connecting pin (pin 15, XS1) is at the high level (side 0) Starts at RW00 during the start of writing (from reading to writing)
4	RW01		
5	RW10		Active when the read/write head connecting pin (pin 15, XS1) is at the low level (side 1) Starts at RW10 during the start of writing (from reading to writing)
6	RW11		
7	ED0		Side 0 erase current sink
8	ED1		Side 1 erase current sink

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Pin No.	Name	Equivalent circuit	Function
9	XHD		1 MB/2 MB selector High = 1 MB Low = 2 MB
10	F2		1.6 MB drive selector Selector signal high level = active High = 1.6 MB drive, low = 2 MB drive
11	XTR2		Inner track/outer track position setting Controls the write current
12	XTR1 (XSWF)		Inner track/outer track position setting Controls the filter and write current
13	XWG		Write enable gate (Schmidt input) Low = active
14	XEG		Erase enable gate (Schmidt input) Low = active
15	XS1		Head/side switching signal Low = active (Schmidt input) High = side 0, low = side 1

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Pin No.	Name	Equivalent circuit	Function
16	DGND		Digital ground
17	RDO		Read data output TTL high level = active
18	XWD		Write data input Operates at falling edge (Schmidt input)
19	FILC		Filter control (f0, Q) Used to switch filter cutoff frequency
20	PS		Power save selector High = active

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FDD / HDD

Pin No.	Name	Equivalent circuit	Function
21	XLVS		Open collector output when low level voltage is detected. Switches to low level when Vcc drops below the specified voltage
22	MONI		Preamplifier output and differentiator output monitoring Monitor is switched with pin 1 (WCS)
23	AGND		Analog ground
24	RCC		Filter (LPF, BPF) cutoff frequency and TDF 1st M/M pulse width setting resistor connection

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●Electrical characteristics (unless otherwise noted, Ta=25°C, V_{CC}=5V)

Current consumption

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Current consumption ,Stand-by	ICCST	—	284	400	μA	*1
Current consumption ,Read	ICCR	—	28	42	mA	*1
Current consumption ,Write	ICCW	—	8.5	15	mA	*2

*1 RRCC=2.0 [kΩ] (XHD=H, XWG=XEG=H, FILC=H or L)

*2 RWCC=2.4 [kΩ] (2 MB inner track, XTR2=H time, except IWR and IER)

Low level voltage detection circuit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Threshold voltage 1	VTH1+	—	4.05	4.30	V	When power supply voltage rises, internal LVS goes into write protec
	VTH1—	3.60	3.85	4.10	V	When power supply voltage falls, internal LVS goes into write protect
Threshold voltage 2	VTH2+	—	3.90	4.15	V	When power supply voltage rises, external LVS
	VTH2—	3.45	3.70	3.95	V	When power supply voltage falls, external LVS
Hysteresis voltage	VH	50	—	—	mV	
Output voltage ,low level	VOL	—	—	0.40	V	V _{CC} =2.5 [V] IOL=0.2 [mA]
Output leakage current	IOH	—	—	10	μA	

Recovery time

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
POWER·SAVE→READ	TR2	—	—	500	μs	by PS
READ→ERASE	TR3	—	—	6	μs	by XEG
READ→WRITE	TR4	—	—	4	μs	by XWG
WRITE→READ	TR5E	—	—	20	μs	by XEG
	TR5W	—	—	160	μs	by XWG
SIDE0↔SIDE1	TR6	—	—	40	μs	by XS1
1MB↔2MB	TR7	—	—	40	μs	by XHD
1.6 MB model↔2 MB model	TR8	—	—	40	μs	by F2
Inner track ↔ outer track	TR9	—	—	40	μs	by XTR1
Write current switch	TR10	—	—	40	μs	by XTR2

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Preamplifier

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Voltage gain (1)	GVD1	43	46	49	dB	f=125[kHz], VIN=2.5[mVp-p] (XTR1=L) (differential)
Voltage gain (2)	GVD2	46	49	52	dB	f=125[kHz], VIN=2.5[mVp-p] (XTR1=H) (differential)
SIDE 0 ↔ SIDE 1 cross talk	GCTLK	50	—	—	dB	f=125[kHz], VIN=100[mVp-p] (differential) *3
Differential input resistance	RID	3.55	4.7	—	kΩ	Input resistance 8.0[kΩ] // damping resistance 11.5[kΩ]
Input conversion noise voltage	VN	—	2.5	3.7	μVrms	f=500[Hz] ~ 1[MHz]
Input sink current	ISINK	—	180	—	μA	
Differential input voltage tolerance amplitude (1)	VIN1	—	—	5.0	mVp-p	5% distortion (sinewave input) (XTR1=L)
Differential input voltage tolerance amplitude (2)	VIN2	—	—	3.5	mVp-p	5% distortion (sinewave input) (XTR1=H)
Common mode rejection ratio	CMRR	50	—	—	dB	f=125[kHz], VIN=100[mVp-p] *3
Power supply rejection ratio	PSRR	40	—	—	dB	f=250[kHz], VIN=100[mVp-p] *3

Preamplifier - L.P.F. - differentiator (B.P.F.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Filter time constant accuracy	EFIL	−10	—	+10	%	*3
Preamplifier - L.P.F. - differentiator, total gain (1)	GVDD1	39.5	43.5	47.5	dB	f=250[kHz], VIN=2.5[mVp-p] (differential) (2 MB set up, XTR1=L, FILC=H)
Preamplifier - L.P.F. - differentiator, total gain (2)	GVDD2	43.5	47.5	51.5	dB	f=250[kHz], VIN=2.5[mVp-p] (differential) (2 MB set up, XTR1=L, FILC=H)
Differentiator output peaking frequency setting range	f ₀	0.1	—	0.5	MHz	Defined according to typical value in the setting

*3 RRCC=2.0 [kΩ] (XHD=L, XTR1=H, F2=L, FILC=H)

Comparator and pluse shaper

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
TDF M/M pulse width accuracy (1)	TDF1	−10	—	+10	%	XHD=H, F2=L (Typ.: 2145[ns]) f=62.5[kHz] ~ 125[kHz] *4
TDF M/M pulse width accuracy (2)	TDF2	−10	—	+10	%	XHD=H, F2=H (Typ.: 1780[ns]) f=62.5[kHz] ~ 125[kHz] *4
TDF M/M pulse width accuracy (3)	TDF3	−10	—	+10	%	XHD=L, F2=H/L (Typ.: 1110[ns]) f=125[kHz] ~ 250[kHz] *4
RD pulse width	TRD	270	400	530	ns	Judgement level 1.5 [V]
Rise time	TTLH	—	—	70	ns	Rise time for 0.4 [V] - 2.0 [V]
Fall time	TTHL	—	—	70	ns	Fall time for 2.0 [V] - 0.4 [V]
Peak shift	P. S.	—	—	1.0	%	f=250[kHz], VIN=1[mVp-p] (differential)
Output "L" level voltage when loaded	VOL	—	—	0.4	V	IOH=0.2[mA]
Output "H" level voltage when loaded	VOH	2.7	—	—	V	IOH=−15[μA] *5

*4 RRCC=2.0 [kΩ]

*5 Rise level from 0.4 [V] to 70 [ns]

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Write circuit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Write current adjustment range	IWR	2.0	—	20	mA0-p	
Write current accuracy	ACIW	-7.0	—	+7.0	%	*6
Write current pairability	Δ IWR	-1.0	—	+1.0	%	RWCC=2.0[k Ω]
Write current supply voltage dependency	PSIW	-4.0	-0.8	+3.0	%/V	RWCC=2.0[k Ω]
Output saturation voltage	VSATRW	—	0.4	1.0	V	IWR=12[mA]
Off-state leakage current	ILKRW1	—	—	20	μ A	Selected side
	ILKRW2	—	—	50	μ A	Unselected side
Minimum write data pulse width	TWD	70	—	—	ns	
Write current inner/outer track ratio accuracy	ACIWTR	$\pm 10 \times (1\text{-setting ratio})$			%	*7
Damping resistance accuracy	ACDR	-25	—	+25	%	8 [k Ω] when writing/damping resistance 11.5 [k Ω]

*6 RWCC=2.0 [k Ω] , adapted for desired setting of XTR1/XTR2

*7 Error in setting ratio (reference: XRT1/XRT2=L)

Erase input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Erase current adjustment range	IER	—	—	40	mA	
Output saturation voltage	VSATER	—	0.2	0.6	V	IER=40[mA]
Output leakage current	IOH	—	—	10	μ A	When OFF, ED0=ED1=Vcc

Logic input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
"H" Input voltage	VIH	2.0	—	—	V	Except FILC
"L" Input voltage	VIL	—	—	0.8	V	Except FILC
Input voltage hysteresis	VH	0.15	—	—	V	Applicable to pins XWD, XWG, XEG, XS1
"L" Input current	IIL	—	50	100	μ A	Vcc=5[V], VIL=GND Applicable to pins XWG, XEG, XHD
	VIH	4.2	—	—	V	Applicable to FILC
	VIM	2.0	2.5	3.0	V	Applicable to FILC
	VIL	—	—	0.8	V	Applicable to FILC
	IIH	—	89	133	μ A	Vcc=5[V], VIH=Vcc, Applicable to FILC
Tri-state interface	IIL	—	89	133	μ A	Vcc=5[V], VIL=GND, Applicable to FILC

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●Read characteristics

Density				1MB				1.6MB		2MB	
Transfer rate			FILC	250[kbps]		300[kbps]		500[kbps]		500[kbps]	
Input	Mode	XHD	NO CARE	HI		HI		LOW		LOW	
		F2	NO CARE	LOW		HI		HI		LOW	
	Track	XTR1 (XSWF)	NO CARE	Outer track LOW	Inner track HI	Outer track LOW	Inner track HI	Outer track LOW	Inner track HI	Outer track LOW	Inner track HI
Output	Filter	f ₀ [kHz]	HI	168	182	201	216	349	403	349	373(C)
			OPEN	152	167	181	199	332	382	349	376(B)
			LOW	168	182	201	216	349	403	349	376(B)
	Characteristics (*1)	NO CARE	(D)	(A)	(D)	(A)	(D)	(A)	(D)	Described above	
	TDF	[nSEC]	NO CARE	2145		1780		1110		1110	

(Note) *1 (A) Butterworth characteristics (B) Chebyshev's characteristics (C) High ripple chebyshev's characteristics
(D) Low Q Butterworth characteristics (However, RRCC=2.0 [kΩ] Refer to filter characteristics

Total filter peak frequency setting

$$f_0 = a / (RRCC [k\Omega] + 0.09) [kHz]$$

FILC	"H"	"M"	"L"	
a =	351	318	351	250 [kbps] outer track
	380	353	380	250 [kbps] inner track
	420	378	420	300 [kbps] outer track
	451	416	451	300 [kbps] inner track
	729	694	729	500 [kbps] outer track (when F2 = H)
	842	807	842	500 [kbps] inner track (when F2 = H)
	729	729	729	500 [kbps] outer track (when F2 = L)
	780	786	786	500 [kbps] inner track (when F2 = L)

TDF time constant setting

$$250 [kbps] : T = 796 \times RRCC [k\Omega] + 607 [ns]$$

$$300 [kbps] : T = 614 \times RRCC [k\Omega] + 552 [ns]$$

$$500 [kbps] : T = 331 \times RRCC [k\Omega] + 448 [ns]$$

●Write current switching ratio

Track		Outer track ← ————— → Inner track			
Density	XTR1	L		H	
	XTR2	L	H	L	H
	2MB	0.450	0.333	0.300	0.300
	1.6MB	0.450	0.383	0.333	0.333
	1MB (250kbps)	0.900	0.800	0.700	0.700
	1MB (300kbps)	0.933	0.800	0.700	0.700

Write current setting

$$I_{wr} = \frac{24.0}{RWCC [k\Omega]} [mA]$$

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● Filter characteristic

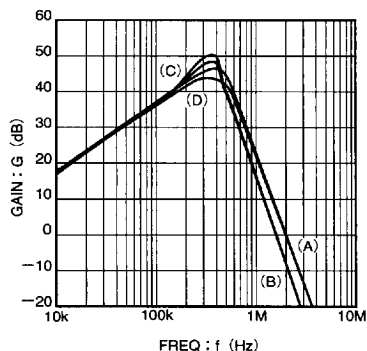
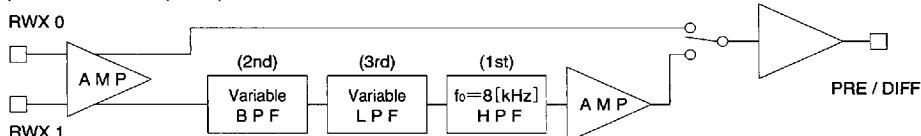
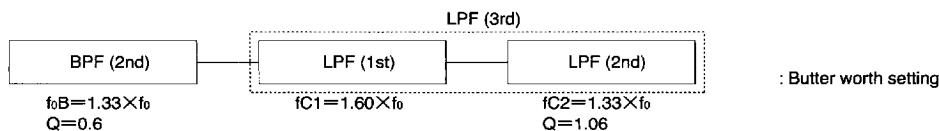
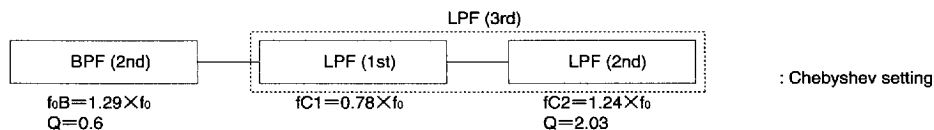
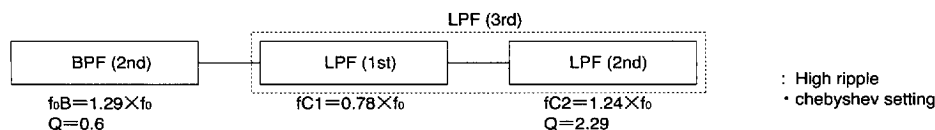
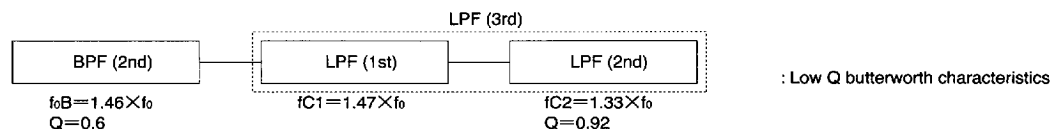


Fig. 1 PRE IN vs. DIFF OUT characteristics

Preamplifier - differentiator(B.P.F.) - L.P.F.

(A) [1 M/1.6 M inner track] Total characteristics peak frequency f_0 (B) FILC="L" time [2 M inner track] Total characteristics peak frequency f_0 (C) FILC="H" time [2 M inner track] Total characteristics peak frequency f_0 (D) [1 M/1.6 M/2 M outer track] Total peak frequency f_0 

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FDD read/write amplifier

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● Operation notes

- (1) Use a short pattern for V_{CC} , and a sufficiently wide AGND and DGND. Keep the impedance between V_{CC} and GND low by inserting a bypass capacitor.
- (2) Use a pattern that will minimize interference between digital signals and the head.

● Electrical characteristic curves

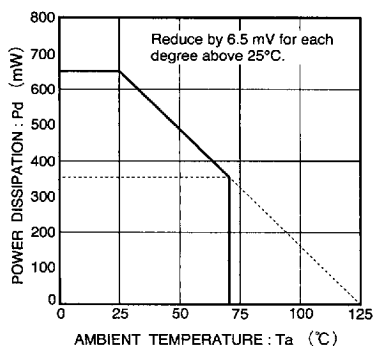


Fig. 3 Thermal derating curve

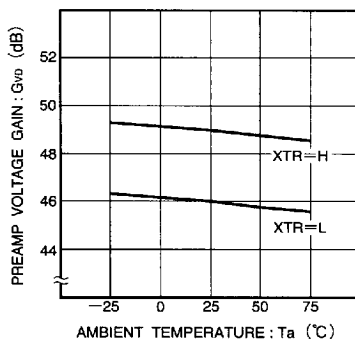


Fig. 4 Preamp voltage gain vs. ambient temperature

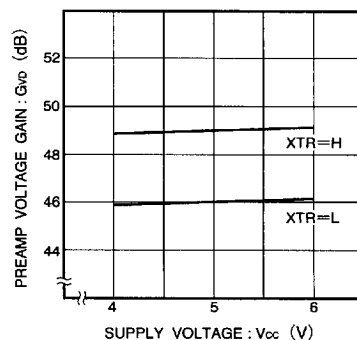


Fig. 5 Preamp voltage gain vs. supply voltage

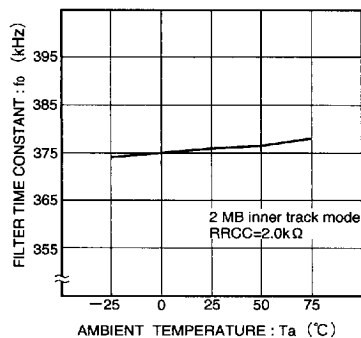
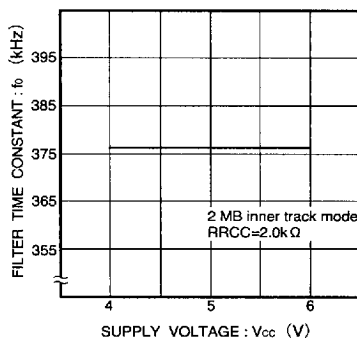
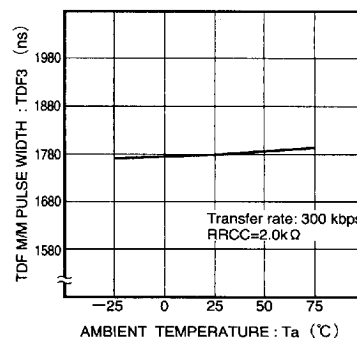
Fig. 6 Filter time constant (f_0) vs. ambient temperatureFig. 7 Filter time constant (f_0) vs. supply voltage

Fig. 8 TDF time constant vs. ambient temperature

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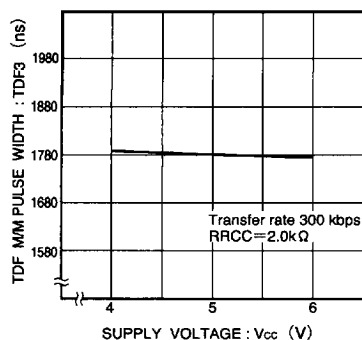


Fig. 9 TDF time constant vs. power supply voltage

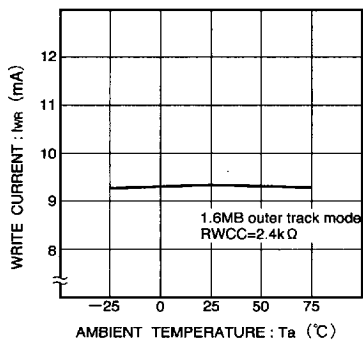


Fig. 10 Write current vs. ambient temperature

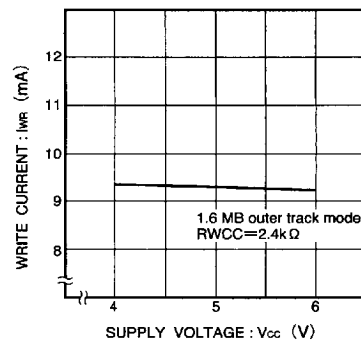


Fig. 11 Write current vs. power supply voltage

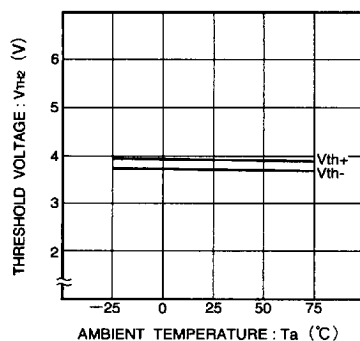


Fig. 12 Low level detection voltage vs. ambient temperature

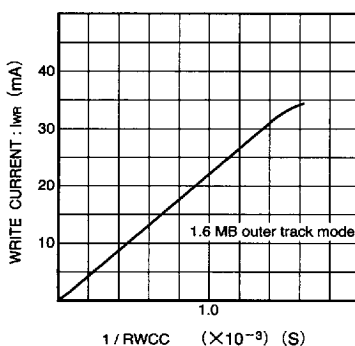
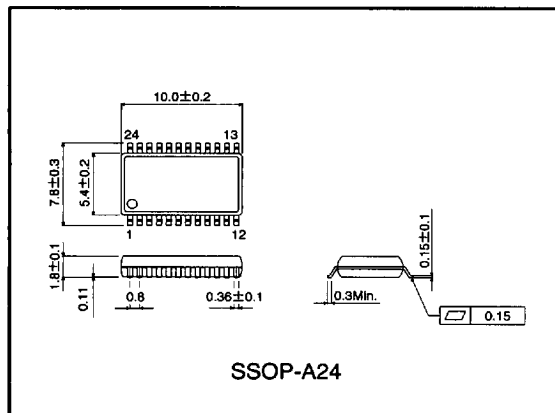


Fig. 13 Write current vs. write current setting resistance

● External dimensions (Units: mm)



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