

4-HEAD PLAYBACK AND RECORD AMPLIFIER FOR VCR

PRELIMINARY DATA

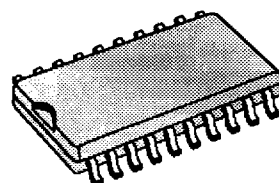
- ONE 5V POWER SUPPLY
- PLAYBACK/RECORD MODE SELECTION THROUGH A LOGIC INPUT
- SO20 PACKAGE
- NO ADJUSTMENT FOR LUMINANCE RECORDING

PLAYBACK MODE

- LOW NOISE AND WIDE BAND AMPLIFIERS FOR 4 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 2 SELECTED HEADS
- ONE PLAYBACK OUTPUT
- ONE OUTPUT FOR AUTOMATIC VIDEO TRACKING
- SP/LP ENVELOPE COMPARATOR
- SHORT-CIRCUIT SWITCHES ON UNUSED HEADS

RECORD MODE

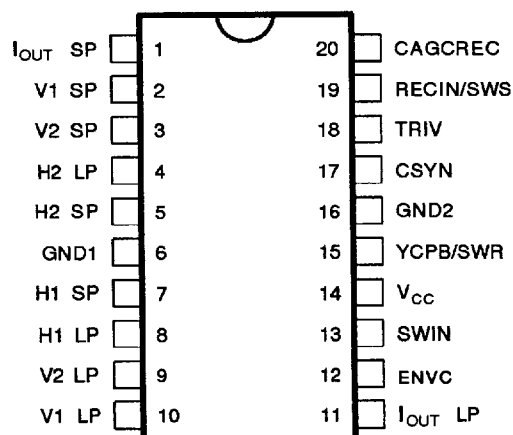
- RECORD AGC AMPLIFIER SAMPLED BY SYNCHRO SIGNAL
- RECORDING SIGNAL LEVEL ADJUSTABLE BY EXTERNAL RESISTOR
- SHORT-CIRCUIT SWITCHES ON UNUSED HEADS



SO20
(Plastic Package)

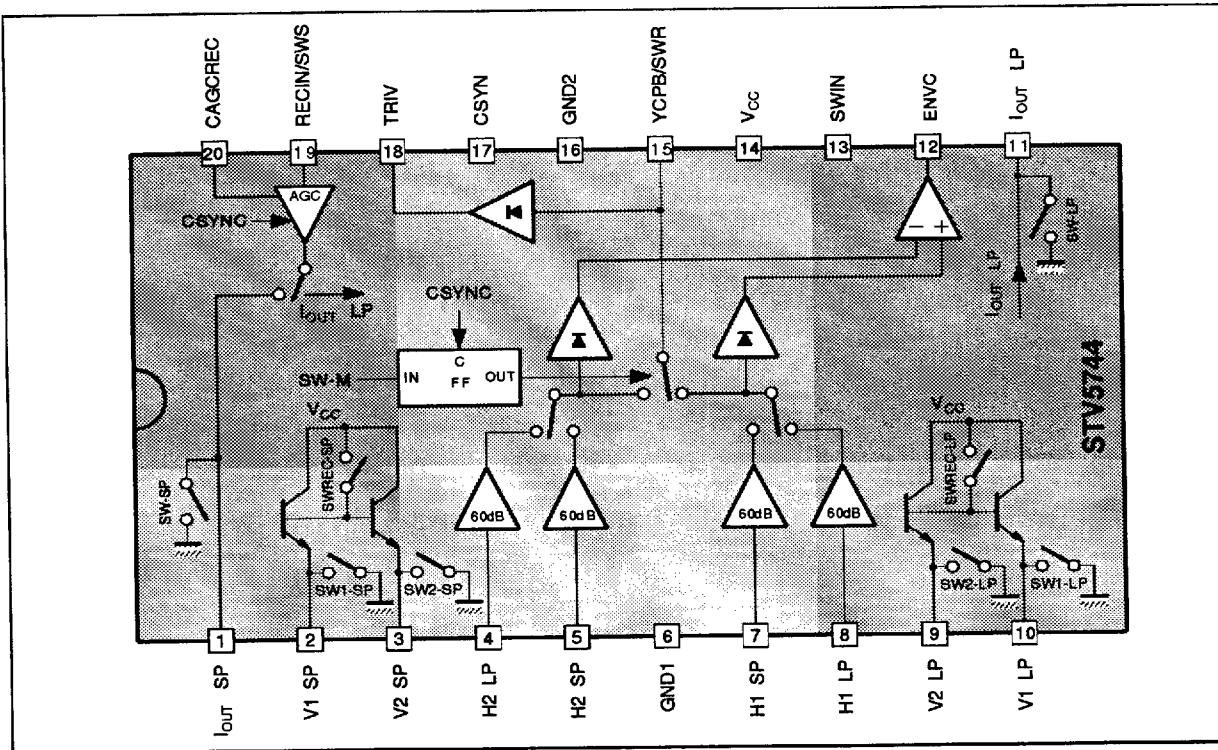
ORDER CODE : STV5744

PIN CONNECTIONS



5744-01.EPS

BLOCK DIAGRAM



5744-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{cc}	Power Supply Voltage	6	V
T _j	Junction Temperature	150	°C
T _{oper}	Operating Temperature	0, +70	°C

5744-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th (j-a)}	Junction-ambient Thermal Resistance	Max. 75	°C/W

5744-02.TBL

RECOMMENDED OPERATING CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{cc}	Power Supply	4.75	5	5.25	V
CAGC	Capacitance on Pin CAGCREC	4.7			nF
RECADJ	Record Biasing Resistor	10		33	kΩ

5744-03.TBL

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified)**Playback Mode** ($V_{CC} = 5\text{V}$, no load on Pin YCPB, Recadj = $12\text{k}\Omega$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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PLAYBACK AMPLIFIER

I_{CC1}	Supply Current		42	52	62	mA
GPB	Playback Gain	Sinewave 600kHz, 0.4mV _{PP} on inputs	58	60	62	dB
EN	Equivalent Voltage Noise	Input grounded via I _{OUT} Pin @ 600kHz, BW = 10kHz		0.6	0.7	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
IN	Equivalent Input Current Noise	Input open @ 6MHz, BW = 10kHz		1.7		$\frac{\text{pA}}{\sqrt{\text{Hz}}}$
CRT1	Crosstalk (LP → SP)	Sinewave @ 4MHz, 0.4mV _{PP}		-45	-40	dB
CRT2	Crosstalk (SP → LP)	Sinewave @ 4MHz, 0.4mV _{PP}		-41	-35	dB
RPBSW	Playback Switch on Resistor	@ 6MHz	5	10	15	Ω
BWLCF	Attenuation @ 100KHz	Reference level @ 600kHz	-3	-2	1	dB
BWHCF	Attenuation @ 8MHz	Reference level @ 4MHz	-3	-1	0	dB
C _{IN}	Input Capacitance	@ 6MHz, 22nF between Vi/Hi	40	50	60	pF
Z _{IN}	Input Impedance	@ 6MHz	300	450	600	Ω
ZCPB	Output Resistance	DC	5	24	50	Ω
VDCPB1	DC Level on Pin YCPB		1.6	2	2.4	V
DVDC	Head Switch Offset		-0.2	0	0.2	V
SHPB1	2nd Harmonic	Sinewave @ 4MHz, 0.4mV _{PP}		-45	-40	dB
RCST	Off-resistance on unused channel	SW-S high	10	15	20	Ω

TRIV FUNCTION

TRIV0	Output Level (1)	No input signal	0	0.3	1	V
TRIV1	Output Level (2)	Sinewave @ 4MHz, 100mV _{PP} @ YCPB		1.3		V
TRIV4	Output Level (3)	Sinewave @ 4MHz, 400mV _{PP} @ YCPB	2.5	3.1	3.5	V
TRIV6	Output Level (4)	Sinewave @ 4MHz, 600mV _{PP} @ YCPB	3.15	3.65	4.15	V
TRIV1 - TRIV0			0.5	1		V

SP/LP ENVELOPE DETECTOR

VENVCH	Output Level		4	4.5	5	V
VENVCL	Output Level		0	0.3	1	V
SENS1	Sensitivity	50 μV_{PP} to 600 μV_{PP} @ SP input pins		0.3	1	V
SENS2	Sensitivity	50 μV_{PP} to 600 μV_{PP} @ LP input pins	4	4.5		V

5744-04 TBL

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified (continued))

Record Mode ($V_{CC} = 5\text{V}$, $\text{Recadj} = 12\text{k}\Omega$, $\text{SWR} = 5\text{V}$, $\text{CAGCREC} = 470\text{pF}$, $\text{RRCY} = 2.2\text{k}\Omega$, $\text{RRCC} = 8.2\text{k}\Omega$, Load $10\mu\text{H}/1\text{k}\Omega$ for each simulated head)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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RECORD AMPLIFIER

I _{CC2}	Current Supply		68	91	115	mA
I _{HA0}	DC Current through I _{OUT}		24	33	41	mA
I _{HA1}	Fundamental	V _{RCY} = 300mV _{PP} @ 4MHz	30	32	34	mA _{PP}
I _{HA2}	2nd Harmonic	V _{RCY} = 300mV _{PP} @ 4MHz		-40	-36	dB
I _{HA2M}	2nd Harmonic	V _{RCY} = 400mV _{PP} @ 4MHz, AGC adjusted for I _{HA1} = 40mA _{PP}			-34	dB
BWRECL	Attenuation at 100kHz	Reference level @ 600kHz, AGC locked	-3	0	1	dB
BWRECH	Attenuation at 8MHz	Reference level @ 4MHz, AGC locked	-2	-0.5	1	dB
DVLREC	Record AGC Sensitivity	V _{IN} = 300mV _{PP} $\pm 3\text{dB}$ @ f = 4MHz	-0.2	0	+0.2	dB
R _{IOUT}	Output Resistance	$\Delta V = 5\text{V}$	3.5	5.5		k Ω
R _{SAT}	Output Stage Resistance	$\Delta I = 10\text{mA}$	5	10	50	Ω
I _{RN}	AGC Capacitor downloading Current	4.5V at CAGC Pin		160		μA
I _{RP}	AGC Capacitor uploading Current	0.5V at CAGC Pin, V _{IN} = 300mV _{PP} @ 4MHz		-165		μA

SWITCHING LEVELS

V _{SWINL}	SWIN Input Voltage	Selects head H2SP	0		0.8	V
V _{SWIN1}	SWIN Input Voltage	Selects head H1SP	1.3		2.3	V
V _{SWIN2}	SWIN Input Voltage	Selects head H1LP	2.8		3.8	V
V _{SWINH}	SWIN Input Voltage	Selects head H2LP	4.3		5	V
I _{SWINH}	SWIN Input Leakage Current	5V at SWIN input		0.5		μA
I _{SWINL}	SWIN Input Leakage Current	0V at SWIN input		-0.2		μA
V _{SWRCH}	SWRC Input Threshold	Selects record mode, 0 to 5V	3.2	3.4	3.8	V
V _{SWRCL}	SWRC Input Threshold	Selects playback mode, 5 to 0V	3.1	3.35	3.8	V
I _{SWRCH}	SWRC Input Leakage Current	5V at SWRC input	2	5	8	mA
I _{SWRCL}	SWRC Input Leakage Current	0V at SWRC input	-20	0	20	μA
t _{ON}	Delay	Signal appears on YCPB		1.6		ms
t ₁	Delay from playback to record : Signal disappears on Pin YCPB	22nF between Hi/Vi		1		μs
t ₂	Delay from record to playback : Signal appears on Pin YCPB			1.9		ms
t ₃	Delay from playback to record : Signal appears on Pin I _{OUT}	V _{RCY} = 300mV _{PP} @ 4MHz		2		ms
t ₄	Delay from record to playback : Signal disappears on Pin I _{OUT}			10		μs
V _{CSYH}	CSYN Input Threshold	Sampling on (I = -25 μA)	2.2	2.5	2.8	V
V _{CSYL}	CSYN Input Threshold	Sampling off (I = 25 μA)	2.2	2.5	2.8	V
I _{CSYH}	Leakage Current	Sampling on			-10	μA
I _{CSYL}	Leakage Current	Sampling off	10			μA
V _{SWST}	SWS Input Threshold			3		V
I _{SWSH}	SWS Input Leakage Current	5V at SWS Input	90	130	170	μA
I _{SWSL}	SWS Input Leakage Current	0V at SWS Input	-20	0	20	μA

5744-05.TBL

INTERNAL SCHEMATICS

Figure 1

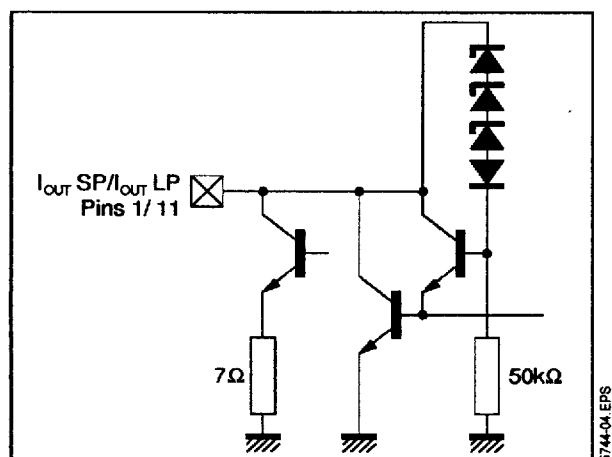


Figure 2

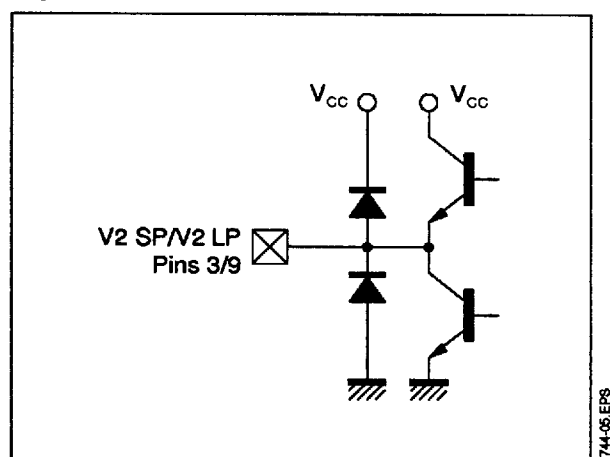


Figure 3

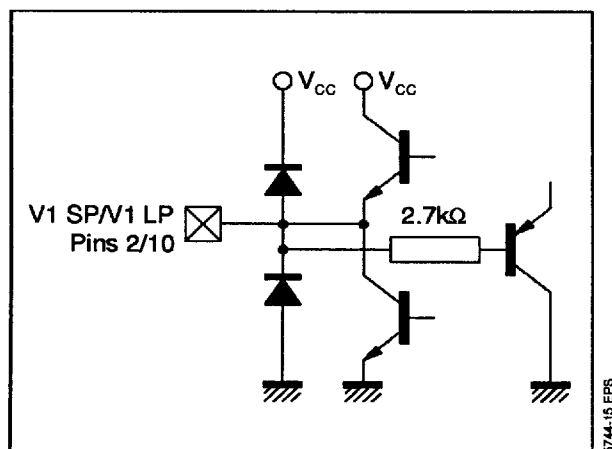


Figure 4

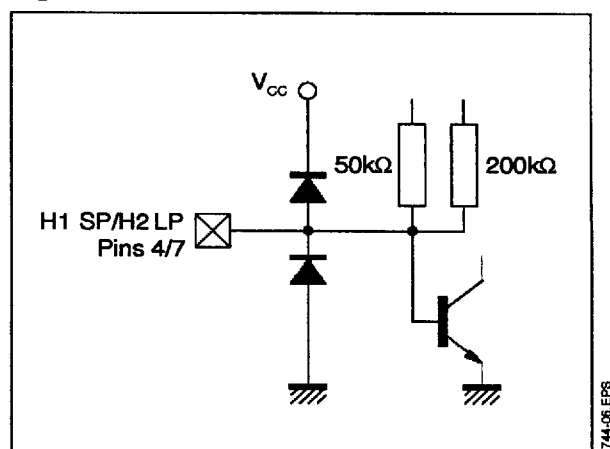


Figure 5

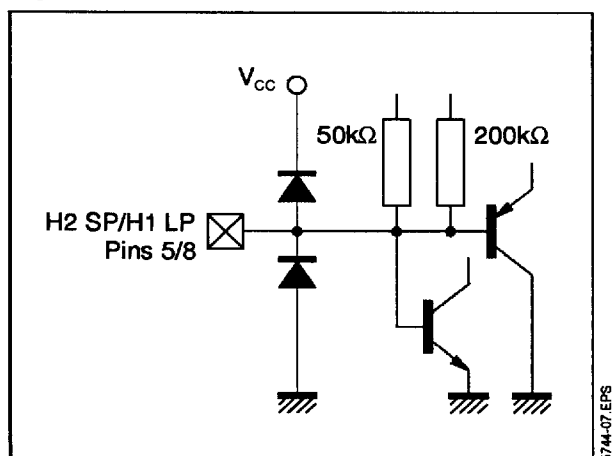
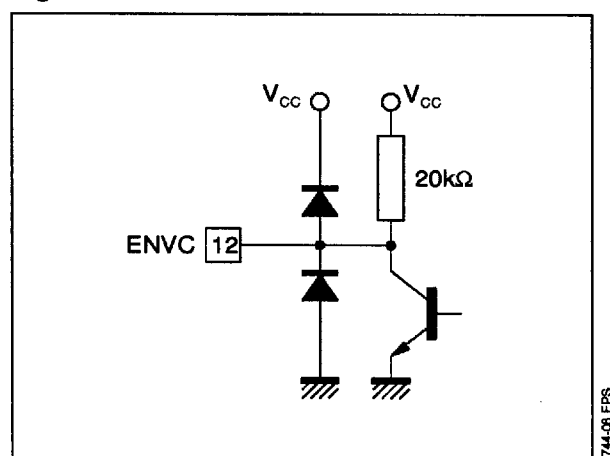
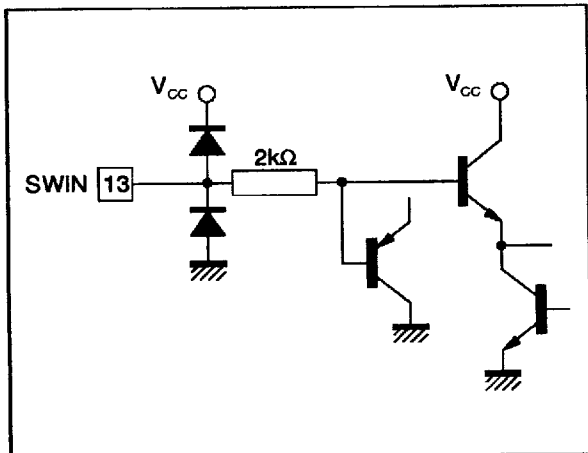


Figure 6



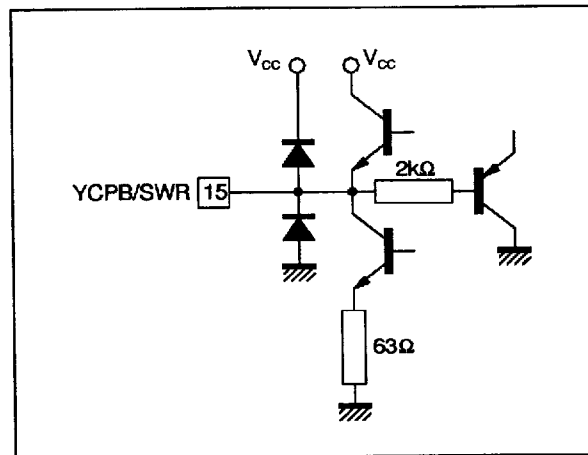
INTERNAL SCHEMATICS (Continued)

Figure 7



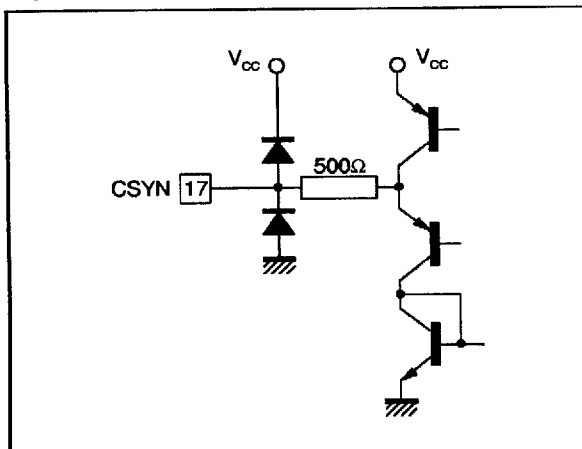
5744-08.EPS

Figure 8



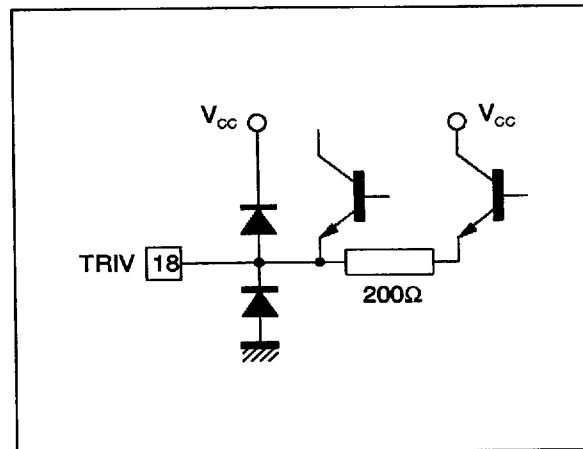
5744-10.EPS

Figure 9



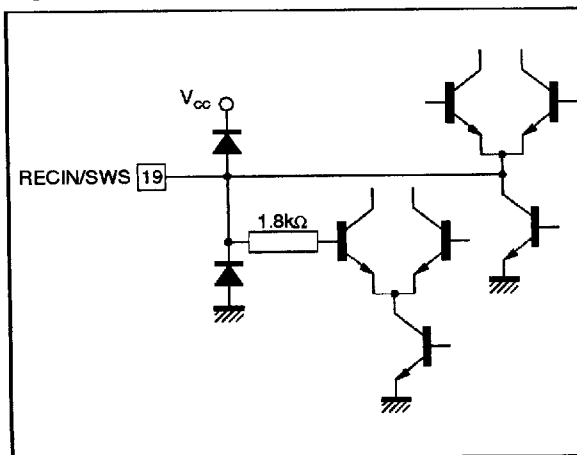
5744-11.EPS

Figure 10



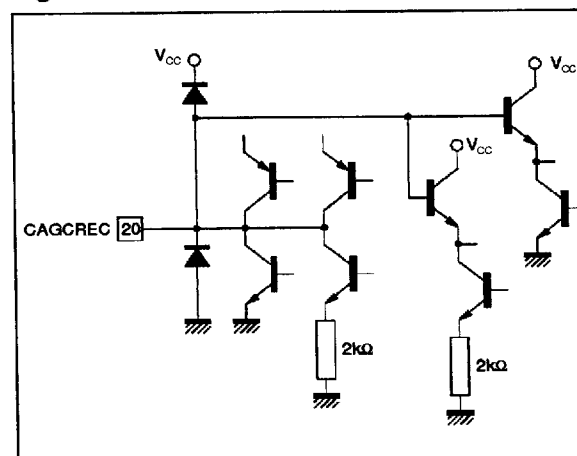
5744-12.EPS

Figure 11



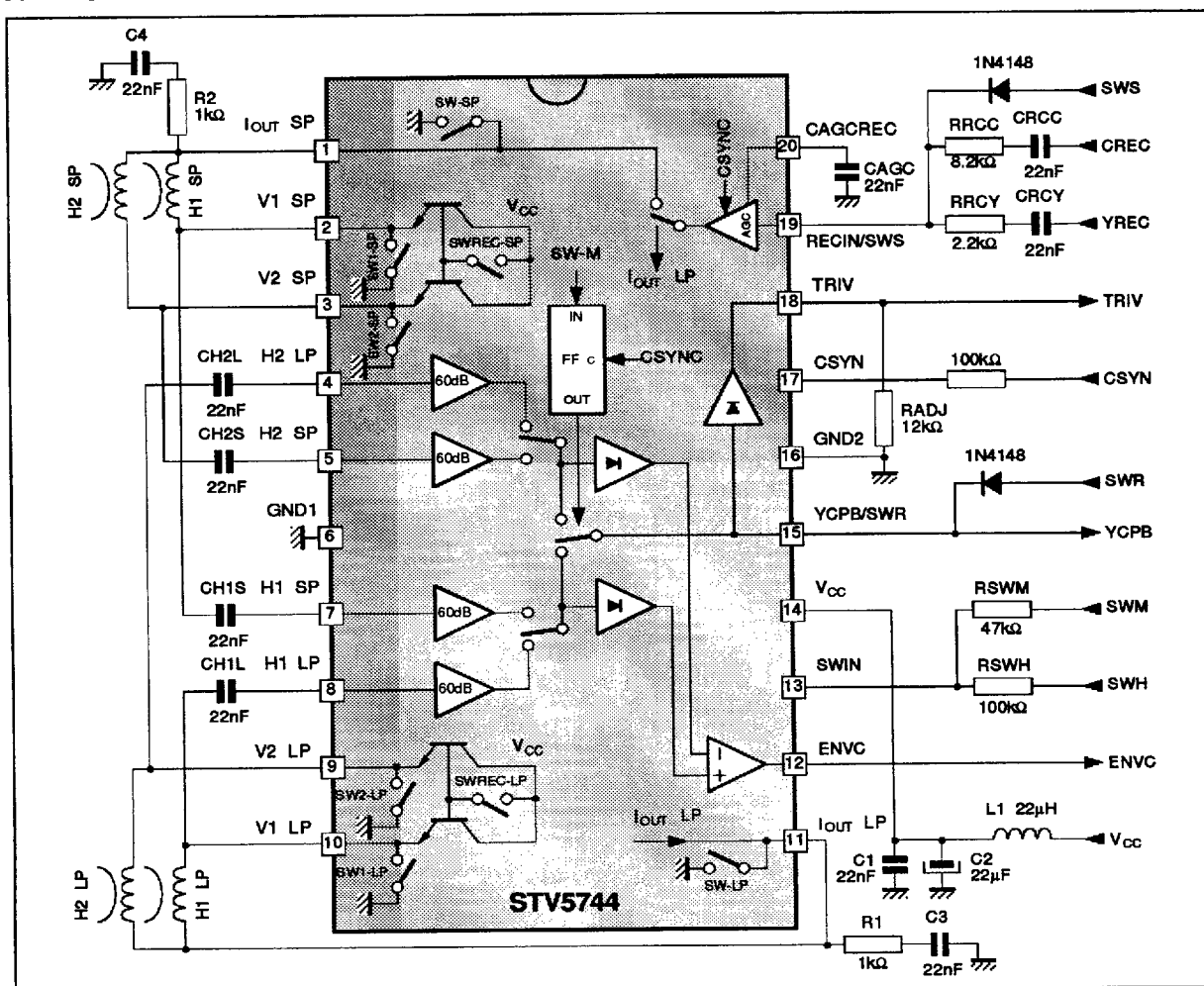
5744-13.EPS

Figure 12



5744-14.EPS

APPLICATION DIAGRAM

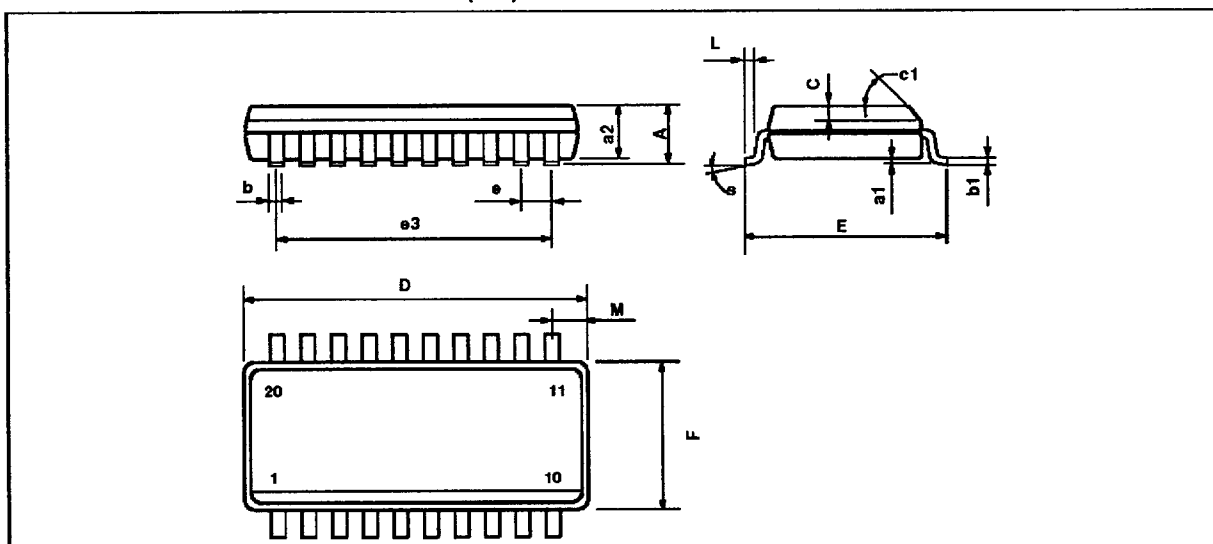


5744-08 EPS

SWITCH TABLE

SW-R	SW-M	SW-S	SW-H	Channel	SW1-SP SW2-SP	SW1-LP SW2-LP	SW-SP	SW-LP	SWREC-SP	SWREC-LP	ENVC (SPLP)
L	L	L	L	2-SP	OFF	OFF	ON	ON	OFF	OFF	High IF LP > SP Low IF LP < SP
			H	1-SP							
	H		L	1-LP							
			H	2-LP							
		L	L	2-SP	OFF	ON					
			H	1-SP							
	H		L	1-LP	ON	OFF					
			H	2-LP							
H	L	L	L	SP	OFF	ON	OFF	ON	ON	OFF	High
			H								
	H		L	LP	ON	OFF	ON	OFF	OFF	ON	
			H								

5744-06 TBL

PACKAGE MECHANICAL DATA
20 PINS - PLASTIC MICROPACKAGE (SO)


PM-SO20L EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

SO20L.TBL

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