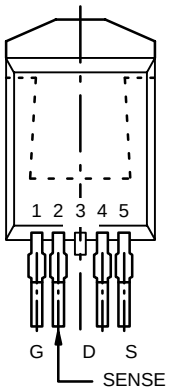
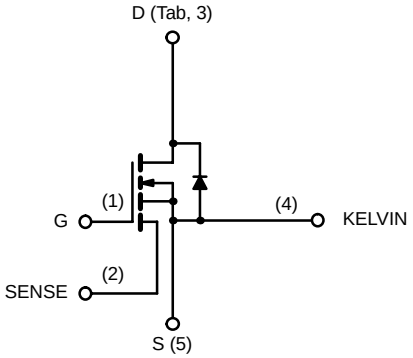
Current Sensing MOSFET, N-Channel 30-V (D-S)

PRODUCT SUMMARY		
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.015 @ V_{GS} = 10 V	50[a]
	0.02 @ V_{GS} = 4.5 V	48[a]

175°C Rated
Maximum Junction Temperature
TrenchFET®
Power MOSFETs

D^2PAK-5





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 175°C)	T_C = 25°C	I_D	50[a]	A
	T_C = 125°C		32[a]	
Pulsed Drain Current		I_{DM}	100	
Avalanche Current		I_{AR}	25	
Repetitive Avalanche Energy[b]	L = 0.1 mH	E_{AR}	31	mJ
Maximum Power Dissipation[b]	T_C = 25°C	P_D	83[c]	W
	T_A = 25°C		2.7[d]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 175	°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Limit**	**Unit**
Junction-to-Ambient	PCB Mount[d]	R_{thJA}	55	°C/W
Junction-to-Case		R_{thJC}	1.8	

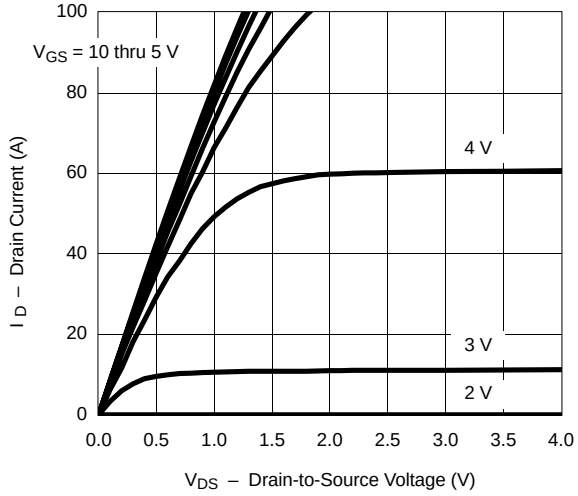
Notes
a. Package limited.
b. Duty cycle ≤ 1%.
c. See SOA curve for voltage derating.
d. When mounted on 1" square PCB (FR-4 material).

MOSFET SPECIFICATIONS (T_J =25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_{DS} = 250 µA	1		3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 125°C			50	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 175°C			150	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	50			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 25 A		0.012	0.015	Ω
		V_{GS} = 10 V, I_D = 25 A, T_J = 125°C		0.019	0.024	
		V_{GS} = 10 V, I_D = 25 A, T_J = 175°C		0.022	0.027	
		V_{GS} = 4.5 V, I_D = 24 A		0.016	0.02	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 25 A	30			S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		1960		pF
Output Capacitance	C_{oss}			380		
Reversen Transfer Capacitance	C_{rss}			180		
Total Gate Charge[c]	Q_g	V_{DS} = 15 V, V_{GS} = 20 V, I_D = 50 A		35	50	nC
Gate-Source Charge[c]	Q_{gs}			7.6		
Gate-Drain Charge[c]	Q_{gd}			5.6		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 15 V, R_L = 0.3 Ω I_D ≃ 50 A, V_{GEN} = 10 V, R_G = 2.5 Ω		10	20	ns
Rise Time[c]	t_r			93	180	
Turn-Off Delay Time[c]	$t_{d(off)}$			30	60	
Fall Time[c]	t_f			10	20	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)[b]						
Continuous Current	I_S				50	A
Pulsed Current	I_{SM}				100	
Forward Voltage[a]	V_{SD}	I_F = 50 A, V_{GS} = 0 V		1.3	1.6	V
Reverse Recovery Time	t_{rr}	I_F = 50 A, di/dt = 100 A/µs		35	70	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			1.5		A
Reverse Recovery Charge	Q_{rr}			0.026		µC
Current Sense Characteristics						
Current Sensing Ratio	r	I_D = 1 A, V_{GSS} = 10 V, R_{SENSE} = 2.2 Ω	420	520	620	
Mirror Active Resistance	$r_{m(on)}$	V_{GS} = 10 V, I_D = 10 mA		3.5		Ω

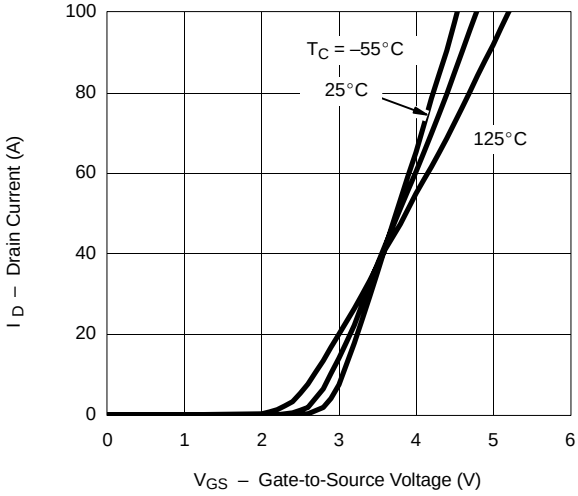
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
e. Guaranteed by design, not subject to production testing.
b. Independent of operating temperature.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

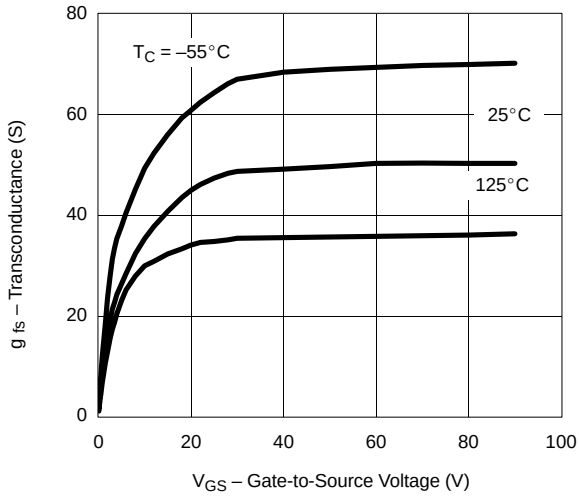
Output Characteristics



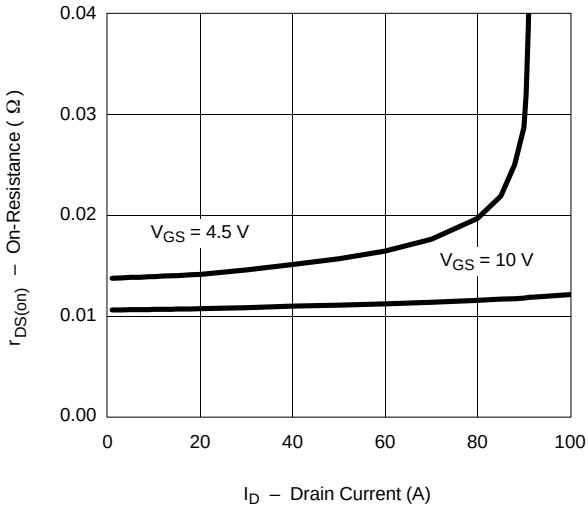
Transfer Characteristics



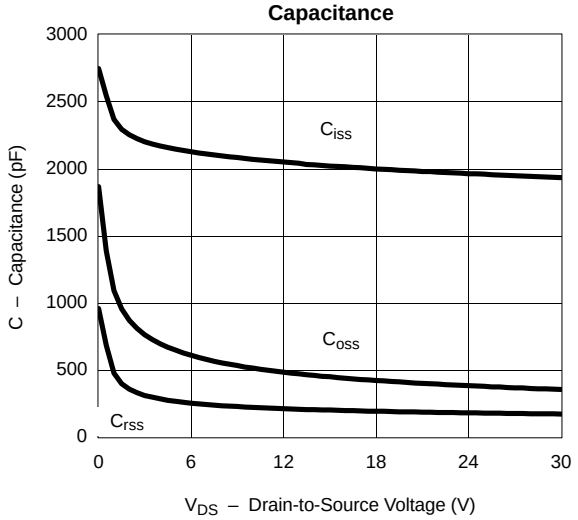
Transconductance



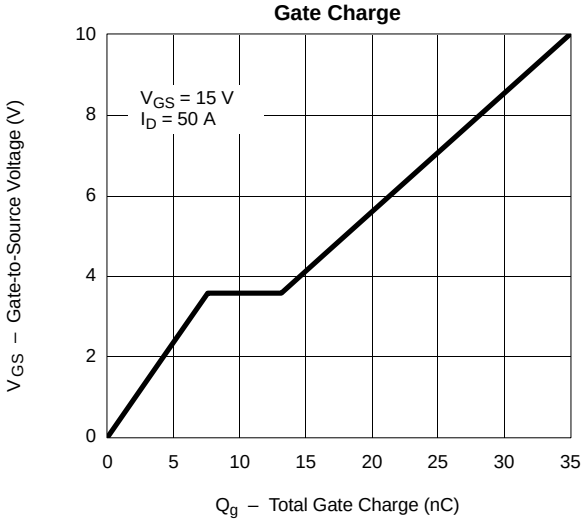
On-Resistance vs. Drain Current



Capacitance

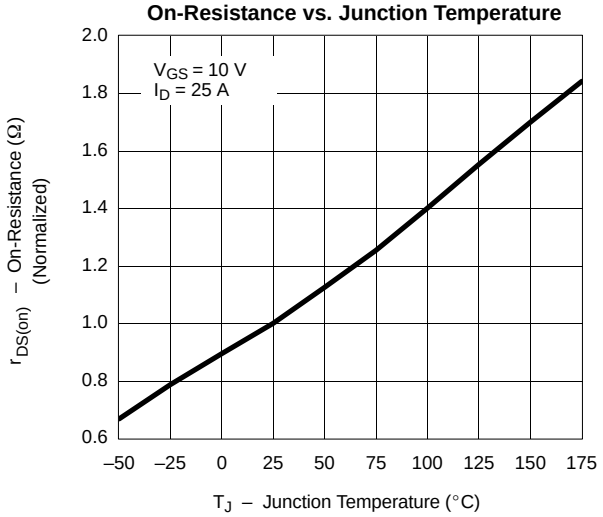


Gate Charge

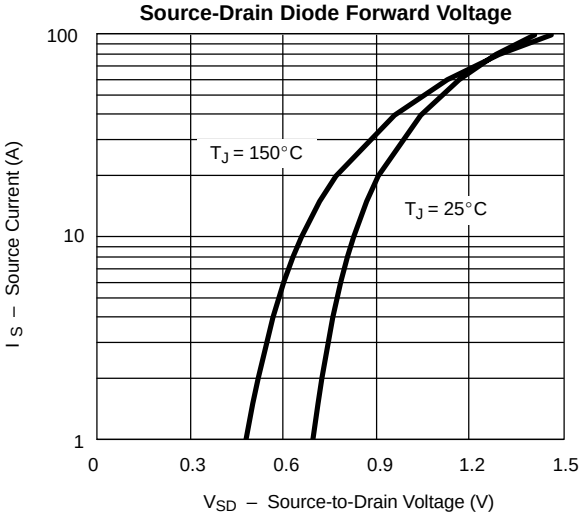


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

On-Resistance vs. Junction Temperature

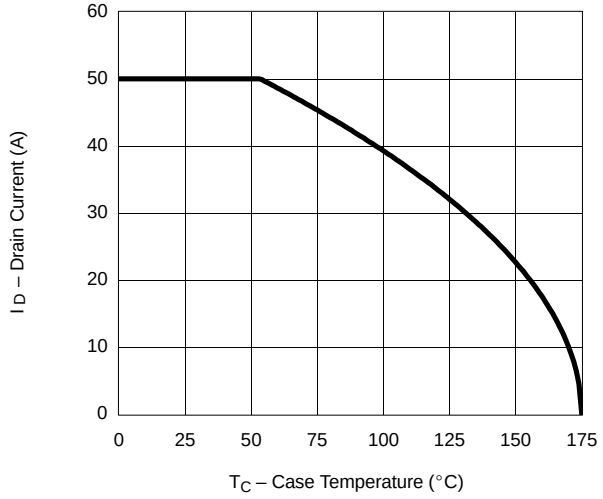


Source-Drain Diode Forward Voltage

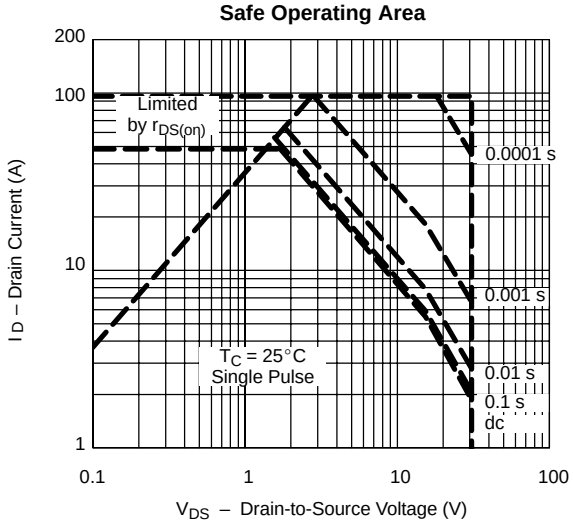


THERMAL RATINGS

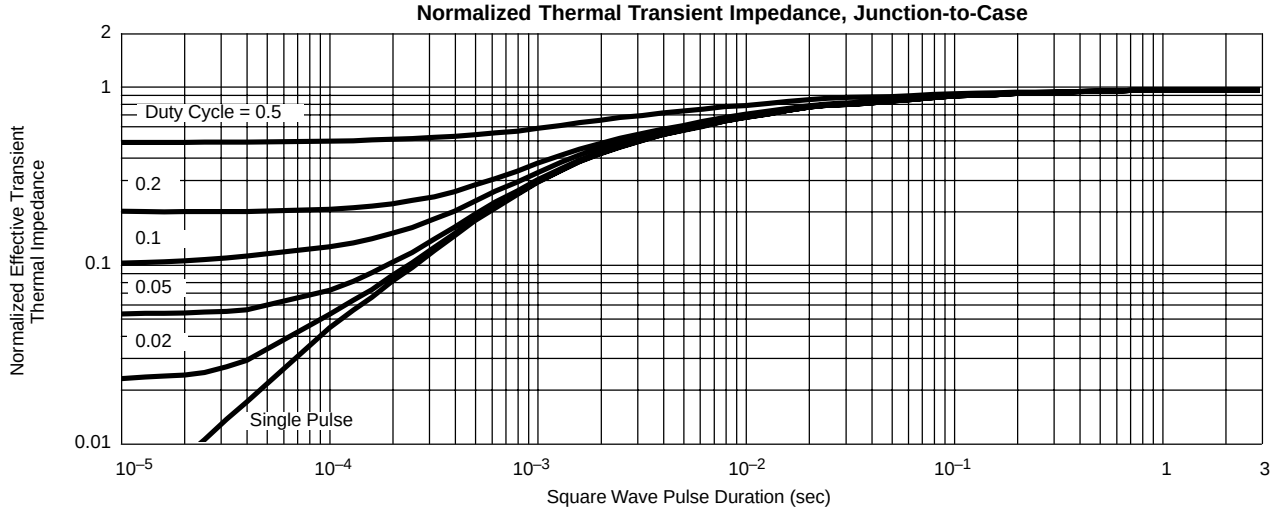
Maximum Drain Current vs. Case Temperature



Safe Operating Area

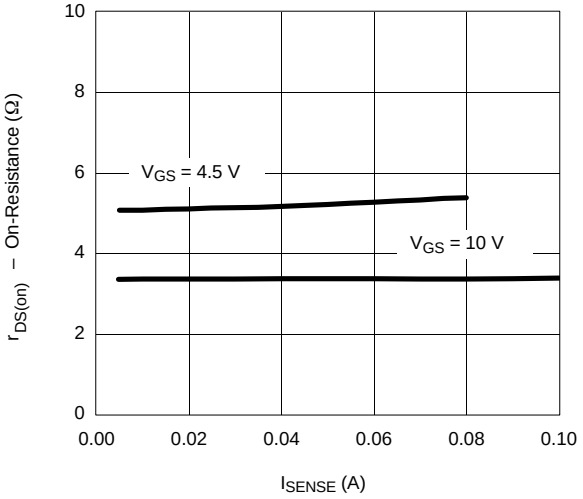


Normalized Thermal Transient Impedance, Junction-to-Case

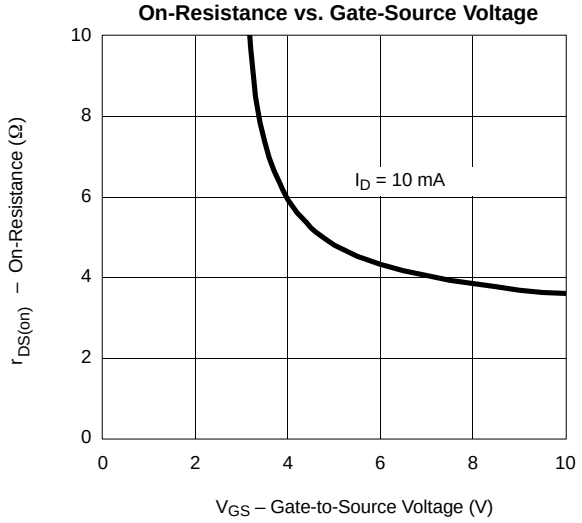


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) SENSE DIE

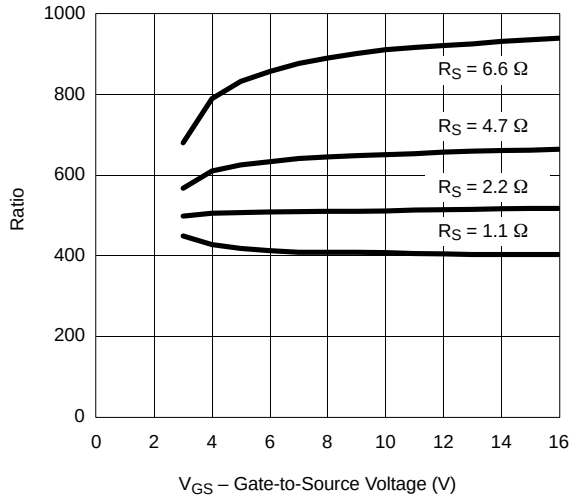
On-Resistance vs. Sense Current



On-Resistance vs. Gate-Source Voltage



Current Ratio ($I_{(MAIN)/IS}$) vs. Gate-Source Voltage (Figure 1)



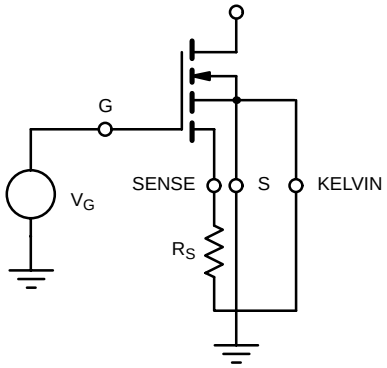


Figure 1