N-Channel 40-V (D-S) 175°C MOSFET

CHARACTERISTICS

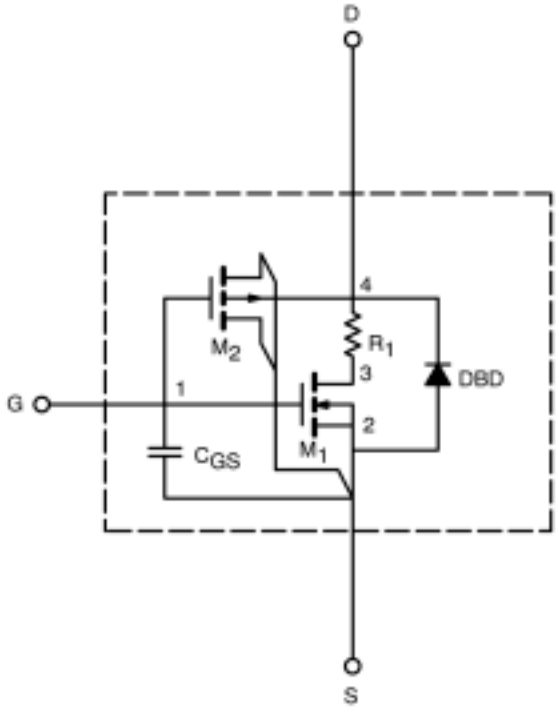
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the –55 to 125°C temperature ranges under the pulsed 0-to-10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.9		V
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	1410		A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10V, I_D = 30A	0.0026	0.0029	Ω
		V_{GS} = 4.5V, I_D = 20A	0.0040	0.0044	
		V_{GS} = 10V, I_D = 30A, T_J = 125°C	0.0037		
		V_{GS} = 10V, I_D = 30A, ,T_J = 175°C	0.0043		
Forward Transconductance[a]	g_{fs}	V_{DS} = 15V, I_D = 30 A	87		S
Forward Voltage[a]	V_{SD}	I_S = 85A, V_{GS} = 0 V	0.92	1.1	V
Dynamic[b]					
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz	6809	6860	pf
Output Capacitance	C_{oss}		1347	1320	
Reverse Transfer Capacitance	C_{rss}		823	800	
Total Gate Charge[b]	Q_g	V_{DS} = 30V, V_{GS} = 10V, I_D = 85A	165	165	nC
Gate-Source Charge[b]	Q_{gs}		25	25	
Gate-Drain Charge[b]	Q_{gd}		55	55	
Turn-On Delay Time[b]	$t_{d(on)}$	V_{DD} = 30V, R_L = 0.35Ω I_D ≅ 85A, V_{GEN} = 10V, R_G = 2.5 Ω	57	15	ns
Rise Time[b]	t_r		103	90	
Turn-Off Delay Time[b]	$t_{d(off)}$		120	95	
Fall Time[b]	t_f		193	125	
Reverse Recovery Time	t_{rr}	I_F = 85A, di/dt = 100 A/µs	65	60	

Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°c UNLESS OTHERWISE NOTED)