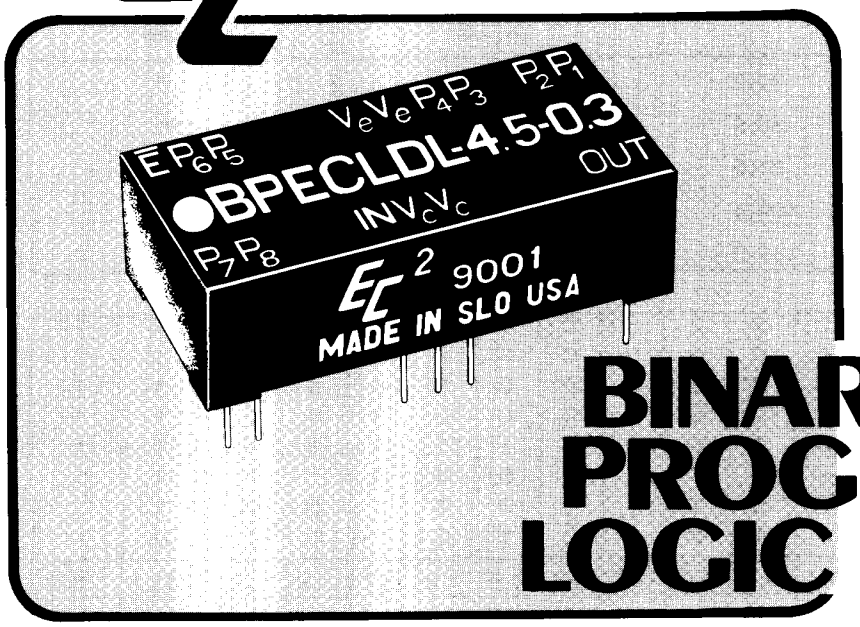


ECL 100K COMPATIBLE 8-BIT BINARY/DECADE PROGRAMMABLE LOGIC DELAY LINE

- **ECL 100K input and output levels**
- **Delays stable and precise**
- **34-pin DIP package (.375 high)**
- **Available in delays up to 132ns**
- **Available in Binary and Decade versions**
- **Step resolution from 0.1 to 0.5ns**
- **Propagation delays fully compensated**
- **All delays digitally programmable**
- **70 ECL DC fan-out capacity**

design notes

The "DIP Series" of Programmable Logic Delay Lines developed by Engineered Components Company have been designed to allow for final delay adjustment during or after installation in a circuit. These Logic Delay Lines incorporate required driving and pick-off circuitry and are contained in a 34-pin DIP package compatible with ECL "100K Series" circuits. The design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the required delay.

The Logic Delay Lines are digitally programmable by the presence of either a "1" or a "0" at each of the programming pins. Since the input and the output terminals are fixed and the programming is accomplished only by DC voltage levels, programming may be accomplished by remote switching or permanent termination of the appropriate programming pins of the Logic Delay Line to Vcc; the Logic Delay Line may also be programmed automatically by computer generated data. MUX set-up time is 1ns maximum. When no need exists in the application to change delay time during normal use, the desired delay is most conveniently established by use of a Vcc pad around each programming pin; programming is accomplished by cutting off those pins which are to remain at state "0" before insertion of the Logic Delay Line into the printed circuit board.

Both the BPECLDL and the DPECLDL are designed for use with positive input pulses and will reproduce these at the output without inversion. All modules can be driven from a standard ECL gate with an external pulldown resistor of 50 or 100 ohms to −2V or 470 ohms to −4.5V. Output is standard ECL 100K open emitter; programming inputs are standard ECL 100K single fan-in. These Logic Delay Lines have the capability of driving up to 70 ECL DC loads.

engineered components company
3580 Sacramento Drive, P. O. Box 8121, San Luis Obispo, CA 93403-8121
Phone: (805) 544-3800

DESIGN NOTES (continued)

These modules are offered in Binary and Decade models with time delays to a maximum of 132ns and with step resolution as shown in the Part Number Table. Programming of maximum delays is accomplished in 256 delay steps in accordance with the Truth Table Examples shown on page 3. Tolerances on minimum delay and deviation from programmed delay are shown in the Part Number Table on page 3.

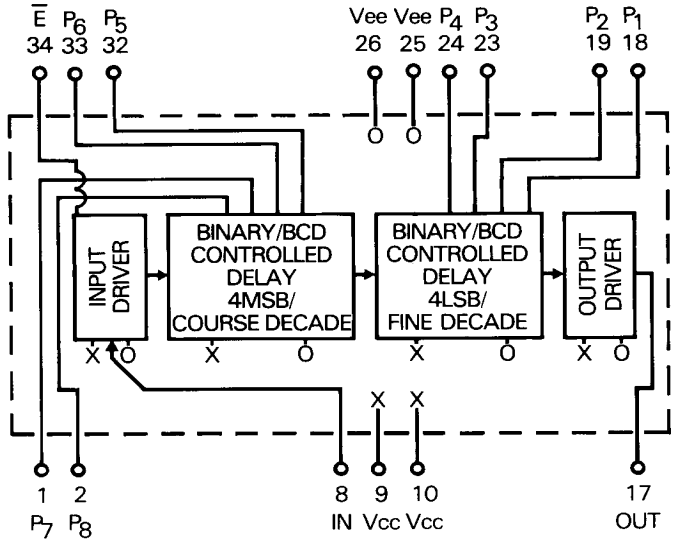
Rise time for all Logic Delay Lines is 2ns maximum, when measured from 20% to 80% pulse amplitude. Temperature coefficient of delay is less than 150 ppm/°C over the operating temperature range of 0 to +85°C.

These modules are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are burned-in to level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 500,000 hours.

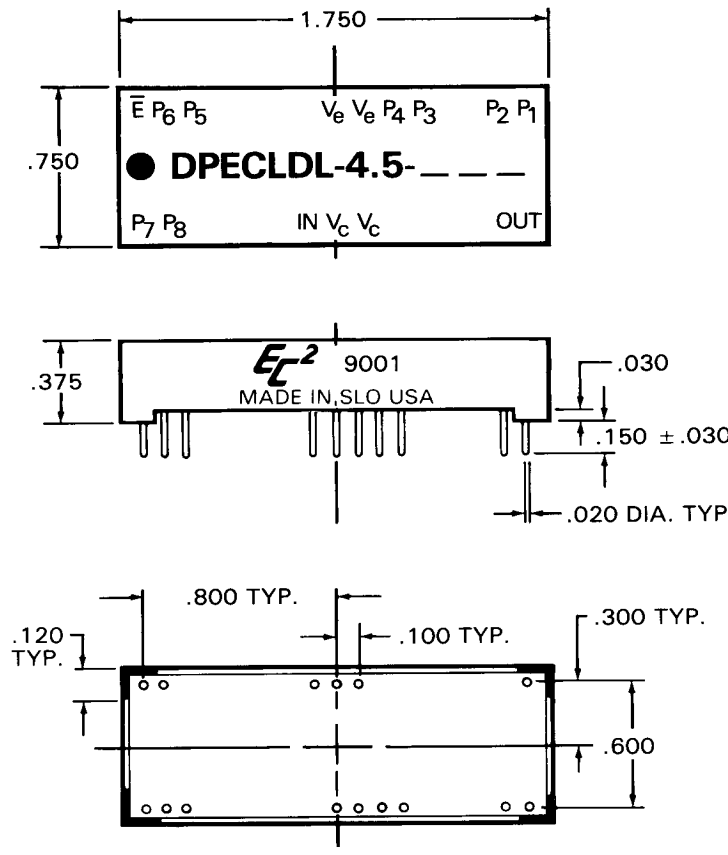
The "DIP Series" Programmable Logic Delay Lines are packaged in a 34-pin DIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, Type SDG-F, and are fully encapsulated in epoxy resin. Leads meet the solderability requirements of MIL-STD-202, Method 208. Corner standoffs on the housing provide positive standoff from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

Marking consists of manufacturer's name, logo (EC^2), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



TEST CONDITIONS

1. All measurements are made at 25°C.
2. Vee supply voltage is maintained at −4.5V DC.
3. All units are tested using a positive input pulse provided by a standard open emitter ECL 100K gate. The input and output utilize a 50 ohm pulldown risistor to −2V; the output is also loaded with one ECL 100K gate.

ø4. Input pulse width used is 100ns. Pulse period for all units is1000ns.

OPERATING SPECIFICATIONS

Supply Voltage:	−4.2 to −4.8 to Vee
Supply Current:	200ma typical
Logic 1 input at 25°C.	
Voltage	−1.165V min.
Current	350ua max.
Logic 0 input at 25°C.	
Voltage	−1.475V max.
Current	.5ua min.
Logic 1 Output at 25°C.	−1.025V min.
Logic 0 Output at 25°C.	−1.620V max.
Operating temperature range:	0 to +85°C.
Storage temperature:	−55 to+125°C.

PART NUMBER TABLE

BINARY	ϕ DELAYS AND TOLERANCES (in ns)		
Part Number	*Step Zero Delay Time	Maximum Delay Time (Nom)	* *Maximum Deviaton From Programmed Delay (4LSB)	* *Maximum Deviation From Programmed Delay (4MSB)
BPECLDL-4.5-0.1	4.5 ±.3	30.0	±.04	±1.0
BPECLDL-4.5-0.2	4.5 ±.3	55.5	±.05	±2.0
BPECLDL-4.5-0.3	4.5 ±.3	81.0	±.10	±4.0
BPECLDL-4.5-0.4	4.5 ±.3	106.5	±.10	±5.0
BPECLDL-4.5-0.5	4.5 ±.3	132.0	±.15	±6.0

TRUTH TABLE EXAMPLES

Programming Pins / Part Number																	
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1
2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
BPECLDL-4.5-0.1	4.5	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2	1.3	25.4	25.5	
BPECLDL-4.5-0.2	4.5	0.2	0.4	0.6	0.8	1.0	1.2	1.4	1.6	1.8	2.0	2.2	2.4	2.6	50.8	51.0	
BPECLDL-4.5-0.3	4.5	0.3	0.6	0.9	1.2	1.5	1.8	2.1	2.4	2.7	3.0	3.3	3.6	3.9	76.2	76.5	
BPECLDL-4.5-0.4	4.5	0.4	0.8	1.2	1.6	2.0	2.4	2.8	3.2	3.6	4.0	4.4	4.8	5.2	101.6	102.0	
BPECLDL-4.5-0.5	4.5	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	127.0	127.5	

PART NUMBER TABLE

DECADE	ϕ DELAYS AND TOLERANCES (in ns)		
Part Number	*Step Zero Delay Time	Maximum Delay Time (Nom)	* *Maximum Deviaton From Programmed Delay (Fine Decade)	* *Maximum Deviation From Programmed Delay (Course Decade)
DPECLDL-4.5-0.1	4.5 ±.3	14.4	±.04	±0.5
DPECLDL-4.5-0.2	4.5 ±.3	24.3	±.05	±1.0
DPECLDL-4.5-0.3	4.5 ±.3	34.2	±.10	±1.5
DPECLDL-4.5-0.4	4.5 ±.3	44.1	±.10	±2.0
DPECLDL-4.5-0.5	4.5 ±.3	54.0	±.15	±2.5

TRUTH TABLE EXAMPLES

Programming Pins / Part Number																	
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
4	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1
3	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
2	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	0
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
DPECLDL-4.5-0.1	4.5	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2	1.3	9.8	9.9	
DPECLDL-4.5-0.2	4.5	0.2	0.4	0.6	0.8	1.0	1.2	1.4	1.6	1.8	2.0	2.2	2.4	2.6	19.6	19.8	
DPECLDL-4.5-0.3	4.5	0.3	0.6	0.9	1.2	1.5	1.8	2.1	2.4	2.7	3.0	3.3	3.6	3.9	29.4	29.7	
DPECLDL-4.5-0.4	4.5	0.4	0.8	1.2	1.6	2.0	2.4	2.8	3.2	3.6	4.0	4.4	4.8	5.2	39.2	39.6	
DPECLDL-4.5-0.5	4.5	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.5	49.0	49.5	

* Delay at step zero is referenced to the input pin.

** All delay times after step zero are referenced to step zero.

ϕ All modules can be operated with a minimum input pulse width of 20% of full delay, and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified delay times for specific applications.