256k (32k × 8) Bit SRAM

BR62256F-70LL

The BR62256F-70LL is a 32768 word × 8 bit asynchronous high-speed CMOS static RAM. It runs on a 5V single power supply, and in addition to its low power consumption and high-speed, its low standby current enables its use in battery backup applications.

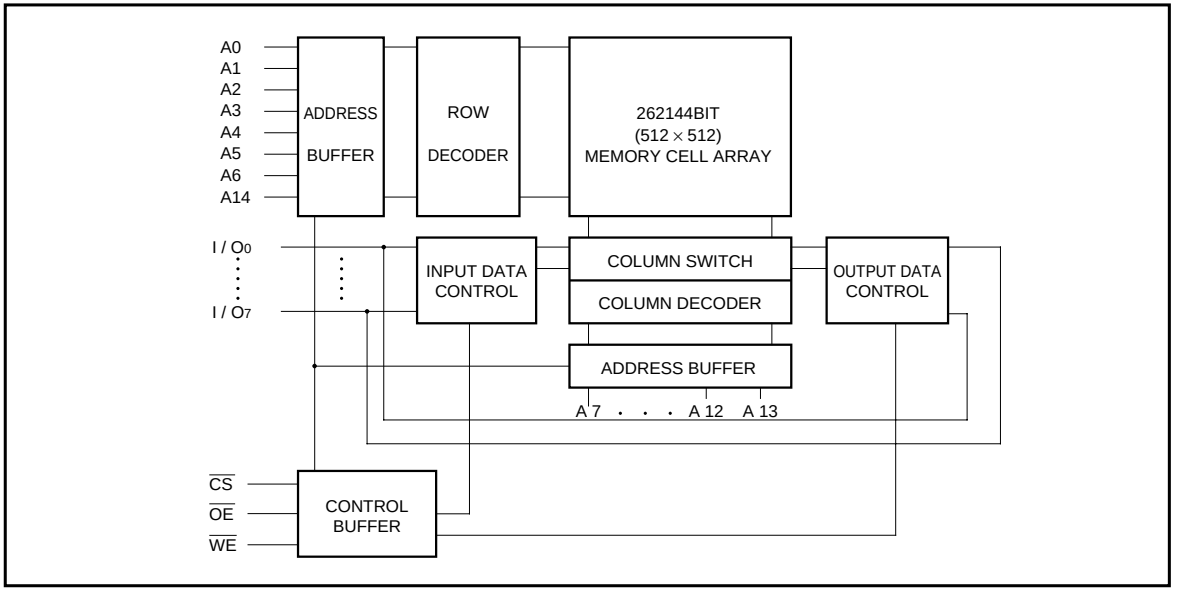
●Applications

General-purpose

●Features

1) SRAM with a 32768 word × 8 bit configuration.
2) High speed read access time of 70ns maximum (Ta = 0 to 70°C).
3) Battery backup is possible.
   Standby current: 50µA max. (Ta = 0 to 70°C)
   Data holding current: 3µA max. (Ta = 0 to 70°C)
4) 5V single power supply voltage with ± 10% fluctuation tolerance.
5) Input / output TTL compatible.
6) Common input / output pin with three output statuses.
7) No clock is necessary (asynchronous static circuit).
8) Input and output data are in the same phase.
9) Low power consumption.

●Block diagram



●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	V_{CC}	– 0.5*1 ~ + 7.0	V
Power dissipation	Pd	850*2	mW
Storage temperature	Tstg	– 55 ~ + 125	°C
Operating temperature	Topr	0 ~ + 70	°C
I / O voltage	VI / O	– 0.5 ~ V_{CC} + 0.5	V
Input voltage	V_{IN}	– 0.5 ~ V_{CC} + 0.5	V

*1 At pulse width of 50ns: – 3.0V (min.)

*2 Reduced by 8.5mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high level voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input low level voltage	V_{IL}	– 0.3	—	0.8	V
Ambient temperature	Ta	0	—	70	°C

●Pin assignments

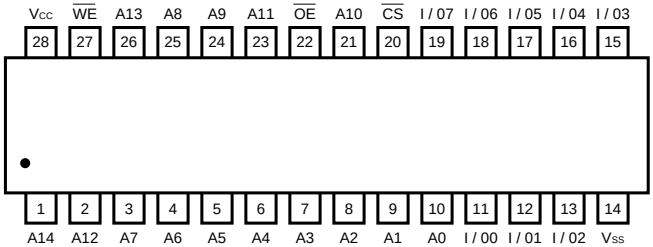


Fig.1

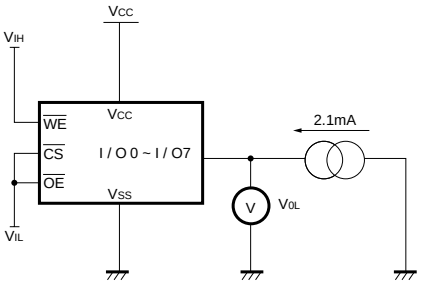
●Pin descriptions

Pin name	I / O	Function
V_{CC}	—	5V ± 10% power supply
V_{SS}	—	Reference voltage for all input / output, 0V
A0 ~ A14	I	32k memory address input
I / 00 ~ I / 07	I / O	8-bit data I / O
$\overline{CS}$	I	Chip segment control input
$\overline{OE}$	I	Output enable control input
$\overline{WE}$	I	Write enable control input

●Electrical characteristics (unless otherwise noted, Ta = 0 to + 70°C, V_{CC} = 5V ± 10%)

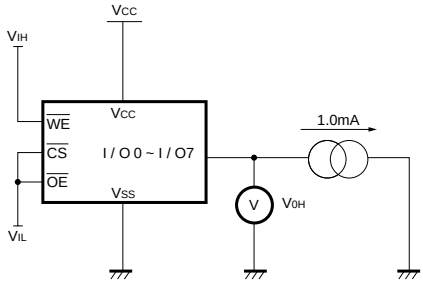
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Mesurement Circuit
Input low level voltage	V_{IL}	– 0.3	—	0.8	V	—	—
Input high level voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V	—	—
Output low level voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1mA	Fig.2
Output high level voltage	V_{OH}	2.4	—	—	V	I_{OH} = – 1.0mA	Fig.3
	V_{OH1}	$V_{CC} \times 0.8$	—	—	V	I_{OH} = – 0.1mA	Fig.3
Input leakage current	I_{LI}	– 1	—	+ 1	µA	V_{IN} = 0 ~ V_{CC}	Fig.4
Output leakage current	I_{LO}	– 1	—	+ 1	µA	$\overline{VI}$ / O = 0 ~ V_{CC} $\overline{CS}$ = V_{IH} or $\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL}	Fig.5
Average operating current	I_{CCA1}	—	—	45	mA	$\overline{CS}$ = V_{IL},I / O: OPEN, Min.cycle time	Fig.6
	I_{CCA2}	—	—	10	mA	$\overline{CS} \leqq$ 0.2V, f = 1MHz, I / O: OPEN $V_{IL} \leqq$ 0.2V, $V_{IH} \geqq V_{CC}$ – 0.2V	Fig.6
Standby current	I_{SB}	—	—	3	mA	$\overline{CS}$ = V_{IH}	—
	I_{SB1}	—	—	50	µA	$\overline{CS} \geqq V_{CC}$ – 0.2V	Fig.7

●Measurement circuits



Data sets all output to LOW (Data 00)

Fig.2



Data sets all output to HIGH (Data FF)

Fig.3

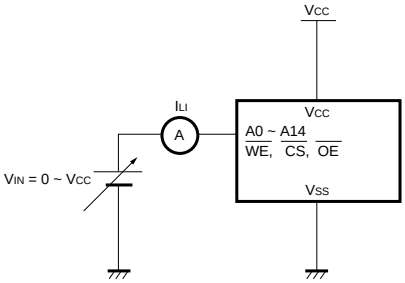


Fig.4

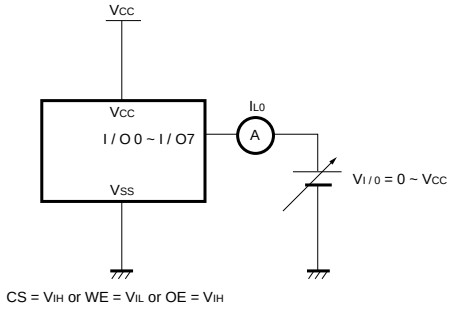
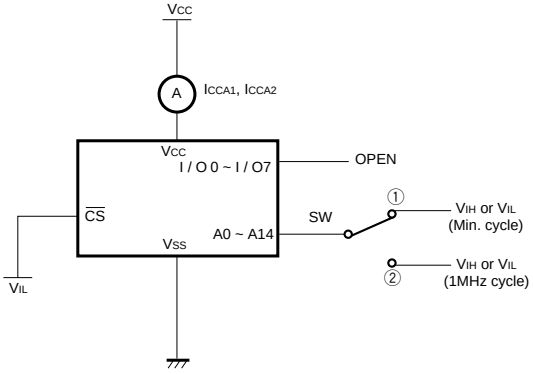


Fig.5



Sw ①: Average operating current I_{CCA1}

Sw ②: Average operating current I_{CCA2}

Fig.6

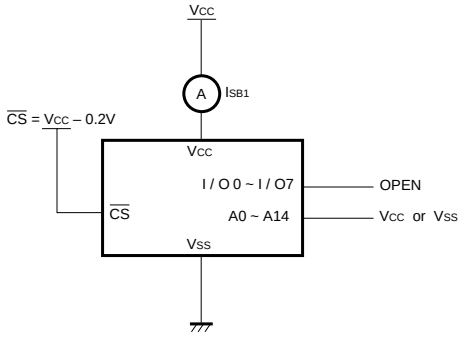


Fig.7

●Operating modes

Control pin			Mode	I / O	Power consumption
$\overline{OE}$	$\overline{CS}$	$\overline{WE}$			
X	H	X	Wait state	High impedance	Standby state
H	L	H	Output disable	High impedance	Operating state
L	L	H	Read	Data output	Operating state
X	L	L	Write	Data input	Operating state

X: Either V_{IL} or V_{IH}

●Input / output capacity (Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input / output capacity	C I / O	—	—	10	pF	V I / O = 0V
Input capacity	C IN	—	—	10	pF	V IN = 0V

Note: These parameters are not measurements for all conditions, but are sample values.

●Part specification

Part number	Acces time (ns)
BR62256F-70LL	70 max.

●AC test conditions (Ta = 0 to + 70°C, V_{CC} = 5V ± 10%)
Input pulse level: 0.8 to 2.4V
Input rise / fall time: 5ns
I / O timing level: 1.5V
Output load: 1 TTL gate and CL = 100pF

●Read cycle

Parameter	Symbol	Min.	Max.	Unit
Read cycle time	t_{RC}	70	—	ns
Address access time	t_{AA}	—	70	ns
Chip enable access time ($\overline{CS}$)	t_{ACS}	—	70	ns
Output enable access time	t_{OE}	—	35	ns
Output hold time	t_{OH}	10	—	ns
$\overline{CS}$ output set time	t_{LZ}	10	—	ns
Output enable and output set time	t_{OLZ}	5	—	ns
Chip deselect output floating	t_{CHZ}	—	30	ns
Chip disable output floating	t_{OHZ}	—	30	ns

●Read cycle timing chart 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, CE2 = $\overline{WE}$ = V_{IH})

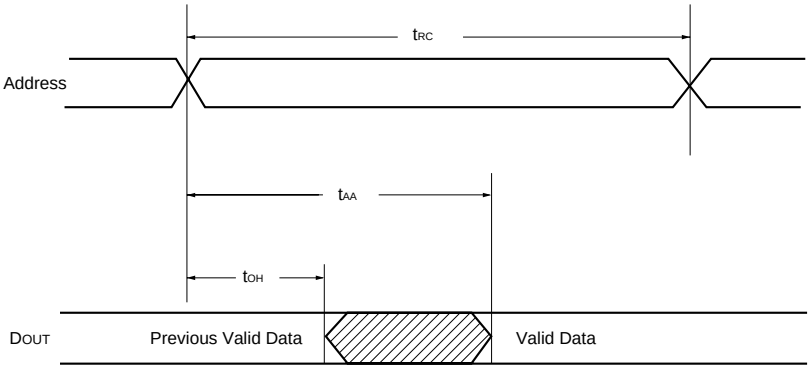


Fig.8

●Read cycle timing chart 2 ($\overline{WE}$ = V_{IH})

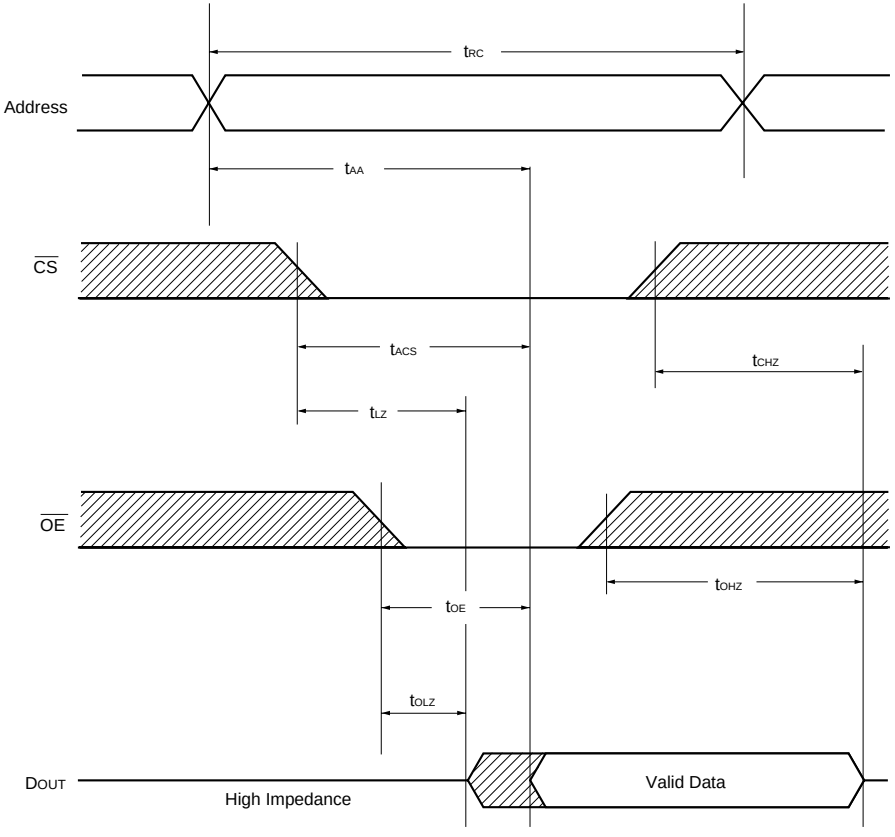


Fig.9

●Write cycle

Parameter	Symbol	Min.	Max.	Unit
Write cycle time	t_{WC}	70	—	ns
Chip select time	t_{CW}	60	—	ns
Address valid time	t_{AW}	60	—	ns
Address setup time	t_{AS}	0	—	ns
Write pulse width	t_{WP}	55	—	ns
$\overline{WE}$ output delay time	t_{WR}	0	—	ns
$\overline{CS}$ output delay time	t_{WR1}	0	—	ns
$\overline{WE}$ output floating time	t_{WHZ}	—	30	ns
Input data set time	t_{DW}	30	—	ns
Input data hold time	t_{DH}	0	—	ns
$\overline{WE}$ output set time	t_{OW}	10	—	ns

●Write cycle timing chart 1 ($\overline{WE}$ control)

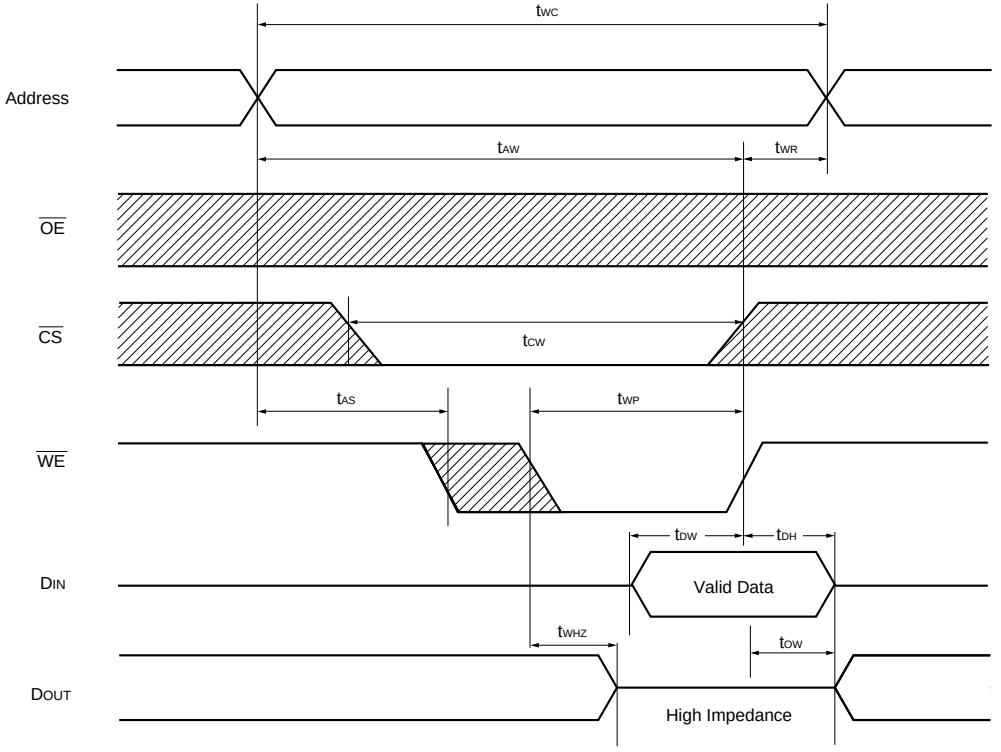


Fig.10

●Write cycle timing chart 2 ($\overline{CS}$ control)

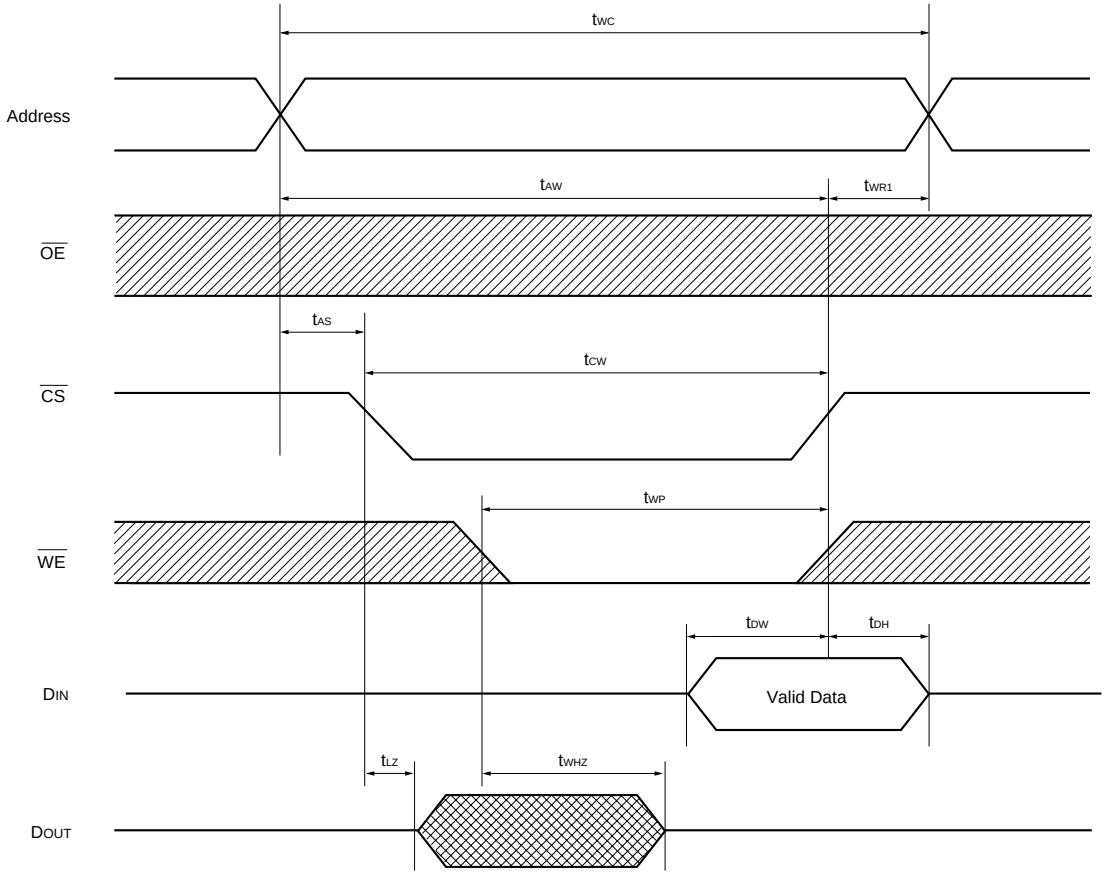


Fig.11

∗ While the I / O pin is in the output state, input signals should not be applied that are in reverse phase to the output.

∗ The contents noted in this document may fall under the jurisdiction of services pertaining to overseas exchange rates and overseas control regulations (services pertaining to design, construction, specifications), and may require special handling.

●Data retention characteristics at low power supply voltage (Ta = 0 to + 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Data retention power supply voltage	VDR	2.0	—	5.5	V	$\overline{CS} \geqq V_{CC} - 0.2V$
Data retention current	ICCDR*1	—	1.0	20	µA	V_{CC} = 3.0V, $\overline{CS} \geqq V_{CC} - 0.2V$
CS data retention time	t_{CDR}	0	—	—	ns	—
Operating recovery time	t_R	5	—	—	ms	—

*1 3µA (max.) when Ta = 0 to 40°C

●Data retention waveform at low power supply voltage

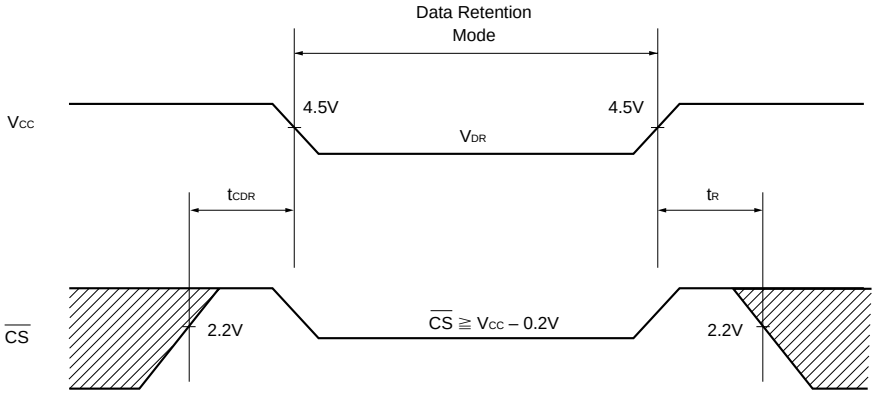
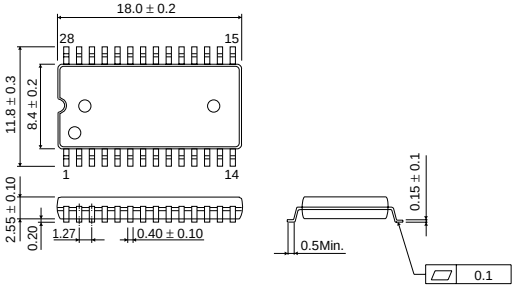


Fig.12

●External dimensions (Units: mm)



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