8-BIT, 4-CELL DIGITAL FILTER PROCESSOR

FEATURES

- 4 filter cells
- Up to 25 MHz sample rate
- 8-bit two's complement or 8-bit unsigned coefficients and signal data
- 26-bit accumulator per stage
- Filter lengths over 500 taps
- Expandable coefficient size, data size and filter length
- Decimation by 2, 3, or 4
- Low power, high-speed CMOS
- 68-pin ceramic leadless chip carrier (LCC)
- Replacement for ZR33481

APPLICATIONS

- 1-D and 2-D FIR filters
- Correlation/convolution
- Adaptive filters
- Matrix multiplication
- Complex multiply-add
- Butterfly computation
- Sample rate converters
- Digital video and audio
- Radar/sonar
- Echo cancellation

GENERAL DESCRIPTION

The ZR33482 (figure 1) is an economical video-speed Digital Filter Processor (DFP) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of four filter cells cascaded internally, all in a single integrated circuit. Each filter cell contains a 9x9 bit two's complement multiplier, three decimation registers and a 26-bit accumulator. The ZR33482 has a maximum sample rate of 25 MHz. The effective multiply-accumulate (MAC) rate is 100 MHz.

Each ZR33482 filter cell contains three resampling or decimation registers which permit output sample rate reduction by 2, 3 or 4. These registers also provide the capability to perform 2-D operations such as matrix multiplication and spatial correlations/convolutions for image processing applications.

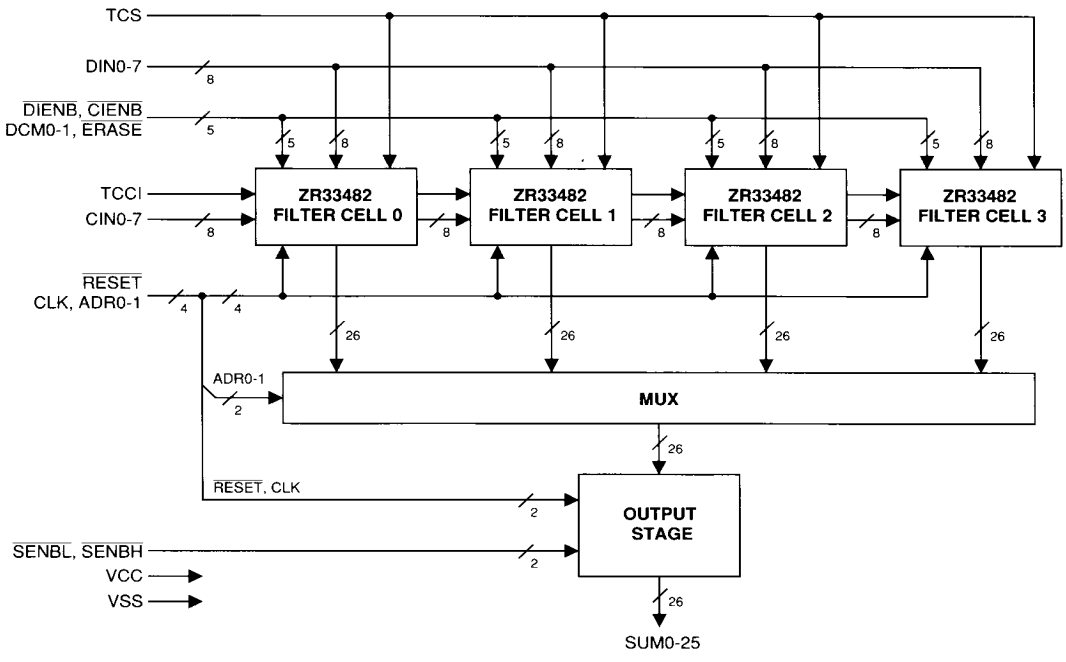


FIGURE 1. ZR33482 BLOCK DIAGRAM

INTERFACE SIGNAL DESCRIPTION

Name	Function
V_{CC}	+5V power supply input.
V_{SS}	Power supply ground input.
CLK	The CLK input provides the ZR33482 system sample clock.
DIN_{0-7}	These eight lines are the data sample input bus. Eight-bit data samples are synchronously loaded through these pins to the data input register (X-REG) of each filter cell of the ZR33482 simultaneously. The $\overline{DIENB}$ signal enables loading, which is synchronous on the rising edge of the clock signal. The data samples can be either 8-bit two's complement or 8-bit unsigned values, depending on the state of the TCS line (see TCS).
$\overline{DIENB}$	A low on this input enables the data sample input bus (DIN_{0-7}) to all filter cells. A rising edge of the CLK signal occurring while $\overline{DIENB}$ is low will load the X register of every filter cell with the 8-bit value present on DIN_{0-7}. A high on this input forces all bits of the data sample input bus to zero; a rising CLK edge when $\overline{DIENB}$ is high will load the X register of every filter cell with zeros. This signal is latched inside the device, delaying its effect by one clock internal to the device. It must go low during the clock cycle immediately preceding presentation of the desired data on the DIN_{0-7} inputs.
CIN_{0-7}	These eight lines are used to input the coefficients. The coefficients are synchronously loaded into the coefficient register (C-REG) of filter CELL0, if a rising edge of CLK occurs while $\overline{CIENB}$ is low. The coefficients can be either 8-bit two's complement or 8-bit unsigned values, depending on the state of the TCCI line (see TCCI).
$\overline{CIENB}$	A low on this input enables the C-REG and the decimation registers (D_1,D_2,D_3) of every filter cell, according to the state of the DCM_{0-1} inputs. A rising edge of the CLK signal occurring while $\overline{CIENB}$ is low will load the C register and appropriate D registers with the coefficient data present at their inputs. This provides the mechanism for shifting the coefficients from cell to cell through the device. A high on this input freezes the contents of the C register and the D registers, ignoring the CLK signal. This signal is latched internal to the ZR33482, therefore it must go low during the clock cycle immediately preceding presentation of the desired coefficient on the CIN_{0-8} inputs.

Name	Function
DCM_{0-1}	These two inputs determine the use of the internal decimation registers as follows: DCM1 DCM0 Decimation Function 0 0 Decimation registers not used 0 1 One decimation register is used 1 0 Two decimation registers are used 1 1 Three decimation registers are used The coefficients pass from cell to cell with a delay determined by the number of decimation registers used. When no decimation registers are used, coefficients move from cell to cell with no added delay. When one decimation register is used, coefficients move from cell to cell with a delay of one clock, etc. These signals are latched internal to the device.
SUM_{0-25}	These 26 three-state outputs are used to output the results of the internal filter cell computations selected by ADR_{0-1}. The signals $\overline{SENBH}$ and $\overline{SENBL}$ enable the most significant and least significant bits of the SUM_{0-25} result respectively. Both $\overline{SENBH}$ and $\overline{SENBL}$ may be enabled simultaneously if the system has a 26-bit or larger bus. However, individual enables are provided to facilitate use with a 16-bit bus.
$\overline{SENBH}$	A low on this input enables result bits SUM_{16-25}. A high on this input places these outputs in their high impedance state.
$\overline{SENBL}$	A low on this input enables result bits SUM_{0-15}. A high on this input places these outputs in their high-impedance state.
ADR_{0-1}	These two inputs select the one cell whose accumulator will be read through the output bus (SUM_{0-25}). They also determine which accumulator will be cleared when $\overline{ERASE}$ is low. If the ADR_{0-1} lines remain at the same address for more than one clock, the output at SUM_{0-25} will not change to reflect any subsequent accumulator updates in the addressed cell. Only the result available during the first clock, when ADR_{0-1} selects the cell, will be output. This does not hinder normal operation since the ADR_{0-1} lines are changed sequentially. This feature facilitates the interface with slow memories where the output is required to be fixed for more than one clock.

INTERFACE SIGNAL DESCRIPTION (continued)

Name	Function
TCS	The TCS input determines the number system interpretation of the data input samples on pins DIN_{0-7} as follows: TCS = LOW → unsigned representation TCS = HIGH → two's complement representation The TCS signal is synchronously loaded into the X register in the same way as the DIN_{0-7} inputs.
TCCI	The TCCI input determines the number system interpretation of the coefficient inputs on pins CIN_{0-7} as follows: TCCI = LOW → unsigned representation TCCI = HIGH → two's complement representation The TCCI signal is synchronously loaded into the C register in the same way as the CIN_{0-7} inputs.

Name	Function
$\overline{RESET}$	A low on this input synchronously* clears all the internal registers, except the cell accumulators. It can also be used with $\overline{ERASE}$ to simultaneously clear all the accumulators. This signal is latched in the ZR33482.
$\overline{ERASE}$	A low on this input synchronously* clears the cell accumulator selected by the ADR_{0-1} signals. If $\overline{RESET}$ is also low simultaneously, all cell accumulators are cleared. This signal is latched in the ZR33482.

* On rising edge of clock.

ZR33482 FILTER CELL

An 8-bit coefficient (CIN_{0-7}) enters each cell through the C register on the left and exits the cell on the right as signals $COUT_{0-7}$ (figure 2). The coefficients may move directly from the C register to the output, exiting the cell on the clock following its entrance. When decimation is selected, the coefficient exit is delayed by 1, 2 or 3 clocks by passing through one or more decimation registers (D_1, D_2 or D_3).

The combination of D registers through which the coefficient passes is determined by the state of DCM0 and DCM1. The output signals ($COUT_{0-7}$) are connected to the CIN_{0-7} inputs of the next cell to its right.

The C and D registers are enabled for loading by $\overline{CIENB}$. Loading is synchronous with CLK when $\overline{CIENB}$ is low. Note that $\overline{CIENB}$ is latched internally. It enables the register for loading after the next CLK following the onset of $\overline{CIENB}$ low. Actual loading occurs on the second CLK following the onset of $\overline{CIENB}$ low. Therefore $\overline{CIENB}$ must go low during the clock cycle immediately preceding presentation of the coefficient on the CIN_{0-7} inputs. In most basic FIR operations, $\overline{CIENB}$ will be low throughout the process, so this latching and delay sequence is only important during the initialization phase. When $\overline{CIENB}$ is high, the coefficients are frozen.

These registers are cleared synchronously under control of $\overline{RESET}$, which is latched and delayed exactly like $\overline{CIENB}$.

The output of the C register (C⟨0:7⟩) is one input to the 9x9 multiplier.

The other input to the 9x9 multiplier comes from the output of the X register. This register is loaded with a data sample from the device input signals DIN_{0-7}.

The X register is enabled for loading by $\overline{DIENB}$. Loading is synchronous with CLK when $\overline{DIENB}$ is low. Note that $\overline{DIENB}$ is latched internally. It enables the register for loading after the next CLK following the onset of $\overline{DIENB}$ low. Actual loading occurs on the second CLK following the onset of $\overline{DIENB}$ low. Therefore $\overline{DIENB}$ must go low during the clock cycle immediately preceding presentation of the data sample on the DIN_{0-7} inputs. In most basic FIR operations, $\overline{DIENB}$ will be low throughout the process, so this latching and delay sequence is only important during the initialization phase. When $\overline{DIENB}$ is high, the X register is loaded with all zeros.

The pipelined multiplier is modeled in figure 2 as a multiplier core followed by two pipeline registers, M0-REG and M1-REG. The multiplier output is sign extended and input as one operand of the 26-bit adder. The other adder operand is the output of the 26-bit accumulator. The adder output is loaded synchronously into both the accumulator and the output register, T-REG.

The T-REG loading is disabled by the cell select signal, CELLn, where n is the cell number. The cell select is decoded from the ADR_{0-1} signals to generate the T-REG load enable. The cell select is inverted, delayed and applied as the load enable to the T-REG, so that the T-REG is loaded whenever the cell is not selected. The purpose of the T-REG is to hold the result of a sum-of-products calculation during the clock when the accumulator is cleared to prepare for the next sum-of-products calculation. This allows continuous accumulation without wasting clocks.

The accumulator is loaded with the adder output every clock unless it is cleared. It is cleared synchronously in two ways. When $\overline{RESET}$ and $\overline{ERASE}$ are both low, the accumulator is cleared along with all other registers of the device. Since $\overline{ERASE}$ and $\overline{RESET}$ are latched internally, clearing occurs on the second CLK following the onset of both $\overline{ERASE}$ and $\overline{RESET}$ low.

The second accumulator clearing mechanism clears a single accumulator in a selected cell. The cell select signal, CELLn, decoded from ADR_{0-1} and the $\overline{ERASE}$ signal, enable clearing of the accumulator on the next CLK.

The $\overline{ERASE}$ and $\overline{RESET}$ signals clear the ZR33482 internal registers and states as follows:

$\overline{ERASE}$	$\overline{RESET}$	CLEARING EFFECT
1	1	No clearing occurs, internal state remains the same.
1	0	Only $\overline{RESET}$ active. All registers except accumulators are cleared, including the internal pipeline registers.
0	1	Only $\overline{ERASE}$ active. The accumulator whose address is given by the ADR0-1 inputs is cleared.
0	0	Both $\overline{RESET}$ and $\overline{ERASE}$ active. All accumulators as well as all other registers are cleared.

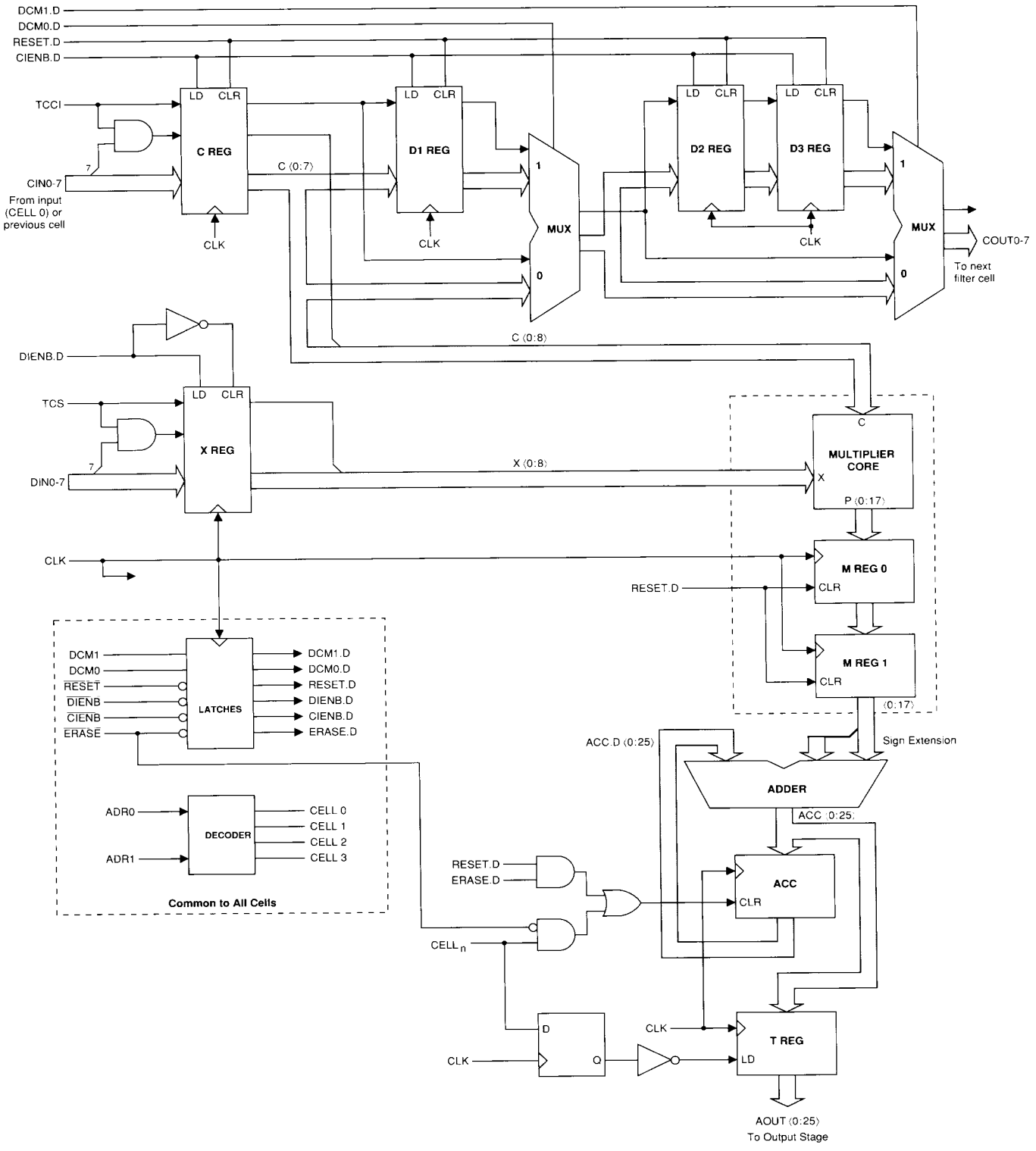


FIGURE 2. TYPICAL ZR33482 FILTER CELL

ZR33482 OUTPUT STAGE

The output stage consists of a cell result multiplexer and a 26-bit three-state driver stage (figure 3).

The cell result mux selects the contents of the filter cell accumulator addressed by ADR_{0-1}. If the ADR_{0-1} lines remain at the same address for more than one clock, the output at SUM0-25 will not change to reflect any subsequent accumulator updates in the addressed cell. Only the result available during the first clock when ADR_{0-1} selects the cell will be output. This does not hinder normal FIR operation since the ADR_{0-1} lines are changed sequentially. This feature facilitates the interface with slow memories where the output is required to be fixed for more than one clock.

The clock input to the cell result mux is used for synchronization and does not introduce an extra delay.

The SUM_{0-25} output bus is controlled by the $\overline{SENBH}$ and $\overline{SENBL}$ signals. A low on $\overline{SENBL}$ enables bits SUM_{0-15}. A low on $\overline{SENBH}$ enables bits SUM_{16-25}. Thus all 26 bits can be output simultaneously if the external system has a 26-bit or larger bus. If the external system bus is only 16 bits, the bits can be enabled in two groups of 16 and 10 bits.

Also, the output may be arbitrarily scaled and truncated by connecting the proper output bits to output bus lines. For example, assume a filter kernel that with expected input signals, will produce only 22-bit results. Those may be scaled and truncated for a 16-bit output bus by connecting bits SUM_{6-21} to output bus lines 0-15 respectively. Both the $\overline{SENBH}$ and $\overline{SENBL}$ should be active in this case.

Note that this technique is much preferable to scaling down the coefficients (or the input data) to produce only 16-bit results directly, since this would require truncating the coefficients (or the data) to only 3 bits (!), introducing extreme degradation of the frequency response characteristics (or high levels of quantization-noise/distortion).

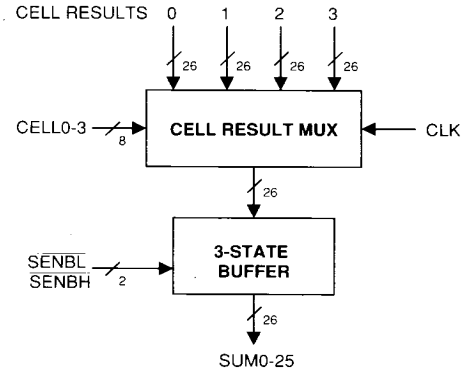


FIGURE 3. ZR33482 OUTPUT STAGE

ZR33482 ARITHMETIC

Both data samples and coefficients can be represented as either unsigned or two's complement numbers. The TCS and TCCI input signals determine the type of arithmetic representation. Internally all values are represented by a 9-bit two's complement number. The value of the additional ninth bit depends on the arithmetic representation selected. For two's complement arithmetic, the sign is extended into the ninth bit. For unsigned arithmetic, bit 9 is 0.

The multiplier output is 18 bits and the accumulator is 26 bits. The accumulator width determines the maximum possible number of terms in the sum-of-products without overflow. The maximum number of terms depends also on the number system and the distribution of the coefficient and data values. As a worst case, assume the coefficients and data samples are always at their maximum absolute values. Then the maximum numbers of terms in the sum of products are:

Number System	Maximum Number of Terms
Two unsigned vectors	1032
Two two's complement vectors	
• Two positive vectors	2080
• Two negative vectors	2047
• One positive and one negative vector	2064
One unsigned and one two's complement vector	
• Positive two's complement vector	1036
• Negative two's complement vector	1028

For practical FIR filters, the coefficients are never all near maximum value, so even larger vectors are possible in practice.

BASIC FIR OPERATION

Detailed operation of the ZR33482 to perform a basic 4-tap, 8-bit coefficient, 8-bit data, 25 MHz FIR filter is best understood by observing the schematic (figure 4), timing diagram (figure 5) and sequence table (table 1). The internal pipeline length of the ZR33482 is four clock cycles, corresponding to the registers C-REG (or X-REG), M0-REG, M1-REG, and T-REG (figures 2 and 3). Therefore the delay from first presentation of data and coefficients at the DIN_{0-7} and CIN_{0-7} inputs to a sum appearing at the SUM_{0-25} output is 8 clock cycles.

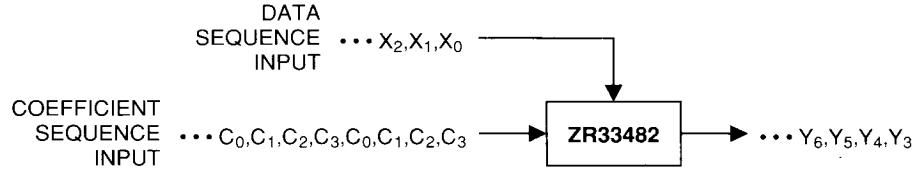
After the pipeline has filled, a new output sample is available every clock. The delay to last sample output from last sample input is 4 clocks.

The output sums, Yn, shown in the timing diagram and sequence table are derived from the sum-of-products equation:

$$Y(n) = C(0)\,X(n) + C(1)\,X(n\text{-}1) + C(2)\,X(n\text{-}2) + C(3)\,X(n\text{-}3)$$

where n refers to an index.

The sequence table (table 1) shows the results of the adder in each cell and the chip output at each clock.



CLK	CELL 0	CELL 1	CELL 2	CELL 3	SUM/CLR
4	$C_3 \cdot X_0$	0	0	0	—
5	+ $C_2 \cdot X_1$	$C_3 \cdot X_1$	0	0	—
6	+ $C_1 \cdot X_2$	+ $C_2 \cdot X_2$	$C_3 \cdot X_2$	0	—
7	+ $C_0 \cdot X_3$	+ $C_1 \cdot X_3$	+ $C_2 \cdot X_3$	$C_3 \cdot X_3$	—
8	$C_3 \cdot X_4$	+ $C_0 \cdot X_4$	+ $C_1 \cdot X_4$	+ $C_2 \cdot X_4$	—
9	+ $C_2 \cdot X_5$	$C_3 \cdot X_5$	+ $C_0 \cdot X_5$	+ $C_1 \cdot X_5$	CELL0 (Y3)
10	+ $C_1 \cdot X_6$	+ $C_2 \cdot X_6$	$C_3 \cdot X_6$	+ $C_0 \cdot X_6$	CELL1 (Y4)
11	+ $C_0 \cdot X_7$	+ $C_1 \cdot X_7$	+ $C_2 \cdot X_7$	$C_3 \cdot X_7$	CELL2 (Y5)

TABLE 1. ZR33482 25 MHz, 4-TAP FIR FILTER SEQUENCE

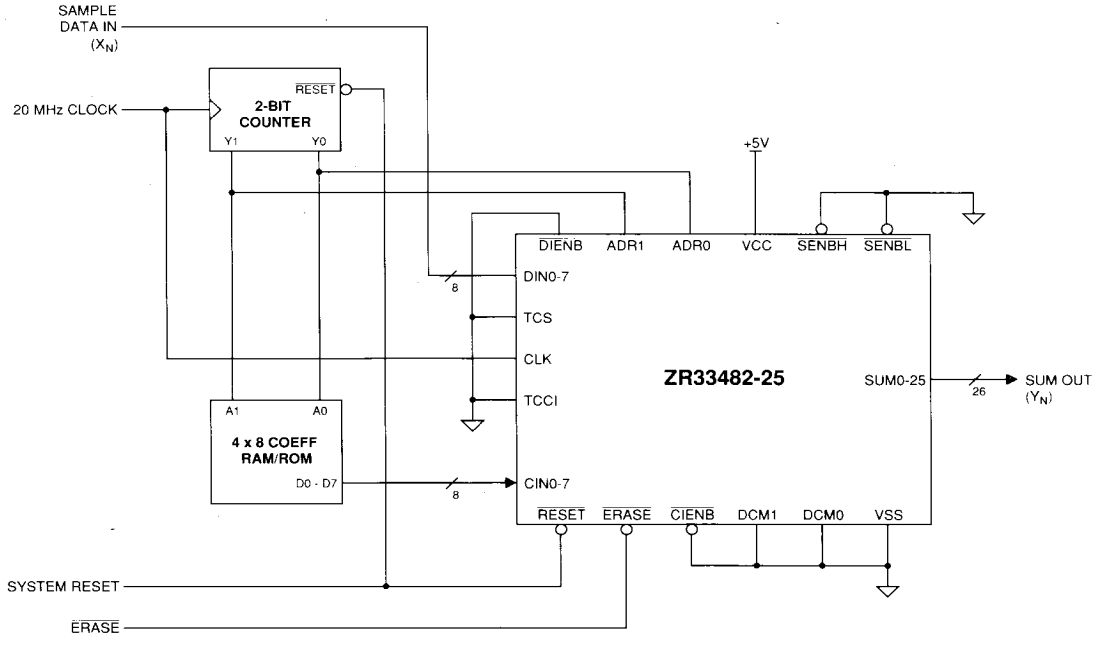


FIGURE 4. ZR33482 25 MHz, 4-TAP FIR FILTER APPLICATION SCHEMATIC

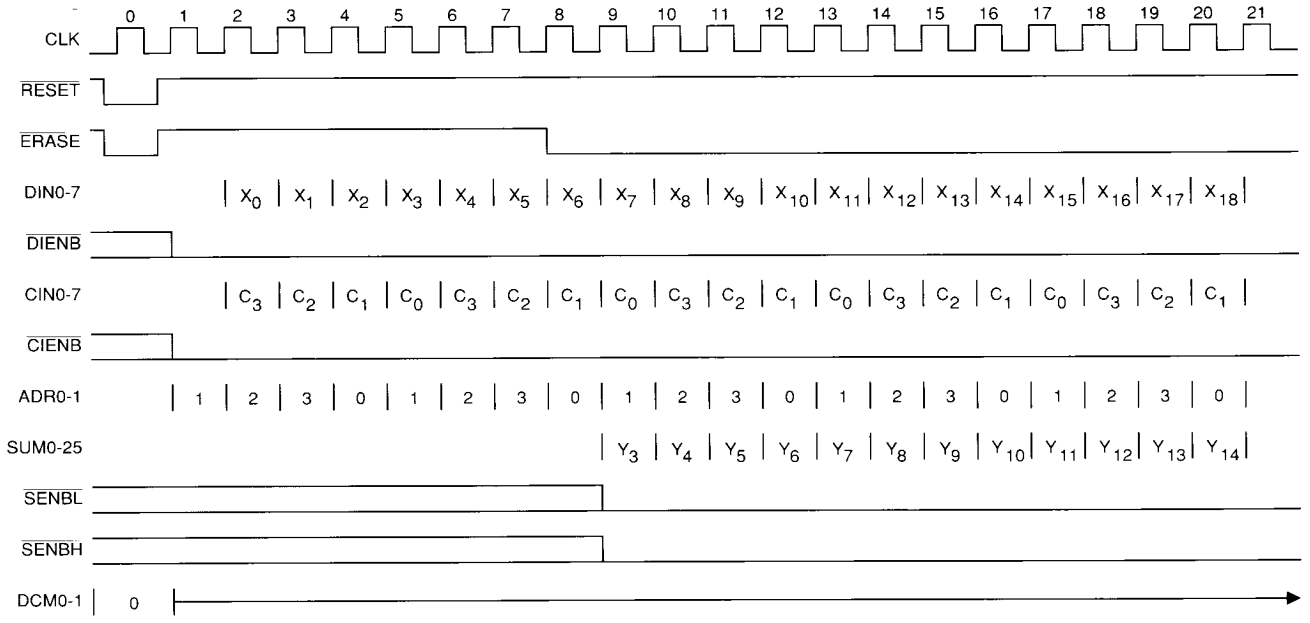
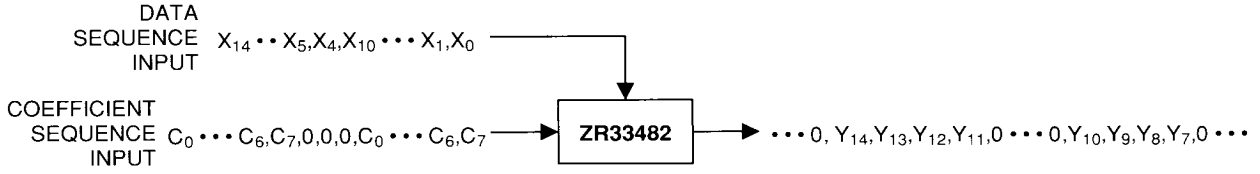


FIGURE 5. ZR33482 25 MHz, 4-TAP FIR FILTER TIMING



CLK	CELL 0	CELL 1	CELL 2	CELL 3	SUM/CLR
4	$C_7 \cdot X_0$	0	0	0	—
5	+ $C_6 \cdot X_1$	$C_7 \cdot X_1$	0	0	—
6	+ $C_5 \cdot X_2$	+ $C_6 \cdot X_2$	$C_7 \cdot X_2$	0	—
7	+ $C_4 \cdot X_3$	+ $C_5 \cdot X_3$	+ $C_6 \cdot X_3$	$C_7 \cdot X_3$	—
8	+ $C_3 \cdot X_4$	+ $C_4 \cdot X_4$	+ $C_5 \cdot X_4$	+ $C_6 \cdot X_4$	—
9	+ $C_2 \cdot X_5$	+ $C_3 \cdot X_5$	+ $C_4 \cdot X_5$	+ $C_5 \cdot X_5$	—
10	+ $C_1 \cdot X_6$	+ $C_2 \cdot X_6$	+ $C_3 \cdot X_6$	+ $C_4 \cdot X_6$	—
11	+ $C_0 \cdot X_7$	+ $C_1 \cdot X_7$	+ $C_2 \cdot X_7$	+ $C_3 \cdot X_7$	—
12	0	+ $C_0 \cdot X_8$	+ $C_1 \cdot X_8$	+ $C_2 \cdot X_8$	—
13	0	0	+ $C_0 \cdot X_9$	+ $C_1 \cdot X_9$	CELL0 (Y7)
14	0	0	0	+ $C_0 \cdot X_{10}$	CELL1 (Y8)
15	$C_7 \cdot X_4$	0	0	0	CELL2 (Y9)
16	+ $C_6 \cdot X_5$	$C_7 \cdot X_5$	0	0	CELL3 (Y10)
17	+ $C_5 \cdot X_6$	+ $C_6 \cdot X_6$	$C_7 \cdot X_6$	0	—
18	+ $C_4 \cdot X_7$	+ $C_5 \cdot X_7$	+ $C_6 \cdot X_7$	$C_7 \cdot X_7$	—
19	+ $C_3 \cdot X_8$	+ $C_4 \cdot X_8$	+ $C_5 \cdot X_8$	+ $C_6 \cdot X_8$	—
20	+ $C_2 \cdot X_9$	+ $C_3 \cdot X_9$	+ $C_4 \cdot X_9$	+ $C_5 \cdot X_9$	—
21	+ $C_1 \cdot X_{10}$	+ $C_2 \cdot X_{10}$	+ $C_3 \cdot X_{10}$	+ $C_4 \cdot X_{10}$	—
22	+ $C_0 \cdot X_{11}$	+ $C_1 \cdot X_{11}$	+ $C_2 \cdot X_{11}$	+ $C_3 \cdot X_{11}$	—
23	0	+ $C_0 \cdot X_{12}$	+ $C_1 \cdot X_{12}$	+ $C_2 \cdot X_{12}$	—
24	0	0	+ $C_0 \cdot X_{13}$	+ $C_1 \cdot X_{13}$	CELL0 (Y11)
25	0	0	0	+ $C_0 \cdot X_{14}$	CELL1 (Y12)

TABLE 2. 9.09 MHz 8-TAP FIR FILTER SEQUENCE USING SINGLE ZR33482-25

EXTENDED FILTER LENGTHS

Using a single ZR33482, a filter of length L>4 can be constructed by processing in L/4 passes as illustrated in the following table (table 2) for an 8-tap FIR. Each pass is composed of 3+L cycles and computes four output samples. In pass i, the samples with indices i*4 to i*4 + (L+2) enter the DIN_{0-7} inputs. The coefficients C_0 - C_{L-1} enter the CIN_{0-7} inputs, followed by three zeros. As these zeros are entered, the result samples are output and the accumulators reset. Filter outputs can be put through a FIFO to even out the sample rate.

EXTENDED COEFFICIENT AND DATA SAMPLE WORD SIZE

The data and coefficient word size can be extended by utilizing several ZR33482's in parallel to get the maximum sample rate, or a single ZR33482 with resulting lower sample rates. The technique is to compute partial products of 8x8 and combine these partial products by shifting and adding to obtain the final result. The shifting and adding can be accomplished with external adders. (Note that the least significant parts of the data and/or coefficients are unsigned.)

DECIMATION/RESAMPLING

The ZR33482 provides a mechanism for decimating by factors of 2, 3, or 4, using the three D registers and two multiplexers in the coefficient path through the cell (figure 2). The sequence table (table 3) and the timing diagrams (figure 6) illustrate the technique for an 8-tap, decimate-by-two, FIR filter with 25 MHz input sample rate and 12.5 MHz output sample rate.

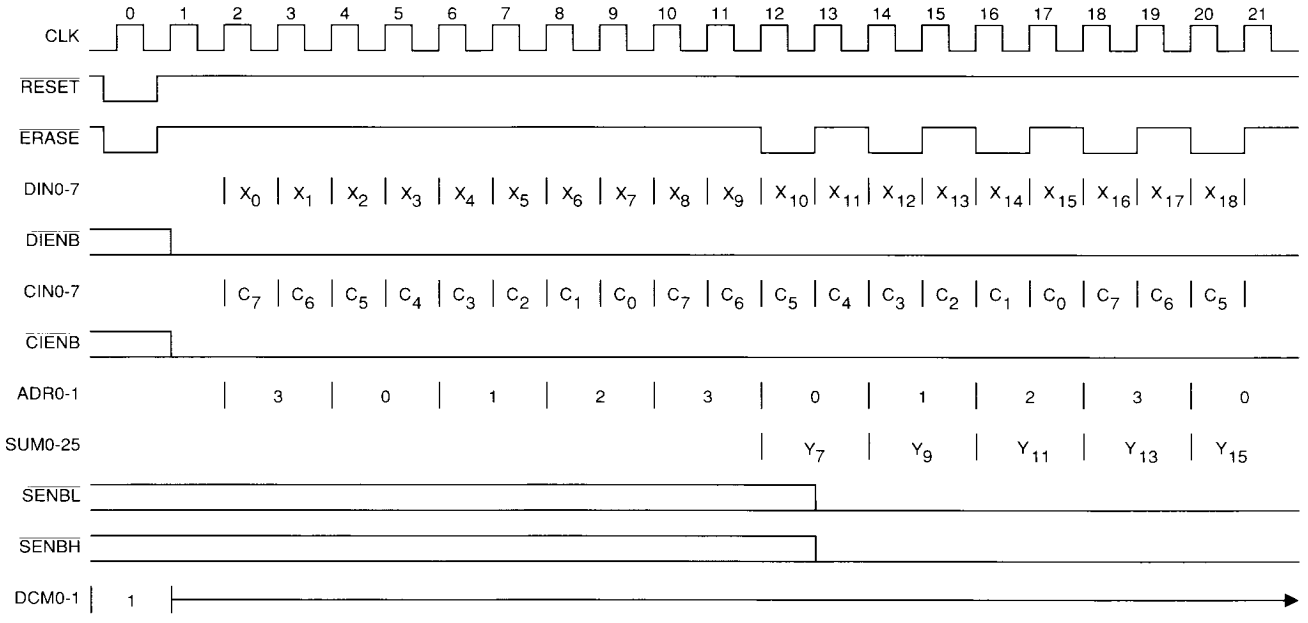
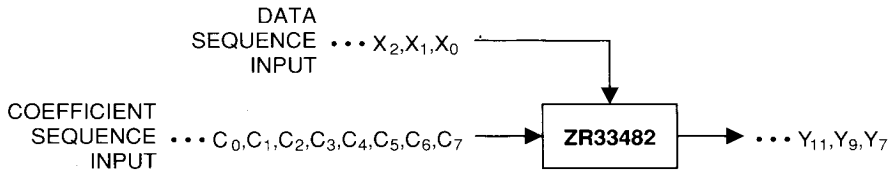


FIGURE 6. ZR33482 8-TAP DECIMATE-BY-TWO FIR FILTER TIMING, 25 MHz IN, 12.5 MHz OUT

OTHER ZR33482 APPLICATIONS

The ZR33482 is a versatile device with many applications beyond simple FIR filtering. The following list is a small sample of some applications possible with the ZR33482. Implementations of some of these applications are discussed in greater detail in various Zoran Application Notes.

- Higher bandwidth (50 MHz and up)
- 2-D FIR Spatial Filtering/Convolution/Correlation
- Matrix multiplication
- Complex multiply
- Butterfly computation
- DFT
- Adaptive filters
  - Echo cancellation
  - Adaptive equalization
- Reverberation generators
- Beam former
- Video decoders



CLK	CELL 0	CELL 1	CELL 2	CELL 3	SUM/CLR
4	$C_7 \cdot X_0$	0			—
5	$+ C_6 \cdot X_1$	0			—
6	$+ C_5 \cdot X_2$	$C_7 \cdot X_2$			—
7	$+ C_4 \cdot X_3$	$+ C_6 \cdot X_3$			—
8	$+ C_3 \cdot X_4$	$+ C_5 \cdot X_4$	$C_7 \cdot X_4$		—
9	$+ C_2 \cdot X_5$	$+ C_4 \cdot X_5$	$+ C_6 \cdot X_5$		—
10	$+ C_1 \cdot X_6$	$+ C_3 \cdot X_6$	$+ C_5 \cdot X_6$	$C_7 \cdot X_6$	—
11	$+ C_0 \cdot X_7$	$+ C_2 \cdot X_7$	$+ C_4 \cdot X_7$	$+ C_6 \cdot X_7$	—
12	$C_7 \cdot X_8$	$+ C_1 \cdot X_8$	$+ C_3 \cdot X_8$	$+ C_5 \cdot X_8$	—
13	$+ C_6 \cdot X_9$	$+ C_0 \cdot X_9$	$+ C_2 \cdot X_9$	$+ C_4 \cdot X_9$	CELL0 (Y7)
14	$+ C_5 \cdot X_{10}$	$C_7 \cdot X_{10}$	$+ C_1 \cdot X_{10}$	$+ C_3 \cdot X_{10}$	—
15	$+ C_4 \cdot X_{11}$	$+ C_6 \cdot X_{11}$	$+ C_0 \cdot X_{11}$	$+ C_2 \cdot X_{11}$	CELL1 (Y9)
16	$+ C_3 \cdot X_{12}$	$+ C_5 \cdot X_{12}$	$C_7 \cdot X_{12}$	$+ C_1 \cdot X_{12}$	—
17	$+ C_2 \cdot X_{13}$	$+ C_4 \cdot X_{13}$	$+ C_6 \cdot X_{13}$	$+ C_0 \cdot X_{13}$	CELL2 (Y11)
18	$+ C_1 \cdot X_{14}$	$+ C_3 \cdot X_{14}$	$+ C_5 \cdot X_{14}$	$C_7 \cdot X_{14}$	—
19	$+ C_0 \cdot X_{15}$	$+ C_2 \cdot X_{15}$	$+ C_4 \cdot X_{15}$	$+ C_6 \cdot X_{15}$	CELL3 (Y13)
20	$C_7 \cdot X_{16}$	$+ C_1 \cdot X_{16}$	$+ C_3 \cdot X_{16}$	$+ C_5 \cdot X_{16}$	—
21	$+ C_6 \cdot X_{17}$	$+ C_0 \cdot X_{17}$	$+ C_2 \cdot X_{17}$	$+ C_4 \cdot X_{17}$	CELL0 (Y15)

TABLE 3. ZR33482 8-TAP DECIMATE-BY-TWO FIR FILTER SEQUENCE, 25 MHz IN, 12.5 MHz OUT

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage to Ground Potential
Continuous ..... -0.5V to +7.0V
DC Voltage Applied to
Outputs for High Output State ..... -0.5V to +7.0V
DC Input Voltage ..... -0.5V to +5.5V

DC Output Current, into Outputs
(not to exceed 200 mA total) 20mA/output
DC Input Current ..... -30 to +5.0mA

NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGE

Commercial Devices

Temperature ..... $0°C \le T_A \le +70°C$
Supply Voltage ..... $4.75V \le V_{CC} \le 5.25V$

Military Devices

Temperature ..... $-55°C \le T_A \le +125°C$
Supply Voltage ..... $4.50V \le V_{CC} \le 5.50V$

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA
I_{CC}	Power Supply Current @ 20 MHz		100	mA	$T_A = 0°C$, $V_{CC} = V_{CCmax}$
I_{LI}	Input Leakage Current		±10	µA	$0 < V_{IN} < V_{CCmax}$
I_{LO}	Output Leakage Current		±10	µA	$0.45 < V_{OUT} < V_{CCmax}$
V_{CL}	Clock in Low Voltage	-0.5	0.6	V	
V_{CH}	Clock in High Voltage	4.0	V_{CC} + 0.5	V	
C_{IN}	Input Capacitance		10	pF	f_C = 1MHz
C_{IO}	I/O, Clock, and Output Capacitance		10	pF	f_C = 1MHz

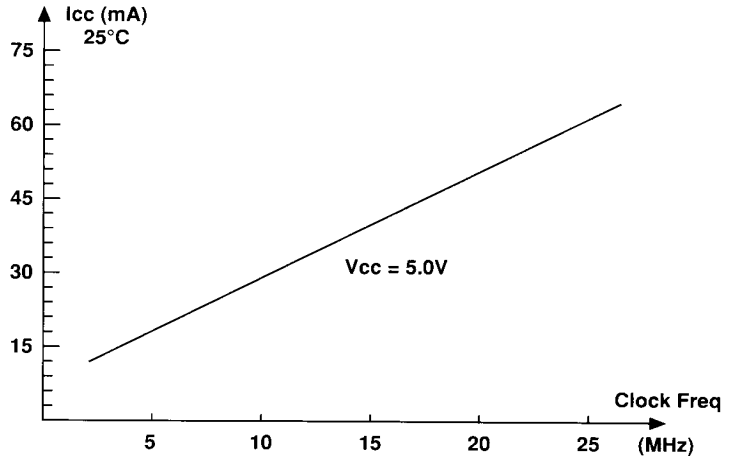


FIG 7. TYPICAL Icc VS. FREQUENCY

AC CHARACTERISTICS

Symbol	Parameter	ZR33482-15		ZR33482-20		ZR33482-25		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
T_{CP}	Clock Period	67	5000	50	5000	40	5000	ns	
T_{CH}	Clock High	30		22		18		ns	
T_{CL}	Clock Low	30		22		18		ns	
T_{CR}	Clock Rise		5		5		5	ns	1.0V to 3.5V
T_{CF}	Clock Fall		5		5		5	ns	1.0V to 3.5V
T_{IH}	In Hold	5		5		5		ns	
T_{IS}	In Setup	14		10		8		ns	
T_{OED}	Output Enable Delay*		25		20		15	ns	
T_{ODD}	Output Disable Delay*		25		20		15	ns	
T_{ODS}	Clock to SUM Output Delay		50		40		28	ns	

* Not tested in production. Guaranteed by characterization.

AC TIMING DIAGRAMS

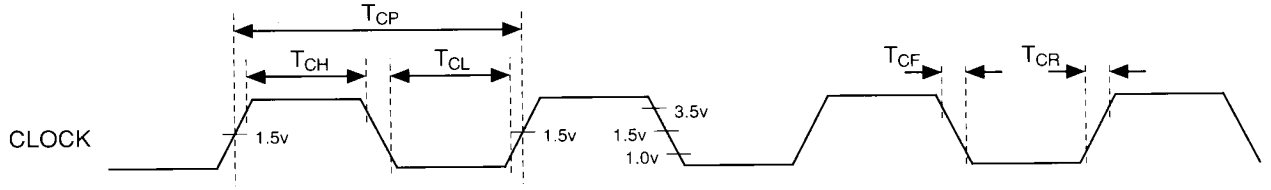
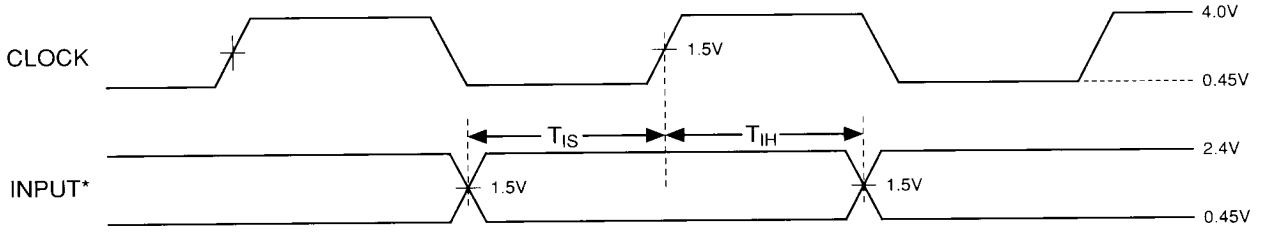
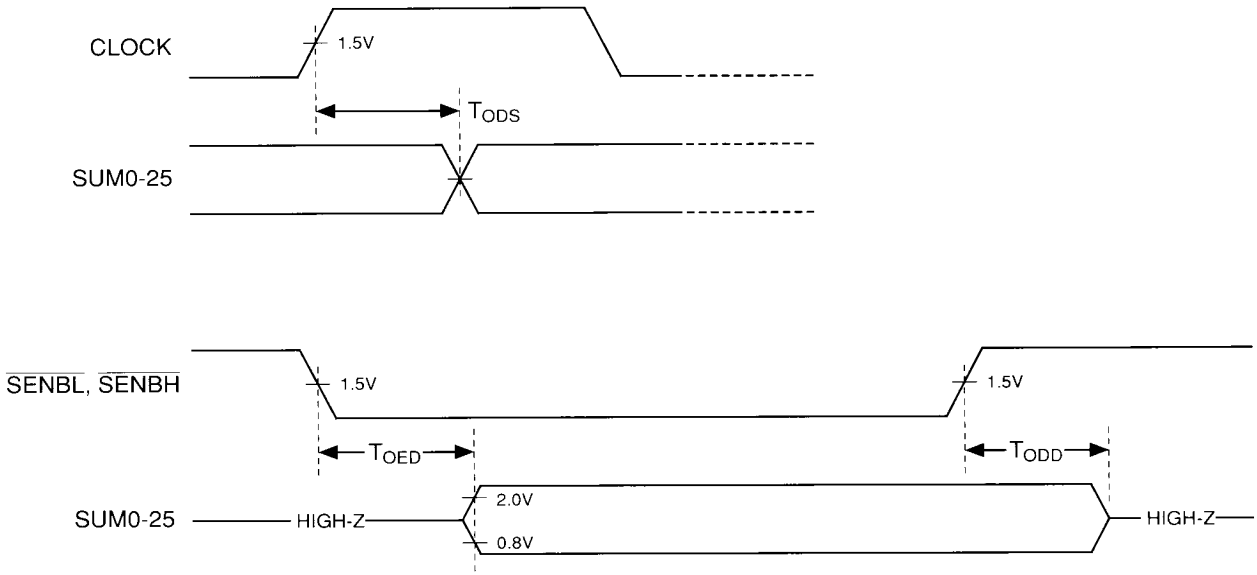


FIGURE 8. CLOCK AC CHARACTERISTICS



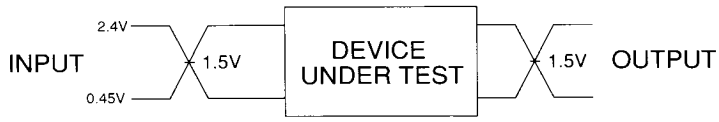
* Input includes: DIN0-7, CIN0-7, $\overline{\text{DIENB}}$, $\overline{\text{CIENB}}$, $\overline{\text{ERASE}}$, $\overline{\text{RESET}}$, DCM0-1, ADR0-1

FIGURE 9. INPUT SETUP AND HOLD



SUM_{0-25} is assumed not to be in high-impedance state.

FIGURE 10. SUM_{0-25}, OUTPUT DELAYS



A.C. testing, inputs are driven at 2.4V for a logic "1" and .45V for a logic "0". Input and output timing measurments are made at 1.5V for both a logic "1" and "0".

FIGURE 11. A.C. TESTING INPUT, OUTPUT WAVEFORM

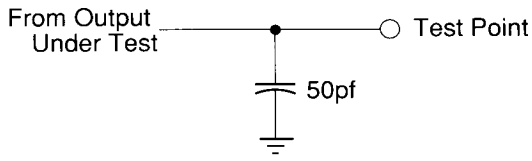
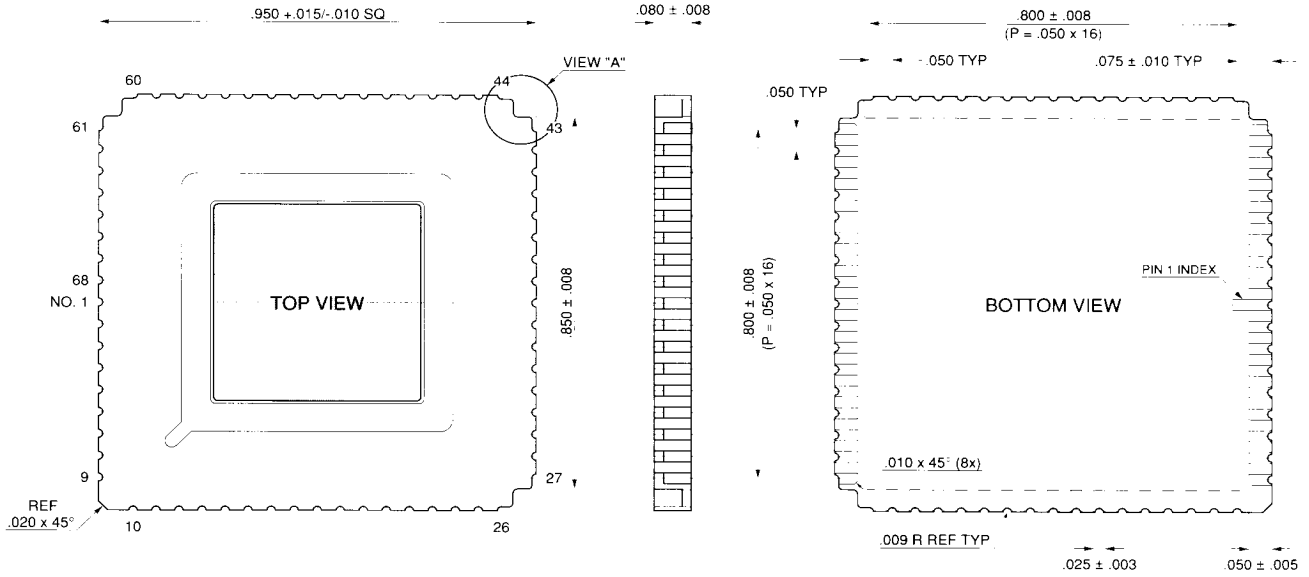
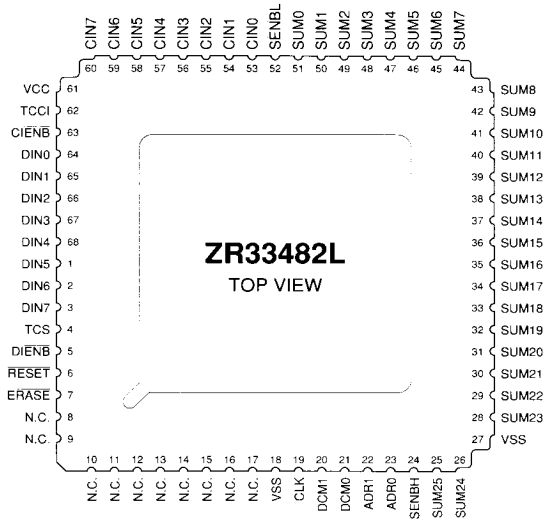


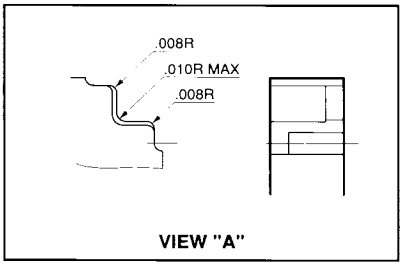
FIGURE 12. NORMAL A.C. TEST LOAD

PACKAGE INFORMATION



Note: All dimensions in inches.





ZR33482 68-PIN LEADLESS CHIP CARRIER (LCC)

REPLACEMENT OF ZR33481 WITH ZR33482

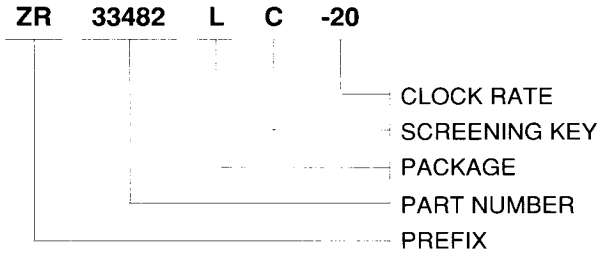
The ZR33482 is designed to be a pin-for-pin replacement for the ZR33481. The following table summarizes the similarities and differences.

For new designs that require longer FIR filters, use Zoran's 8-filter cell Digital Filter products: ZR33891 and ZR33881. Please contact us for more information.

PRODUCT	ZR33482LC	ZR33481LC
Package Type	68-Pin Ceramic Leadless Chip Carrier (LCC)	Identical
Clock Speed Versions	15, 20 & 25 MHz	15 & 20 MHz Only
Number of Filter Cells	Four	Identical
Coefficient & Input Format	8-bit 2's complement or 8-bit unsigned	Identical
Output Format	26-bit 2's complement	Identical
Decimation Modes	2, 3 & 4	Identical
Coefficient Cascadability	Not Supported; $COUT_{0-7}$, $\overline{COENB}$ & TCCO Pins are "No Connects" (Opens)	As Specified

NOTES:

ORDERING INFORMATION



PACKAGE
L - 68-Pin Leadless Chip Carrier

CLOCK RATE
15, 20, 25 MHz

SCREENING KEY
C - 0°C to +70°C (V_{CC} = 4.75V to 5.25V)
M - Assembly and test to Zoran's MIL. (883)

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