AMERICAN MICROSYSTEMS, INC.
WavePlex™ Wireless Products

SX041, SX042, SX043
Spread Spectrum Baseband Controllers

January, 1997

Datasheet

1.0 Introduction

AMI's WavePlex™ Wireless Products include the following Spread Spectrum Baseband Controller ICs:

- SX041 Transmit-Only
- SX042 Receive-Only
- SX043 Transceiver

1.1 Features

- Low power with user controlled 'shutdown' modes.
- 3.3 volt (or 5.0 volt - H option) (+/- 10%).
- Narrow band and Spread Spectrum operation, independently selectable for transmit and receive.
- Performs all baseband functions required for implementation of direct sequence spread spectrum and can be used in any radio frequency band.
- User programmable transmission protocol with pass through or packetization formatting.
- Generic microprocessor interface.
- Full or half duplex operation. (SX043 only)
- High process gain (up to 2047 chips/bit) with data rates from 100 bps to 4 Mbps. (SX041 maximum data rate is 2 Mbps).
- Independent transmit and receive PN code generators for the SX043.
- Gold code and 11-chip Barker code options.
- Programmable preamble lengths for faster acquisition when there has been recent transmission or reception.
- Byte wide transmit and receive data FIFOs.
- 16 or 32 bit CRC error checking.
- 8 or 16 bit receiver address for the SX042 & SX043.
- Optional data scrambling.
- Support for: Binary Phase Shift Keying (BPSK); Differential Binary Phase Shift Keying (DBPSK); Quadrature Phase Shift Keying (QPSK); Differential Quadrature Phase Shift Keying (DQPSK); 8 & 16 Quadrature Amplitude Modulation (QAM). (QAM is not supported on the SX041).
- Continuous tracking feature, for transferring multiple packets of data at high data rates without reacquiring signal-lock.

AMI's WavePlex ICs simplify the design of direct sequence spread spectrum radios. They contain all the baseband circuitry needed to implement a radio, thus providing an economical solution to the extensive digital hardware requirements of high performance spread spectrum radios.

The SX041, SX042 and SX043 are available in either 3.3 volt or 5 volt versions. The 3.3 volt version is a low power device intended for portable battery powered applications. It utilizes a 3.3 volt power supply and interfaces to a 3 volt microcontroller and logic. The 5 volt version is intended for applications where power consumption is not critical and 5 volt supplies and interfaces are required.

The SX043 Transceiver IC consists of a microprocessor interface and a full duplex transmit/receive message processor circuit. Included in the SX041 Transmit-Only IC and the SX043 message processor transmit circuits are the data scrambler, packet generator, CRC generator, pseudonoise (PN) code generator, and modulation mode formatter. The SX042 Receive-Only IC and the SX043 message processor receive circuits include the receive PN code generator, receive synchronization and tau-dither tracking loop, integrate and dump control, data descrambler, packet decoder, CRC checker, demodulator, and signal strength indicator. Each transmit and receive PN code generator consists of two 11-bit PN generators, allowing selection of an "A" code, a "B" code, or a "Gold code" combination of the "A" and "B" codes. AMI's SX043 uses separate transmit and receive 64 MHz VCO's, which allows fully independent transmit and receive operations.

AMI's WavePlex ICs interface to a generic microprocessor bus for programming and data transfer, and to an IF modulator/demodulator and RF radio for the transmission medium. 8530 SCC operation and HDLC protocol are emulated for the message packetization and error checking. No packetization can also be selected for data to be transmitted as received from the host.

The SX041, SX042 and SX043 are high performance parts, capable of chipping rates up to 64 Mchips/second in transmit and receive modes. This results in a maximum data rate of 2 Mbps using QPSK or DQPSK modulation and a PN code length of 63. A maximum data rate of 1 Mbps is achieved using BPSK or DBPSK modulation and a PN code length of 63. At lower chipping rates, the ICs are capable of generating code lengths up to 2047 chips. The lowest possible chipping rate is 300 Hz. The flexibility of the design allows an optimal combination of transmitted power, system process gain, system bandwidth and bit rate in order to achieve a reliable communication channel with minimum interference to other adjacent channel or co-channel users.

Figure 1: SX041 Transmit-Only Block Diagram Top Level

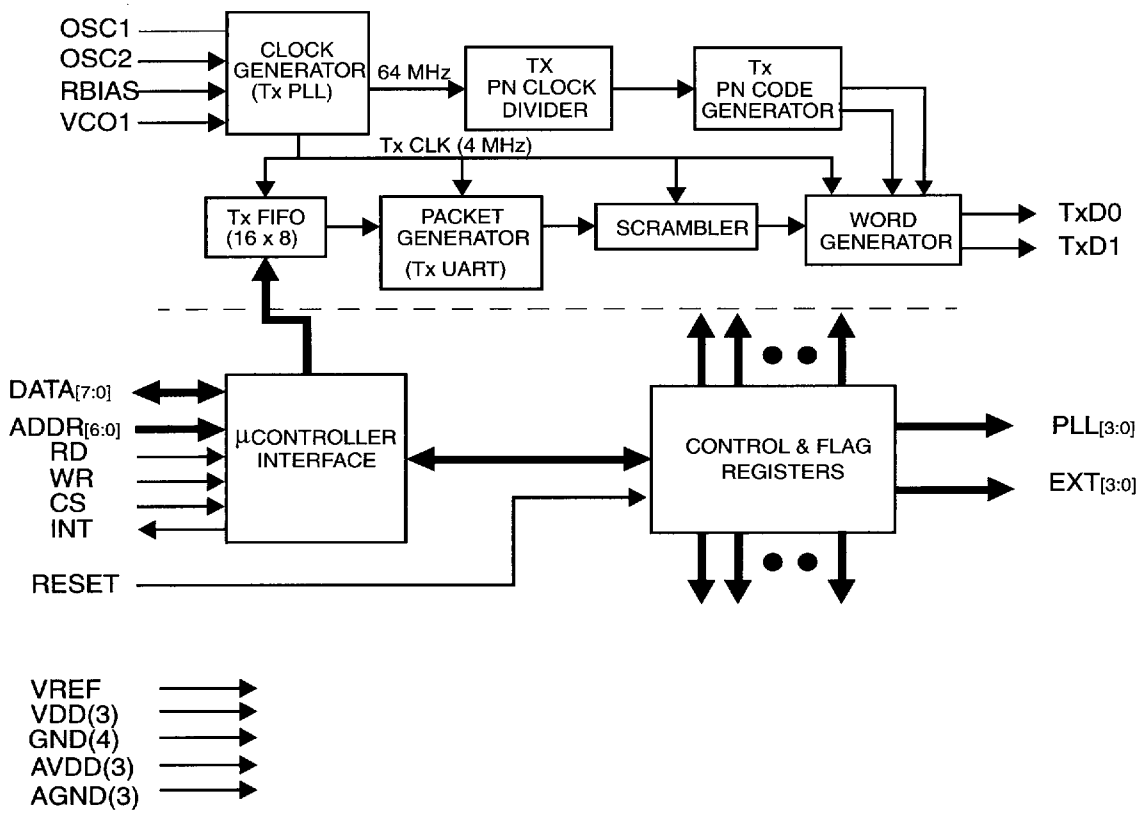


Figure 2: SX042 Receive-Only Block Diagram Top Level

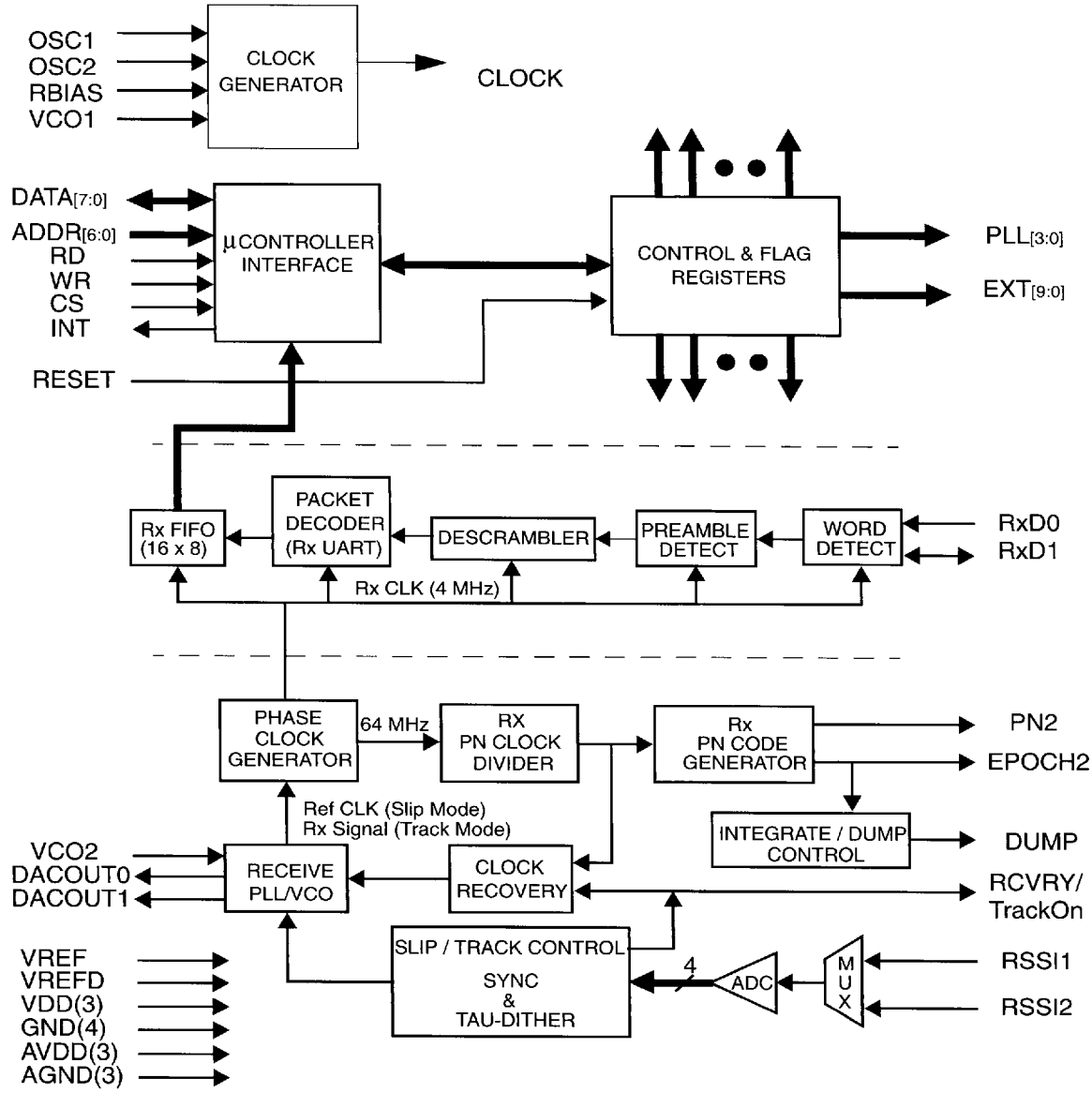
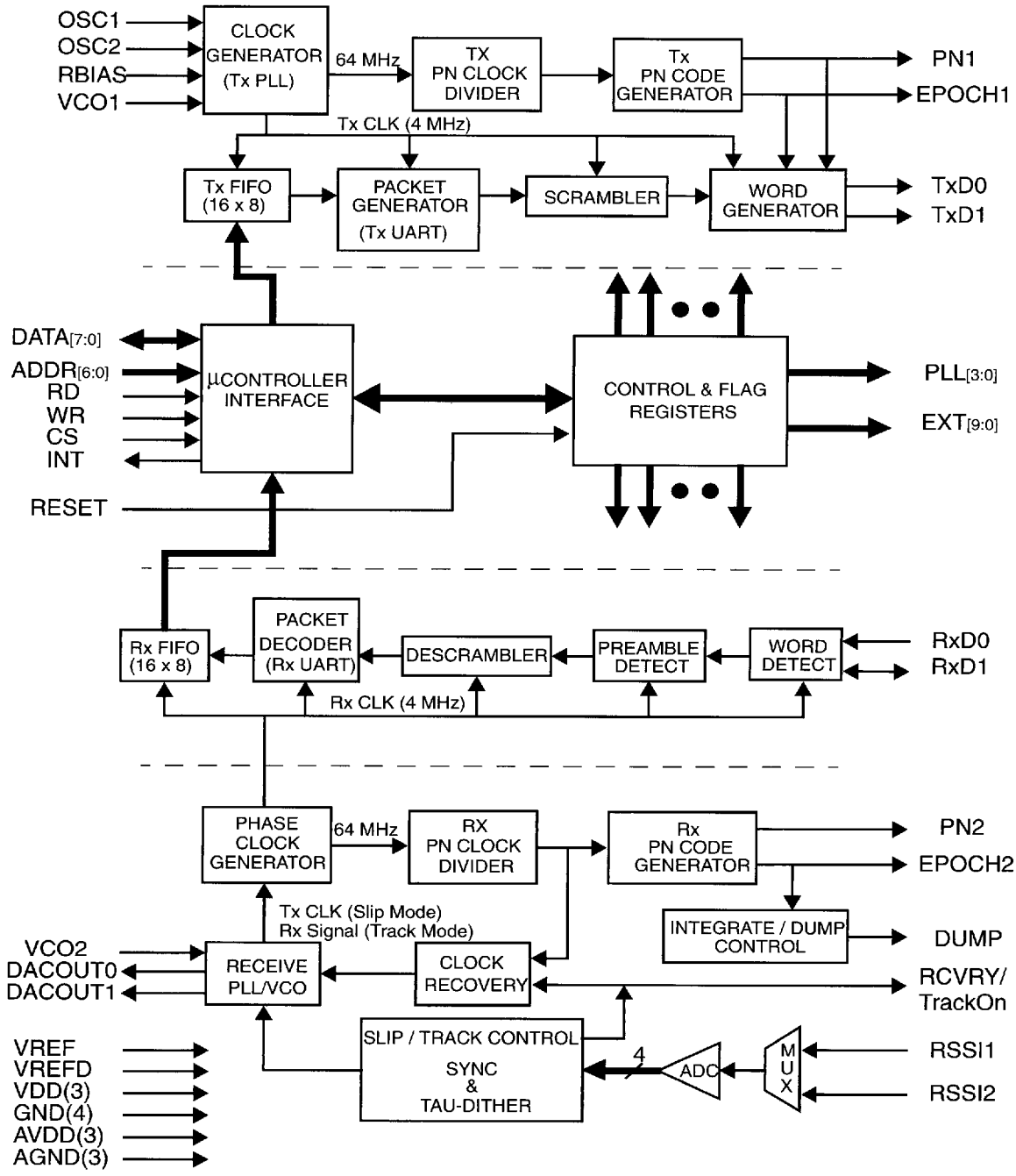


Figure 3: SX043 Transceiver Block Diagram Top Level



2.0 Package Availability

- SX041 available in a 52-lead PQFP.
- SX042 & SX043 available in a 64-lead PQFP, 64-lead TQFP and a 68-lead PLCC.

Table 1: Pin Descriptions

ICs	PIN NAME	TYPE	FUNCTION
ALL	AGND1	Analog GND	
ALL	GND1	ground	
ALL	VDD1	Vdd	
ALL	OSC1	input	Crystal Oscillator or external reference input. This input is divided by OSCDIV to generate the reference clock for the transmit PLL.
ALL	OSC2	padosc	Xtal Osc output.
ALL	PLL[3:0]	output	Off-Chip PLL programming; bit0, Enable1; bit1, Sclk, bit2, Enable0, bit3, Sdata.
SX041, SX043	TXD0	output	Transmit data "I" output.
SX041, SX043	TXD1	output	Transmit data "Q" output, or QAM output clock.
SX043	EPOCH1	output	Transmit PN Generator Epoch Signal. (68 PIN PLCC PACKAGE ONLY)
SX043	PN1	output	Transmit PN Generator output, can be internally disabled (PMR bit 4).
ALL	GND2	ground	
ALL	EXT[3:0]	output	External Control port (lower bits), User Defined Functions for radio control.
ALL	VDD2	Vdd	
SX042, SX043	EXT [7:4]	output	External Control port (upper bits), User Defined Function for radio control.
SX042, SX043	EXT[9:8]	output	External Control port (upper bits), User Defined Functions for radio control. (68 PIN PLCC PACKAGE ONLY)
ALL	INT	output	Active high. Initiates an interrupt to the microprocessor.
ALL	RESET	input	Active low. Sets all registers to default values and forces AMI's WavePlex ICs into standby states.
ALL	CS	input	Active low. Selects the chip for reading and writing via the uP interface.
ALL	RD	input	Active low. Initiates a read operation via the uP interface.
ALL	WR	input	Active low. Initiates a write operation via the uP interface.
ALL	GND3	ground	
ALL	DATA[7:0]	BiDirection	uP Interface data bus.
ALL	ADDR[6:0]	input	uP Interface address bus.
ALL	VDD3	Vdd	
ALL	GND4	ground	

Table 1: Pin Descriptions

ICs	PIN NAME	TYPE	FUNCTION
SX042, SX043	DUMP	output	Integrate & Dump Control logic output.
SX042, SX043	EPOCH2	output	Receive PN Generator Epoch Signal. (68 PIN PLCC PACKAGE ONLY)
SX042, SX043	PN2	output	Receive PN Generator output.
SX042, SX043	RCVRY	BiDirection	Clock recovery input for Narrow Band Mode. Track-On (active high) output for Spread Spectrum Mode. Indicates to external circuitry that the MODEL SX043 is locked and tracking the received PN code.
SX041	TEST	input	Pin for manufacturing test only. Should be tied to ground for normal operation.
SX042, SX043	RXD1	Analog I/O	Receive data input 'Q' or QAM mode output clock to external shift register.
SX042, SX043	RXD0	Analog In	Receive data input 'I'.
SX042, SX043	VREFD	Analog In	Reference voltage for integrate and dump comparators and switches.
ALL	AGND2	Analog GND	
SX042, SX043	VCO2	Analog Input	Receive VCO control voltage input.
ALL	AVDD2	Analog VDD	
SX042, SX043	DACOUT1	Analog Output	Receive DAC output during TRACK operation. Note: DACOUT0 and DACOUT1 are provided in the event separate gain control is necessary for SLIP and TRACK operation.
SX042, SX043	DACOUT0	Analog Output	Receive PLL DAC output during SLIP operation.
ALL	RBIAS	Analog Input	Current reference for DACs and analog buffers. Nominal resistor value of 20K ohm to AGND3.
ALL	VREF	Analog Input	Reference voltage for ADC and DACs. Value is mid-scale between VDD and GND.
ALL	AGND3	Analog GND	
SX042, SX043	RSSI1	Analog Input	Analog input to the ADC. Received Signal Strength Indicator from the RF receiver. Range is zero to VREF (full scale on internal ADC).
SX042, SX043	RSSI2	Analog Input	Analog input to the ADC. Received Signal Strength Indicator from the RF receiver. Range is zero to VREF (full scale on internal ADC).This input is not usable in "Slip" mode.
ALL	AVDD3	Analog VDD	
ALL	AVDD1	Analog VDD	
ALL	VCO1	Analog I/O	Transmit VCO voltage control input.

3.0 Electrical Specifications

3.1 Absolute Maximum Ratings

PARAMETER	MIN.	MAX.	UNITS
VDD/AVDD	-0.3	6.0	Volts
Input pin voltage, all pins	-0.3	VDD+0.3	Volts
Input pin current, all pins	-10	10	mA
Storage temperature	-55	125	°C
Lead temperature		300	°C for 10 sec.

NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these, or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

3.2 Operational Ranges

Applies to all following specifications unless otherwise specified.

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNITS
VDD/AVDD	Supply voltage		3	3.3	3.6	Volts
Ta	Operating temperature	Industrial	-40		85	°C
		Commercial	0		70	°C

3.3 DC Electrical Operating Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNITS
Vil	Input low voltage			0.25VDD	Volts
Vih	Input high voltage		0.7VDD		Volts
Vol	Output low voltage	Iol = 2mA		0.4	Volts
Voh	Output high voltage	Ioh = -1mA	2.4		Volts
Iil	Input leakage	Vin = 0 Volts to VDD/AVDD		±10	µA
Ioz	Output leakage	I/O = Hi impedance, Vout = 0 Volts to VDD/AVDD		±10	µA

3.4 Analog Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DAC LSB	DAC current source, least significant bit		10.3		µA
DAC ZERO	DAC current with 0 input			100	nA
DAC FULL SCALE Source and Sink	DAC current source, with HEX F input	±100	±155	±200	µA
DAC DIFF LIN	DAC differential nonlinearity		±0.1		LSB
ADC STEP1[1,2]	ADC FIRST STEP		130		mV
ADC LSB[2]	ADC least significant bit		103		mV
ADC FULL SCALE[2]	ADC Full Scale		1.56		V
ADC DIFF LIN[2]	ADC differential nonlinearity		±0.3		LSB
VCO GAIN[2]	VCO Gain		45		MHz/Volt
RXDRES[2]	RXD0/1 resistance		74		Ohms
CVIL[2]	Comparator input low voltage			1.5	Volts
CVIH[2]	Comparator input high voltage	1.8			Volts

Specified typical values are from characterization at 25°C, 3.3V AVDD, VDD.

NOTES 1. ADC STEP1 includes offset. Successive steps defined by ADC/LSB value.
2. Applies to SX042 and SX043 only.

3.5 IDD Characteristics

All IDD tests are done at AVDD=VDD=3.6V, 1 MPBS BPSK, 64 MHz chipping, Internal transmit PN code mixing A & B Gold codes, 50 pF load using the indicated condition.

SYMBOL	CONDITION	MIN.	MAX.	UNITS
ISLEEP	Sleep Mode		50	µA
ITXS	TX Standby		21	mA
IRXS[2]	RX Standby		38	mA
IALL[1]	Full Duplex		70	mA
IPN1[1]	Full Duplex with PN1 disabled		68	mA
ITXON1[3]	TX on, RX VCO off		41	mA
ITXON2[2]	TX on, RX VCO on		58	mA
IRXON[2]	RX on		58	mA

NOTES 1. SX043 only.
2. SX042 and SX043 only.
3. SX041 and SX043 only.

4.0 Microcontroller Interface Read/Write Timing

4.1 Read Timing Characteristics

See Figure 4: Read Timing Diagram.

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
Tcsd	Read chip select low to valid data out		60	nS
Trd	Read low to valid data out		60	nS
Tcsdz	Chip select high to data bus disable		25	nS
Trdz	Read high to data bus disable		25	nS
Tcsur	Read chip select setup	0		nS
Tchr	Read chip select hold	10		nS
Tadrsur	Read address setup	10		nS

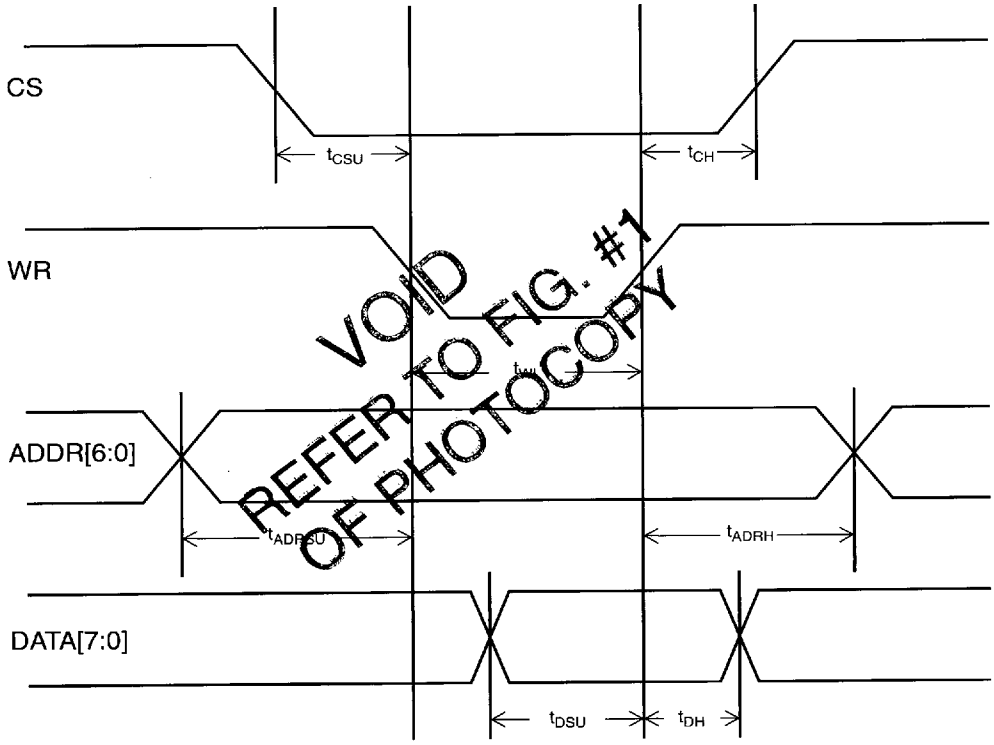
4.2 Write Timing Characteristics

See Figure 5: Write Timing Diagram.

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
Tcsuw	Write chip select setup	0		nS
Tchw	Write chip select hold	10		nS
Tadrsuw	Write address setup	10		nS
Tadrh	Write address hold	10		nS
Tdsu	Write data setup time	15		nS
Tdh	Write data hold	10		nS

For additional information please contact your nearest AMI representative for an Spread Spectrum IC User's Manual.

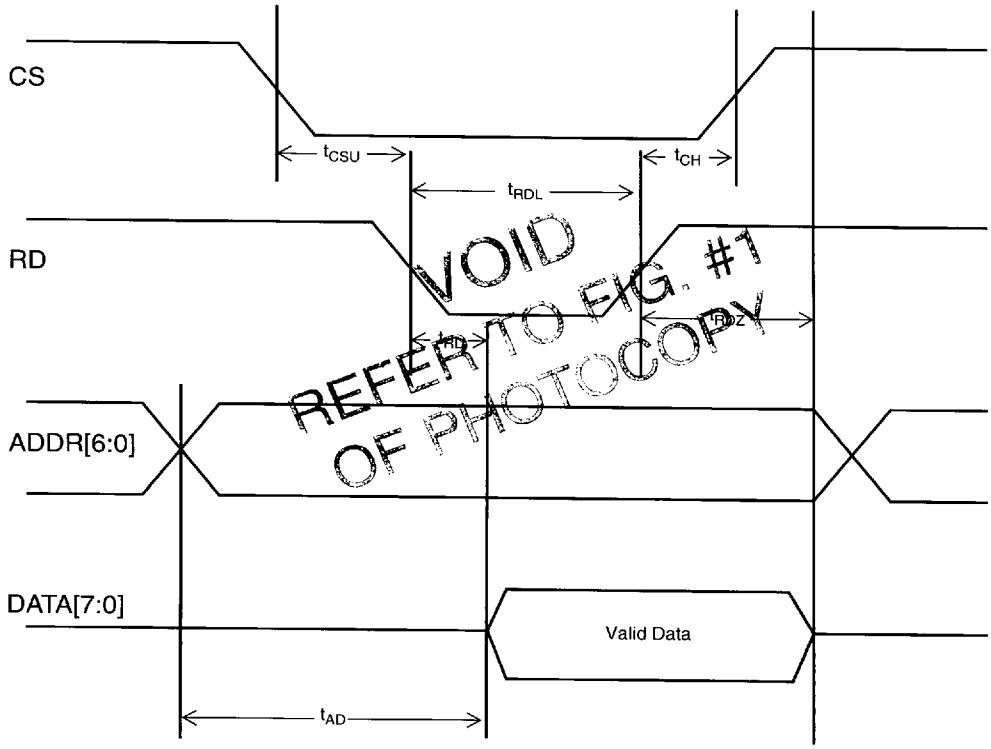
Figure 4: Microcontroller Write Timing



Write Timing Specifications

PARAMETER	MIN.	MAX.	UNITS
t_{CSU}	0		nSecs
t_{CH}	0		nSecs
t_{ADRSU}	5		nSecs
t_{ADRH}	5		nSecs
t_{DSU}	5		nSecs
t_{WL}	20		nSecs
t_{DH}	5		nSecs

Figure 5: Microcontroller Read Timing



Read Timing Specifications

PARAMETER	MIN.	MAX.	UNITS
t_{AD}		20	nSecs
t_{CSU}	0		nSecs
t_{CH}	0		nSecs
t_{RD}	5	40	nSecs
t_{RDZ}	0	10	nSecs
t_{RDL}	30		nSecs

1.0 Electrical Specifications – *5.0V*

1.1 Operational Ranges

Applies to all following specifications unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
VDD/AVDD	Supply voltage	4.5	5	5.5	Volts
Ta	Operating temperature	-40		85	°C

1.2 DC Electrical Operating Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNITS
Vil	Input low voltage			0.25VDD	Volts
Vih	Input high voltage		0.7VDD		Volts
Vol	Output low voltage	Iol = 2mA		0.4	Volts
Voh	Output high voltage	Ioh = -1mA	2.4		Volts
Iil	Input leakage	Vin = 0 Volts to VDD/AVDD		±10	µA
Ioz	Output leakage	I/O = Hi impedance, Vout = 0 Volts to VDD/AVDD		±10	µA
OSCI VIL*	Input low voltage			0.1LVDD	Volts
OSCI VIH*	Input high voltage		0.9VDD		Volts

**These levels are needed for both 3.3V and 5V versions on the OSCI input if it is being driven by an external clock.*

1.3 Analog Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DAC LSB	DAC current source, least significant bit		11.3		µA
DAC ZERO	DAC current with 0 input			100	nA
DAC FULL SCALE Source and Sink	DAC current source, with HEX F input	±100	±175	±250	µA
DAC DIFF LIN	DAC differential nonlinearity		±0.2		LSB
ADC STEP1[1,2]	ADC FIRST STEP		190		mV
ADC LSB[2]	ADC least significant bit		154		mV
ADC FULL SCALE[2]	ADC Full Scale		2.35		V
ADC DIFF LIN[2]	ADC differential nonlinearity		±0.50		LSB
VCO GAIN[2]	VCO Gain		45		MHz/Volt
RXDRES[2]	RXD0/1 resistance		60		Ohms
CVIL[2]	Comparator input low voltage			2.25	Volts
CVIH[2]	Comparator input high voltage	2.75			Volts

Specified typical values are from characterization at 25°C, 5.0V AVDD, VDD.

1.4 IDD Characteristics

All IDD tests are done at AVDD=VDD=5.0V, 1 MPBS BPSK, 64 MHz chipping, Internal transmit PN code mixing A & B Gold codes, 50 pF load using the indicated condition.

SYMBOL	CONDITION	MAX.	UNITS
ISLEEP	Sleep Mode	50	µA
ITXS	TX Standby	25	mA
IRXS[2]	RX Standby	45	mA
IALL[3]	Full Duplex	90	mA
IPN1[3]	Full Duplex with PN1 disabled	85	mA
ITXON1[4]	TX on, RX VCO off	65	mA
ITXON2[2]	TX on, RX VCO on	70	mA
IRXON[2]	RX on	70	mA

NOTES 1. ADC STEP1 includes offset. Successive steps defined by ADC/LSB value. 2. Applies to SX042 and SX043 only. 3. Applies to SX043 only. 4. Applies to SX041 and SX043 only.

2.0 Microcontroller Interface Read/Write Timing – *5.0V*

2.1 Read Timing Characteristics

See Figure 2: Read Timing Diagram.

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
Tcsd	Read chip select low to valid data out		45	nS
Trd	Read low to valid data out		45	nS
Tcsdz	Chip select high to data bus disable		15	nS
Trdz	Read high to data bus disable		15	nS
Tcsur	Read chip select setup	0		nS
Tchr	Read chip select hold	10		nS
Tadrsur	Read address setup	10		nS

2.2 Write Timing Characteristics

See Figure 1: Write Timing Diagram.

SYMBOL	PARAMETER	MAX.	UNITS
Tcsuw	Write chip select setup	0	nS
Tchw	Write chip select hold	10	nS
Tadrsuw	Write address setup	10	nS
Tadrh	Write address hold	10	nS
Tdsu	Write data setup time	10	nS
Tdh	Write data hold	10	nS

For additional information please contact your nearest AMI representative for a Spread Spectrum IC User's Manual.

Figure 1: Microcontroller Write Timing

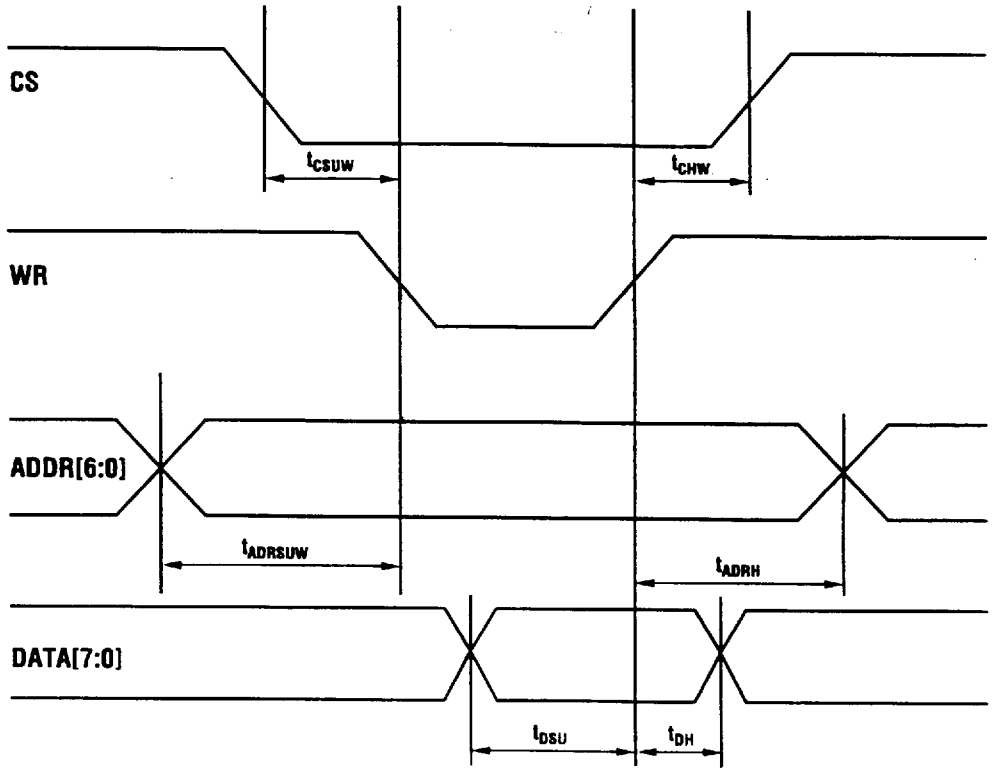


Figure 2: Microcontroller Read Timing

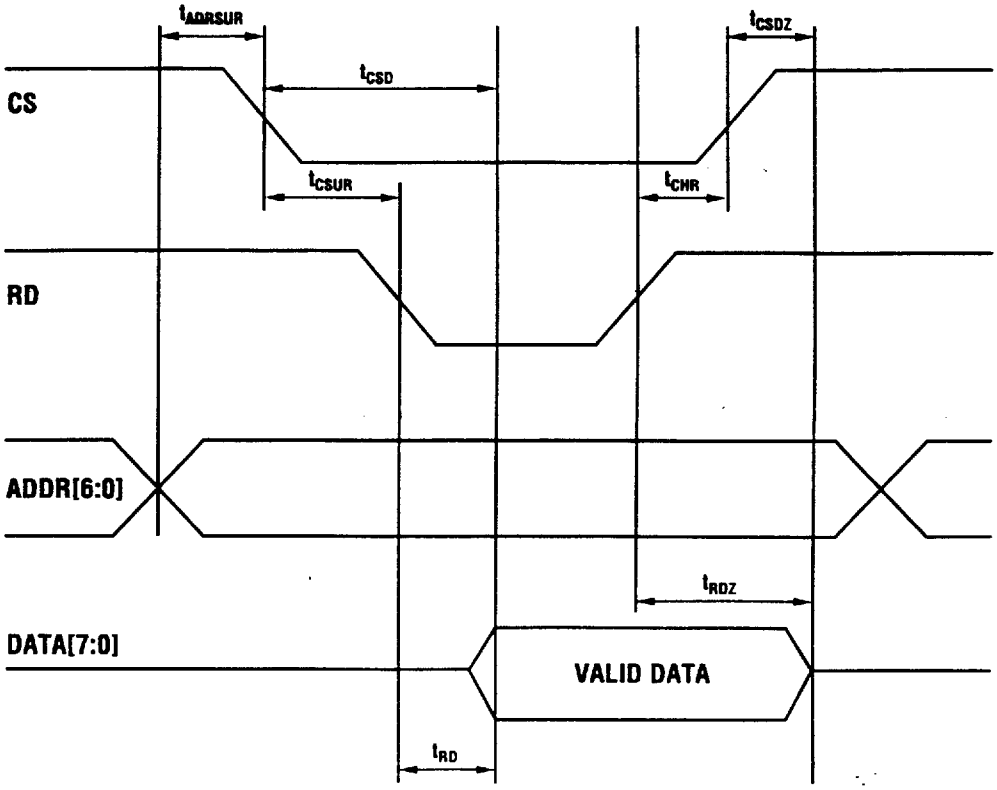


Figure 3: Input Test Waveforms and Measurment Levels

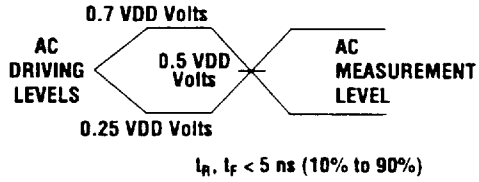


Figure 4: Output Test Load