MPEG-1 SYSTEM and VIDEO DECODER

FEATURES

- Single chip MPEG-1 System and Video Decoder, conforming to the MPEG-1 standard (ISO 11172-1,2)
- Highly integrated device:
  - Parses the MPEG-1 system bitstream and performs real-time decoding of video bitstreams at SIF resolution, (up to 384 pixels or 288 lines)
  - Synchronizes the MPEG-1 audio and video data
  - Includes the circuitry required for minimal-glue interfacing to host buses, and supports DMA or programmed I/O data transfer, 8 or 16 bits wide
- High quality of decoded video:
  - Accepts up to 5Mbits/second MPEG-1 system bitstream
  - Accepts up to 3Mbits/second MPEG-1 video bitstream
- Flexible video output:
  - Supports NTSC and PAL video timing standards
  - Provides progressive SIF-size or interlaced CCIR-size output
  - Provides several video output formats with optional pixel interpolation and field repetition: 24-bit RGB, 16-bit RGB (5,5,5 or 5,6,5), 16-bit YUV 4:2:2, 12-bit YUV 4:1:1
  - Provides brightness and contrast control
- Full support for stand-alone MPEG-1 applications:
  - Optional on chip sync generation
  - Provides outputs compatible with industry-standard digital video encoders
- Full support for video-CD 2.0:
  - Supports transfer to host of picture header user data
  - Decodes high-resolution still-image sequences (up to 704x576)
- On-chip support for synchronization of audio and video:
  - Decodes audio and video time stamps from the MPEG-1 multiplexed system bitstream
  - Provides programmable compensation for the total delays of the audio and video reconstruction chains
  - Maintains synchronization during freeze, single step and slow motion playback of video
  - Two serial output ports provide audio and private bitstreams to external decoders
- Includes special display modes and operating features:
  - Pause, freeze, single step
  - Slow motion, with slowdown factors of 2 to 7
  - Fast search
  - Random access
  - Video and audio stream selection on the fly
- Performs automatic frame rate conversion from all common MPEG picture rates to standard NTSC or PAL display frame rates, including 3/2 pulldown
- Provides serial port data pass-through (e.g., PCM audio)
- Includes error detection and concealment features
- Interfaces directly to DRAM:
  - Requires 4Mbits of 80ns or faster DRAM, supports 8Mbits DRAM
  - Supports two configurations, 256Kx16 or 4x256Kx4
- Occupies minimal PCB area:
  - Available in a 128 pin small-outline PQFP

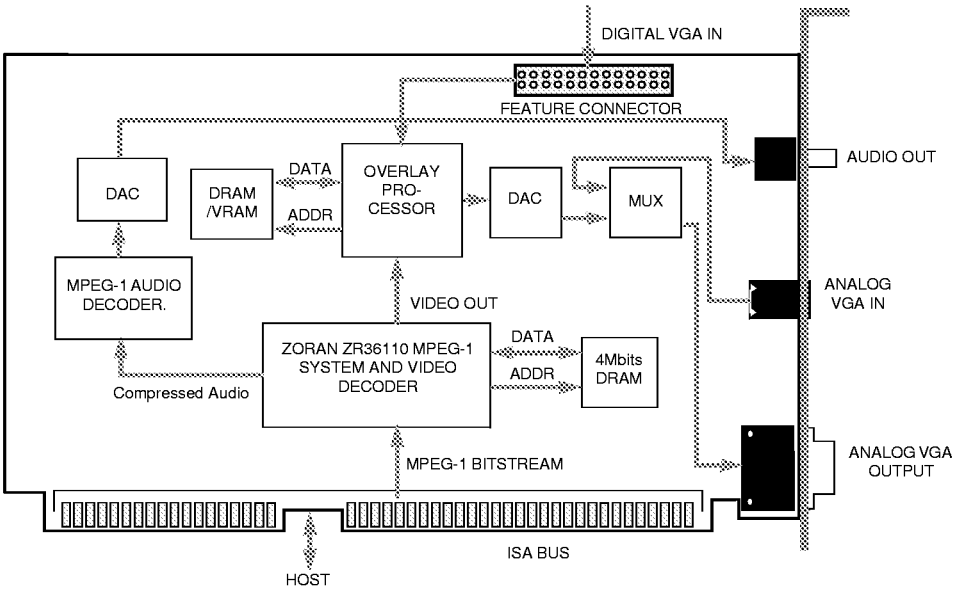


Figure 1. Block Diagram of a Typical MPEG-1 Playback Card

APPLICATIONS

- Entertainment and games
- Interactive training/education tools
- Video kiosks and karaoke systems
- Movie players
- Video-enhanced presentations
- Multimedia books and reference materials

INTRODUCTION

Zoran's ZR36110 MPEG-1 System and Video Decoder is targeted to the needs of developers of cost-sensitive MPEG-1 full-motion video playback products, both personal computer add-in cards and stand-alone consumer Video CD players.

In addition to being a full-motion MPEG-1 video decoder, the ZR36110 is an MPEG-1 system-layer decoder and audio-video synchronizer. In this capacity, it demultiplexes the MPEG system bitstream, extracts the time stamps from the individual video and audio bitstreams, buffers both the compressed audio and video data, and provides the audio data to the input of an external audio decoder, all while maintaining full synchronization of audio and video, and compensating for any differences in processing delay of the audio and video decoders. Support from a host controller is minimal, confined mainly to initialization of the ZR36110 for decoding of the desired MPEG bitstream. During the decoding itself, the host controller is only required to feed the bitstream to the decoder while monitoring its status, and optionally giving it on-line commands to enter one of the special decoding modes, but is not required to perform continuous parsing of the bitstream.

A block diagram of a personal computer MPEG add-in board employing the ZR36110 is shown in Figure 1. This application typifies the interconnection of components in an MPEG decoding system featuring the ZR36110. In this example, the host controller for the ZR36110 is the personal computer's CPU, which initializes the decoder and transfers the bitstream to it. If the host system has a DMA controller, this can be used for the bitstream data transfer, thus reducing the load on the CPU to a minimum.

The decoded video, including appropriate sync signals, is sent to a display control circuit, in this case the overlay processor, where it is scaled to fit a window in the computer's graphics display and provided to the DAC with appropriate timing derived from the graphics card's syncs and pixel clock. The output of the DAC is multiplexed with the analog output of the graphics card to create the effect of MPEG video in a graphics window. Alternatively, the video output of the ZR36110 can be connected directly to a video encoder whose composite video output is suitable for display on a television monitor.

The MPEG audio stream, extracted from the multiplexed bitstream and correctly synchronized with the displayed video by the ZR36110, is passed in bit-serial form to the audio decoder. The analog audio can be connected directly to an audio amplifier and speakers, or to the auxiliary input of the computer's sound system.

FUNCTIONAL DESCRIPTION

Figure 2 is a simplified block diagram of the ZR36110, showing the major functional blocks and their interfaces to the host controller, video display, audio decoder and external DRAM.

Host Interface

The MPEG bitstream is transferred to the ZR36110 through its host bus, a parallel interface typically connected to a host microprocessor. The host interface is also used for initialization of the device prior to starting the MPEG decoding, for on-line commands from the host to start decoding and while decoding is in progress, and for status readout during the initialization and decoding phases.

The host interface has a flexible configuration that allows it to be connected with minimal glue logic to a variety of bus types. It has a 16-bit data bus and two address lines. The byte order on the 16-bit bus is selectable, to conform with either the Intel or Motorola conventions. The bus can also be configured to operate with a width of 8 bits. Two handshake modes are supported for the bitstream transfer, a programmed I/O mode in which the bitstream port is addressed directly by the host CPU, and a mode suitable for DMA. Initialization, on-line commands and status readout always use the programmed I/O mode of access.

System Bitstream Demultiplexing

The System Bitstream Demultiplexer separates the MPEG-1 bitstream into its elementary streams - the video and audio streams or the two optional private data streams. These elementary streams are stored in buffers in the DRAM: one buffer for the video stream data and two buffers for any combination of audio or private data. In addition to MPEG system bitstreams, the system bitstream demultiplexer can be configured to deal with input from the host interface consisting of an MPEG video-only or audio-only elementary bitstream. The ZR36110 can also "pass through" (convert from parallel to serial) other audio bitstreams (e.g., 2*16 bit stereo PCM) or any other bitstream with a constant bit rate output not greater than 1.412 Mbits/second. In these cases, it clearly does not have to perform any demultiplexing, but only stores the incoming data in the DRAM buffer.

The video and audio (or private) elementary streams are extracted concurrently from the buffers in DRAM by the Video Decoder and Audio Synchronizer, respectively.

Video Decoding

The Video Decoder computes the motion vectors, and the Huffman-decoded transform coefficients subsequently undergo dequantization, rescaling, inverse discrete cosine transformation, and motion compensation. Reconstructed pictures are buffered as needed in the DRAM, to be read out later in the correct display order.

Video Post Processing

The reconstructed pictures are stored in DRAM in the native progressive SIF 4:2:0 format of MPEG-1, in which each 2 x 2 array of luminance samples is associated with one chrominance sample pair. Before being output through the video interface, they are post-processed by the Video Post Processor and, optionally, the Color Space Convertor, to produce video in one of a number of commonly used pixel representations and one of two raster size options.

The video format (size and representation) options are:

- Progressive SIF-size, with 16-bit 2:1:1 YUV, 24-bit 2:2:2 RGB, 16-bit (5,6,5) 2:2:2 RGB, or 15-bit (5,5,5) 2:2:2 RGB pixels
- Interlaced CCIR-size, with 16-bit 4:2:2 YUV, 12-bit 4:1:1 YUV, 24-bit 4:4:4 RGB, 16-bit (5,6,5) 4:4:4 RGB, or 15-bit (5,5,5) 4:4:4 RGB pixels

The term "CCIR-size" is used here to denote a video frame whose vertical and horizontal dimensions are each twice that of the original MPEG picture. Typically but not necessarily, the pixel clock frequency and number of pixel clocks per line are as specified in CCIR601. The term is used interchangeably for square-pixel or other similar (non-CCIR601) formats.

When interlaced CCIR-size output is selected, the SIF-size pictures are doubled in size horizontally, and (except when performing frame rate conversion, see below) the same picture is output in both fields. Conversion from the native 4:2:0 pixel format to any of the supported representations entails reconstruction of missing rows of chrominance samples; this is done by duplication of the existing rows. In all cases for which missing samples must be reconstructed to double the size horizontally, this can optionally be done by duplication or by interpolation using a two-tap filter. This includes reconstruction of chrominance samples for the RGB representation, and reconstruction of chrominance and luminance for the doubling to CCIR-size fields.

The ZR36110 is also automatically configured for decoding of high-resolution still-image sequences. In this case, the decoding is not done in real time. These sequences have each still image encoded as one picture up to double the horizontal and vertical resolution of standard SIF. The video post-processor and output interface are configured for interlaced CCIR-size operation. For high-resolution PAL (704 pixels x 576 lines), 8 Mbits (2 DRAM banks) may be required.

Video Timing and Sync Generation

The video sync signals have dual significance in the ZR36110. The horizontal and vertical sync signals provide the raster timing for the post-processed video output; the vertical sync signal also determines the rate at which the pictures are decoded from the bitstream.

The sync signals can be configured as inputs, in which case they are driven by an external sync generator. More commonly, the ZR36110's internal sync generator is used as the master sync generator, and the sync signals are configured as outputs. The sync generator is highly programmable, and is capable of generating the standard interlaced NTSC and PAL raster formats, as well as a wide variety of other interlaced and progressive formats.

The ZR36110 supports cropping of the decoded picture, so that the active displayed region can optionally be smaller than the decoded picture. With the exception of some necessary restrictions, the active region can be positioned anywhere within the display raster defined by the vertical and horizontal sync signals. The display region outside the active region, except for the horizontal and vertical blanking regions, is filled with a user-specified background color.

Video decoding in the ZR36110 is tightly synchronized to the vertical sync signal. That is, it decodes pictures from the video stream, and thus consumes the video stream (and consequently the whole MPEG system bitstream), at a rate which bears a fixed relationship to the video frame rate. Nominally, this picture decoding rate is the same as the video frame rate. When, however, the video interface is configured for interlaced CCIR-size output, the ZR36110 is also capable of performing conversions from commonly used picture rates to the standard PAL and NTSC frame rates. A simple example of rate conversion supported is 3/2 pulldown, in which a 23.976 pictures/sec video bitstream is decoded, and output at the NTSC rate of 29.97 frames/sec, by displaying each decoded picture during two or three fields in an alternating sequence. This achieves the required ratio of two decoded pictures for every five output fields.

One consequence of the tight coupling of the bitstream consumption rate to the vertical sync rate is that, if the bitstream is provided to the ZR36110 at a constant rate over which it has no control, the master video clock of the ZR36110 should be locked to the bitstream clock to ensure continuous operation without glitches. On the other hand, in a computer environment, where the bitstream can be provided on request, there is no such requirement to lock the clocks.

Serial Ports

The audio or private data from each of the buffers in the DRAM is assigned to one of the two serial output ports. The data is read out of the buffer and output from the serial port at a constant user-programmed rate, which, in the case of an audio stream, is equal to the audio bit rate. The audio decoder connected to the serial port must be able to accept and decode the serial stream at the rate provided by the ZR36110. Since the ZR36110 decodes the video, and consumes the system bitstream, at a rate which is determined by the vertical sync frequency, this usually means that the audio decoder's output sampling clock must be locked to the ZR36110's video clock.

Synchronization of audio and video is achieved by timing the start of audio bitstream output from the serial port, relative to the start of video decoding. The starting time is computed from the time stamps embedded in the MPEG system bitstream. Thereafter, synchronization is maintained automatically.

Microcoded Architecture

The ZR36110 comprises a number of hard-wired functional units operating in conjunction with, and under control of, a programmable microcoded unit. Microcode for all the modes and options contained in this data sheet is provided by Zoran. Users are also advised to consult the ZR36110 microcode release notes for information on new features that are added from time to time.

To initialize the ZR36110 for decoding, the host system must load the microcode, and also a 128-byte array of set-up parameters that configure the hard-wired functional units and microcode.

On-line Commands and Special Playback Modes

Once it is initialized, the behavior of the ZR36110 is controlled by the host by means of on-line commands. The commands supported are for the basic playback functions of starting, pausing, continuing and ending decoding, and also the following special playback modes and parameter changes:

Mode Change On-line Commands

- *Pause stream:* stop video decoding and audio output and freeze the display
- *Single step:* step to the next picture and pause
- *Decode to first I picture:* decode and display until the next I picture is displayed, then pause
- *Decode to next I picture:* freeze the displayed picture and continue decoding until the next I picture, then display it and pause
- *Fast search:* decode and display only certain types of pictures
- *Slow motion:* decode and display with a slowdown factor of 2 to 7
- *Freeze frame:* continue decoding while displaying the same frame
- *Random access:* start or restart decoding at a random location in the bitstream

Parameter Change On-line Commands

- Change brightness of the output video
- Change contrast of the output video
- Change stream I.D. of the active video stream or audio streams

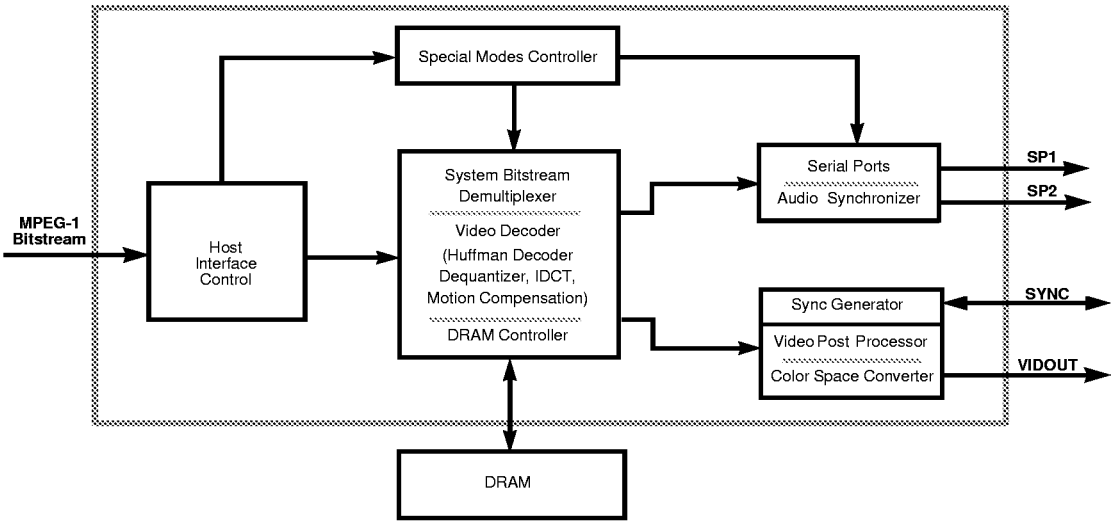


Figure 2. Simplified Block Diagram

SIGNAL DESCRIPTION

Name	Type	Description
VCC (5V)	S	5 volt power supply inputs.
VSS (0V)	S	Power supply ground inputs.
GCLK	I	General Clock input. Used by the internal PLL to generate the ZR36110's internal processing clock (PCLK). When $\overline{MB4}$ is low, the PLL multiples GCLK by 4, and the allowed frequency range of GCLK is 13.5MHz to 15.18MHz. When $\overline{MB4}$ is high, the PLL multiples GCLK by 9/2, and the allowed frequency range of GCLK is 12.0MHz to 13.5MHz. In most applications, the VCLK and GCLK pins can be tied together. If the internal crystal oscillator is used, with a crystal connected between GCLK and XT, a 20pF capacitor must be connected between GCLK and VSS.
XT	O	Crystal oscillator output. Instead of using an external clock generator connected to GCLK, a parallel resonant crystal of the required frequency may be connected between GCLK and XT for clock generation. If a crystal is not used, this pin should be left unconnected. If a crystal is used, a 20pF capacitor must be connected between XT and VSS.
$\overline{MB4}$	I	Input signal used to select the multiplication ratio of the PLL. Low selects a ratio of 4 and high selects a ratio of 9/2.
PCLK	O	Output signal used to monitor the ZR36110's internal processing clock. Used for test purposes only.
$\overline{RESET}$	I	Active low reset input. Reset operation is described in the *Reset and Standby Power* section of this document.
$\overline{STDBY}$	I	Active low input that drives the chip to the Standby state, forcing all output signals to float. In Standby the chip consumes a minimal amount of power. For operating restrictions when STDBY is activated, see the *Reset and Standby Power* section of this document.
IDLE	O	An active high output signal, activated by the ZR36110 after Reset or after the decoding of a sequence has ended. The ZR36110 deactivates the IDLE signal after receiving the **GO** on-line command.
VIDOUT (23:0)	O	24-bit output bus used to output the video data. The data has one of several sizes and formats with different color space, width, and sub-sampling configurations.

Name	Type	Description
VCLK	I	Video clock input. Synchronizes the VIDOUT bus and video sync signals (HSYNC, VSYNC, FI_EN). VCLK is the pixel clock when the video output mode is Interlaced CCIR-size and also in the special Enabled video output mode. VCLK can optionally be configured to be the pixel clock when the video output mode is Progressive SIF-size. When a serial port clock is configured as an output, it is derived by integer division from VCLK.
QCLK_V	O	In the normal video output modes, this is an output clock signal derived by dividing VCLK by 4. QCLK_V can optionally be configured to be the pixel clock when the video output mode is Progressive SIF-size. In the special Enabled video output mode, this is an active high signal indicating that the video output FIFO contains at least 8 valid pixels.
HSYNC	I/O	A signal indicating the beginning of a line on the VIDOUT bus. HSYNC can be configured to be active high or active low, short or long, input or output.
VSYNC	I/O	A signal indicating the beginning of a field or frame on the VIDOUT bus. VSYNC can be configured to be active high or active low, short or long, input or output.
FI_EN	I/O	This signal can be programmed for one of four functions. It can be an input or output signal that indicates the field (Field I or Field II) being output. This signal is relevant only for interlaced video output. *Note*: Field I is defined to be the field that starts at the beginning of a line, while Field II is defined to be the field that starts at the middle of a line. It can be an output, active low, composite blanking signal. It can be an output, active low signal, meaning that decoded pictures are high resolution stored with full resolution. In the Enabled video output mode, this signal is an input, used as an enable signal for the video output.
BUSDAT (15:0)	B	16-bit host interface bus. The MPEG bitstream, set-up parameters, microcode and on-line commands are all transferred to the ZR36110 over this bus. Status is read back to the host using bits 7:0. Lines 15:8 are output zero when read.
BUSADD (1:0)	I	2-bit input host address bus.
DREQ	O	Active high output control signal requesting data transfer from the host in DMA mode.
$\overline{\text{DACK}}$	I	Active low input control signal acknowledging the request of data transfer from the host in DMA mode.
$\overline{\text{BUSWR}}$	I	Host interface write strobe.
$\overline{\text{BUSRD}}$	I	Host interface read strobe.
$\overline{\text{BUSCS}}$	I	Host interface chip select.
READY	O	Active high output host bus control signal permitting data transfer from the host in I/O mode.
RAMDAT (15:0)	B	16-bit bidirectional bus used to transfer data between the ZR36110 and the external DRAM.
RAMADD (8:0)	O	9-bit output bus used by the ZR36110 for addressing the external DRAM.
$\overline{\text{RAS}}$	O	Active low output control signal used by the ZR36110 to specify the DRAM row address and enable the transfer of data between the ZR36110 and the DRAM.
$\overline{\text{CAST}}$	O	Active low output control signal used by the ZR36110 to specify the DRAM column address and initiate the transfer of data between the ZR36110 and the DRAM.
$\overline{\text{CAS2}}$	O	Active low output control signal used by the ZR36110 to specify the DRAM column address and initiate the transfer of data between the ZR36110 and the second DRAM bank (i.e., when 8 Mbits are used). Otherwise, it should not be connected.
$\overline{\text{WE}}$	O	Active low output control signal used by the ZR36110 to specify whether the transfer of data between the ZR36110 and the external DRAM buffer is a write operation ($\overline{\text{WE}}$ low) or a read operation ($\overline{\text{WE}}$ high).
SP1DAT	O	Output signal for serial port 1 data. Serial port 1 data can be assigned to an audio stream, or one of the two private bitstreams.
SP1CLK	I/O	Serial port 1 clock. Can be programmed to be either an input or an output.

Name	Type	Description
SP1FRM	O	Output frame synchronization signal for data output from serial port 1.
SP2DAT	O	Output signal for serial port 2 data. Serial port 2 data can be assigned to an audio stream, or one of the two private bitstreams.
SP2CLK	I/O	Serial port 2 clock. Can be programmed to be either an input or an output.
SP2FRM	O	Output frame synchronization signal for data output from serial port 2.

Key to signal types: S -power supply; I - input only; O - output only; B - bi-directional bus; I/O - configurable as input or output.

TYPICAL CIRCUIT DIAGRAM

Figure 3 is a generic schematic showing the connections of the ZR36110 to a host microcontroller, video display circuit, decoders of serial port data, DRAM, clock generator, and general system control circuits.

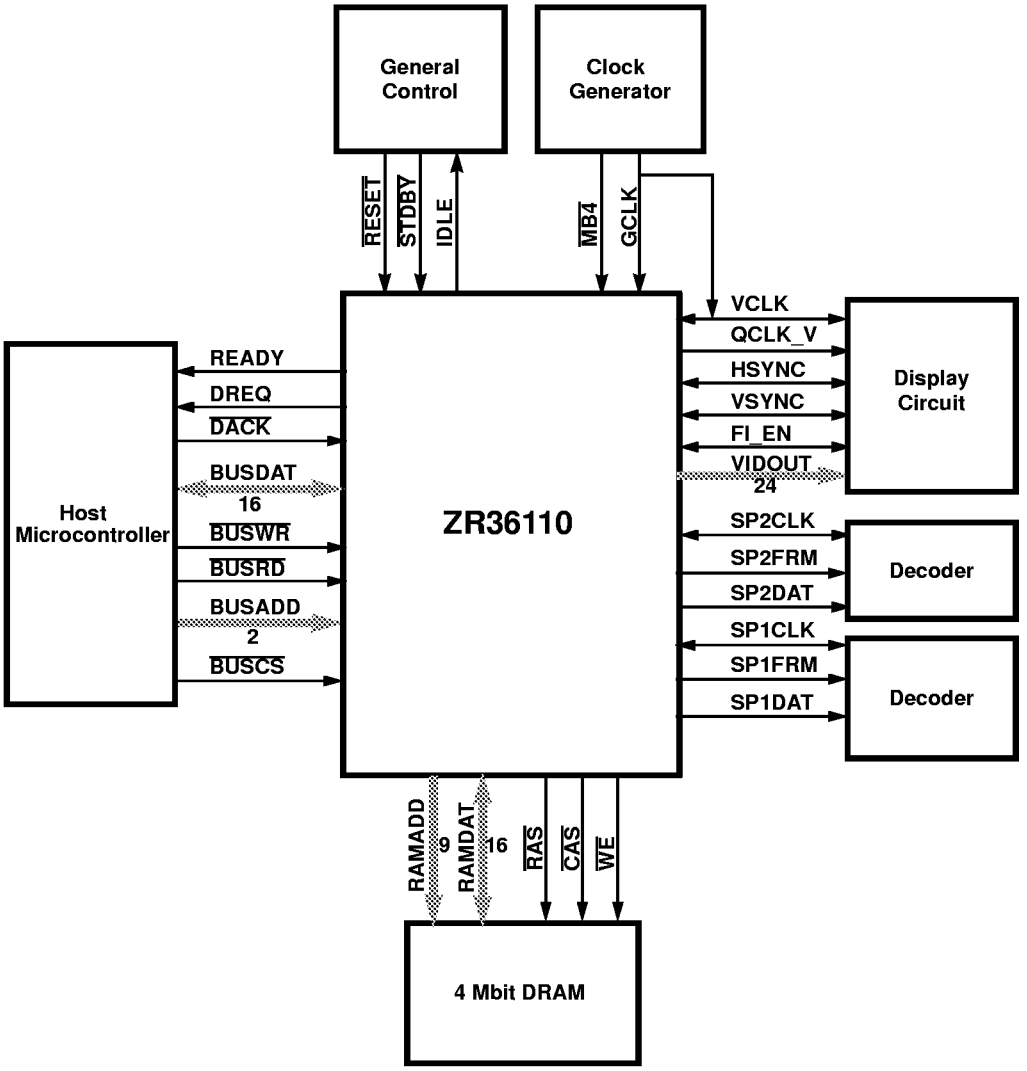


Figure 3. Generic ZR36110 Schematic Diagram

An actual implementation could differ from this in a number of typical ways:

- Only one serial port is typically used, connected to an audio decoder.
- The video sync signals, HSYNC and VSYNC, are either outputs or inputs, depending on whether the ZR36110's internal or an external sync generator is used. Depending on the video interface mode, a subset of the 24 bits of the VIDOUT bus may be used, and the QCLK_V and FI_EN signals may be unused.
- DREQ and $\overline{\text{DACK}}$ are only used if the bitstream is transferred by the host in DMA mode.
- 8 bits of the BUSDAT bus are unused if the host interface is always operated in its 8-bit configuration.
- The READY and IDLE signals may be unused since their states are available to the host via a status register.
- VSYNC is typically provided as an interrupt to the host controller, to maintain synchronization of the host software with the decoding of the MPEG bitstream.

SUPPORTED BITSTREAMS

The ZR36110 can be configured to accept the MPEG-1 bitstream in one of three forms:

- System bitstream, with multiplexed video and/or audio and/or private streams as defined in ISO 11172-1,2,3
- Video-only bitstream, that is, containing only the elementary video stream data as defined in ISO 11172-2
- Audio-only bitstream, that is, containing only the elementary audio stream data as defined in ISO 11172-3

The bitstream must be byte-aligned as supplied to the host interface.

In addition, the ZR36110 can be configured to accept non MPEG-1 bitstreams for output through its serial port. These bitstreams, together with the audio-only bitstreams, are called, collectively, serial port-only bitstreams.

For a bitstream to be decoded properly, or passed through properly, it must obey the following restrictions.

Note: Numbers in [ ] are for high resolution still images.

System (multiplexed) bitstream

The ZR36110 decodes any legal MPEG-1 system bitstream which conforms to the ISO 11172-1 standard and obeys the following restrictions.

System Header

1. rate_bound - Less than or equal to 13107 (in 50 bytes/sec units, equivalent to 5Mbits/sec).

Pack Header

2. mux_rate - Less than or equal to 13107 (in 50bytes/sec units, equivalent to 5 Mbits/sec).

Packet Header

3. STD_buffer_size -
   - Less than or equal to 32 if STD_buffer_scale is 0 and the preceding stream_id is 110b bbbb (they always go together in the packet header). This is equivalent to 4Kbytes input buffer for the audio or private1 streams.
   - Less than or equal to 46 [224], if STD_buffer_scale is high and the preceding stream_id is 1110 bbbb (they always go together in the packet header). This is equivalent to 46Kbytes [224 Kbytes] input buffer for the video bitstream.
   -
4. The packet rate must be less than or equal to 300 per second.

Video bitstream (video-only, or the elementary video stream multiplexed in a system bitstream)

The ZR36110 decodes any legal MPEG-1 video bitstream which conforms to the ISO 11172-2 standard and obeys the following restrictions.

Sequence Header

1. horizontal_size - Less than or equal to 384 [704]. Minimum value is 32.
2. vertical_size - Less than or equal to 288 [576]. Minimum value is 32. The product int((HS+15)/16)*int((VS+15/16) is restricted to be less than or equal to 396 [1584] if pps=25, or 330 [1320] if pps is otherwise.
3. picture_rate - The picture rate codes supported are: 0001 (23.976 pps), 0010 (24 pps), 0011 (25 pps), 0100 (29.97 pps), 0101 (30 pps).
4. bit_rate - Less than or equal to 7865 in 400 bits/sec units, equivalent to 3 Mbits/sec.
5. vbv_buffer_size - Less than or equal to 20 [112] in 16Kbits units, equivalent to 40Kbytes [224 Kbytes].
6. A video stream within a system-multiplex bitstream may include more than one sequence, i.e., after a video sequence end code, a new sequence may start. In such a case, the HS and VS parameters must be the same for all sequences within the video stream.

Picture Header

7. picture_coding_type - Not equal to 4, i.e. no sequences with D-pictures.

Audio bitstream (audio-only, or multiplexed in a system bitstream)

The ZR36110 passes through its serial port, to the audio decoder device, any legal MPEG-1 audio bitstream which conforms to the ISO 11172-3 standard (Layer I and II) and obeys the following restrictions: The bitrate_index, layer and sampling_frequency parameters of all frames must have the same values as in the first frame. Free bit rate, that is, bitrate_index=0, is not allowed.

Private1 bitstream (multiplexed in a system bitstream)

The ZR36110 passes through its serial port any legal MPEG-1 private1 bitstream which conforms to the ISO 11172-1 standard and obeys the following restrictions.

8. Maximum bit rate less than or equal to the maximum bit rate allowed for audio bitstreams in ISO 11172-3.
9. Maximum buffer size less than or equal to 4Kbytes.

Private2 bitstream (multiplexed in a system bitstream)

The ZR36110 passes through its serial port any legal MPEG-1 private2 bitstream which conforms to the ISO 11172-1 standard and obeys the following restrictions.

10. Maximum bit rate less than or equal to the maximum bit rate allowed for audio bitstreams in ISO 11172-3.
11. Maximum buffer size is less than or equal to 4Kbytes.

Serial port-only bitstream

The ZR36110 passes through its serial port any bitstream which obeys the following restrictions.

12. Constant bit rate less than or equal to 1,411,200 bits/sec.

SET-UP PARAMETERS

The set-up parameters of the ZR36110 consist of 128 bytes of data, divided up as follows:

- 7 single-byte parameters, 6 of which are further divided into single-bit or multi-bit sub-fields, configure the decoding system and interfaces
- 22 parameters (38 bytes) control the display (sync raster and video output)
- 8 parameters (19 bytes) control timing and delays
- 3 parameters (3 bytes) control video and audio stream selection
- 61 additional bytes, here designated as reserved. Some of these may be assigned to new functions implemented in the microcode and not described in this data sheet; the most current parameter assignments are specified in the ZR36110 microcode release notes. If unused, the reserved bytes must be loaded with the value zero.

The complete 128-byte array must always be loaded whenever a change to any parameter is required, for example when a sequence has ended and a new sequence with different MPEG parameters must be decoded.

Some of the parameter fields have default values, which are preset to a given value during a cold reset (cold reset is defined in the *Reset and Standby Power* section). The only parameters that have default values are those needed to specify signal directions for bidirectional lines to avoid contention, and to define the initial configuration of the host interface.

Some of the parameters and bit fields, designated "fixed parameter", or "fixed bit," may not be changed without a cold reset. These parameters pertain generally to the overall system configuration. All parameters with default values are also defined to be "fixed" in this sense.

The set-up parameters are listed in Table 1.

Table 1. Set-up parameters

Byte No. (Hex)	Symbol	Brief description
00	BUSMODE	Host bus mode
01	BUSOFF	Request off timing (in DMA mode)
02	SYSMODE	Decoding system mode
03	VIDMODE	Video output mode
04	SYNMODE	Video synchronization mode
05	SPOMODE	Serial ports mode
06	EXTMODE	Extension of other mode parameters
07		Reserved
08	NAP (m.s.)	Number of active pixels per line
09	NAP (l.s.)	Number of active pixels per line
0A	NOP (m.s.)	Number of offset pixels per line
0B	NOP (l.s.)	Number of offset pixels per line
0C	NTP (m.s.)	Number of total pixels per line
0D	NTP (l.s.)	Number of total pixels per line
0E	NBP (m.s.)	Number of blank pixels per line
0F	NBP (l.s.)	Number of blank pixels per line

Table 1. Set-up parameters (continued)

Byte No. (Hex)	Symbol	Brief description
10	NBPF (m.s.)	Number of front blank pixels per line
11	NBPF (l.s.)	Number of front blank pixels per line
12	NDP (m.s.)	Number of delay pixels per line
13	NDP (l.s.)	Number of delay pixels per line
14	NAL (m.s.)	Number of active lines per picture
15	NAL (l.s.)	Number of active lines per picture
16	NOL (m.s.)	Number of offset lines per picture
17	NOL (l.s.)	Number of offset lines per picture
18	NTL (m.s.)	Number of total lines per frame
19	NTL (l.s.)	Number of total lines per frame
1A	NBL (m.s.)	Number of blank lines per field [frame]
1B	NBL (l.s.)	Number of blank lines per field [frame]
1C	NBLF (m.s.)	Number of front blank lines per field [frame]
1D	NBLF (l.s.)	Number of front blank lines per field [frame]
1E	NDL (m.s.)	Number of delay lines per field [frame]
1F	NDL (l.s.)	Number of delay lines per field [frame]
20	HSW	Width of horizontal sync signal (in pixels)
21	VSW	Width of vertical sync signal (in lines)
22	CRV (m.s.)	V to R color space conversion coefficient
23	CRV (l.s.)	V to R color space conversion coefficient
24	CBU (m.s.)	U to B color space conversion coefficient
25	CBU (l.s.)	U to B color space conversion coefficient
26	CGV (m.s.)	V to G color space conversion coefficient
27	CGV (l.s.)	V to G color space conversion coefficient
28	CGU (m.s.)	U to G color space conversion coefficient
29	CGU (l.s.)	U to G color space conversion coefficient
2A	BGRV	R or V component of the background color

Table 1. Set-up parameters (continued)

Byte No. (Hex)	Symbol	Brief description
2B	BGGY	G or Y component of the background color
2C	BGBU	B or U component of the background color
2D	FIL	Value output on bits 23:16 of VIDOUT
2E	SP1BR (m.s.)	Serial port 1 bit rate ratio
2F	SP1BR	Serial port 1 bit rate ratio
30	SP1BR (l.s.)	Serial port 1 bit rate ratio
31	SP2BR (m.s.)	Serial port 2 bit rate ratio
32	SP2BR	Serial port 2 bit rate ratio
33	SP2BR (l.s)	Serial port 2 bit rate ratio
34	SP1CD (m.s.)	Divisor of VCLK for SP1CLK
35	SP1CD (l.s.)	Divisor of VCLK for SP1CLK
36	SP2CD (m.s.)	Divisor of VCLK for SP2CLK
37	SP2CD (l.s.)	Divisor of VCLK for SP2CLK
38	SP1DL (m.s.)	Serial port 1 delay
39	SP1DL (l.s.)	Serial port 1 delay
3A	SP2DL (m.s.)	Serial port 2 delay
3B	SP2DL (l.s.)	Serial port 2 delay
3C	VOD (m.s.)	Video output delay
3D	VOD (l.s.)	Video output delay
3E	VCLK (m.s.)	VCLK rate (Hz)
3F	VCLK	VCLK rate (Hz)
40	VCLK (l.s.)	VCLK rate (Hz)
41	Reserved	
42	SP2SID	Serial port 2 stream I.D.
43	SP1SID	Serial port 1 stream I.D.
44	VIDSID	Video stream I.D.
45 - 7F	Reserved	

Key: l.s. indicates the least significant byte, m.s. indicates the most significant byte of a multi-byte parameter.

Configuration Parameters

BUSMODE

This byte configures the host interface. It contains the following sub-fields.

- **BSWD** (bit 7) - host bus width.
  This bit defines the active width of the host bus, either 8 bits or 16 bits.
  0 - The host bus width is 8 bits.
  1 - The host bus width is 16 bits.
  Default is 0, 8 bits bus width.
- **BSOR** (bit 6) - Order of bytes on the host bus.
  This bit defines the byte order of the data on the host bus, when the active width of the host bus is 16 bits. It defines which byte of the host data bus contains the earlier byte of the bitstream, the lower-numbered byte of the set-up parameters or microcode, or the m.s. byte of an on-line command. When the active width is 8 bits, the data are always on bits 7:0 and BSOR must be 0.
  0 -"Motorola" style. Bits 15:8 of the host bus contain the earlier byte, lower-numbered byte or m.s. byte.
  1 - "Intel" style. Bits 7:0 of the host bus contain the earlier byte, lower-numbered byte or m.s. byte.
  Default is 0. When BSWD is 0 (8-bit bus width), BSOR is not applicable and must be 0.
- **BSTM** (bit 5) - bitstream transfer mode.
  BSTM specifies whether the MPEG-1 bitstream is transferred using programmed I/O or DMA. Microcode, set-up parameters, on-line commands, status and user data always use programmed I/O.
  0 - programmed I/O.
  1 - DMA.
  Default is 0, programmed I/O.
- **BSLN** (bits 4:0) - burst length.
  This is part of the mechanism that regulates the MPEG bitstream data transfer over the host bus interface. The same mechanism is used also during loading of the set-up parameters.
  In programmed I/O transfer and set-up parameter loading, this bit field specifies the maximum number of write cycles that the host can perform after checking READY, before it must again check READY.
  In DMA transfer mode, this field specifies the maximum number of DMA write cycles for which the DREQ signal will remain active before being de-activated.
  For 8-bit host bus width, the allowed range for BSLN is 2 to 30, even numbers only. For 16-bit host bus width, the allowed range for BSLN is 1 to 15.
  Default value is 16.

BUSOFF

This parameter is used to regulate the utilization of the host bus in DMA transfer mode. It is an unsigned integer which, when multiplied by 16, defines the minimum time, in PCLK periods, for which the ZR36110 will refrain from requesting the host bus, that is, not activate DREQ, after deactivating DREQ. Minimum value is 1 (16 PCLK periods). Must be zero in programmed I/O transfer mode.

SYSMODE

This byte configures the decoding system. It contains the following sub-fields.

- **CODE** (bit 7) - Coded bitstream selection.
  This bit defines the nature of the coded bitstream.
  0 - For a system-multiplexed bitstream.
  1 - For a non-system-multiplexed bitstream.
- **VIDS** (bit 6) - Video frame rate selection.
  This bit, used for frame rate conversion, defines the video output frame rate as 29.97 fps (NTSC) or 25 fps (PAL).
  0 - The frame rate is 29.97 (NTSC).
  1 - The frame rate is 25 (PAL).
  This parameter must be fixed.
- **VIDB** (bit 5) - Video interface mode.
  This bit configures the video interface for the special Enabled mode, described in the *Video Interface* section.
  0 - Normal video interface mode.
  1 - Enabled video interface mode.
  This parameter must be fixed.
- **HHRS** (bit 4) - Half high resolution indication.
  This bit determines whether, for high resolution sequences, the half high resolution format is selected.
  0 - If needed (due to DRAM size limitations).
  1 - Unconditionally.
- **NBANK** (bit 3) - Number of memory banks.
  This bit specifies that one DRAM bank (4 Mbits) or two DRAM banks (8 Mbits) are in use.
  0 - One DRAM bank.
  1 - Two DRAM banks.
- **XCODE** (bit 2) - CODE bit subselections.
  When the CODE bit is high, this bit specifies whether the coded bitstream is an MPEG-1 video only bitstream (according to 11172-2), or a serial port-only bitstream (e.g., an MPEG-1 audio only bitstream, according to 11172-3). When the CODE bit is low, this bit specifies whether the bitstream is a regular, MPEG system-multiplexed bitstream, or a bitstream of Video-CD (white book) sectors, including sector headers and trailers.
  0 - Video only bitstream (CODE bit high), or a system-multiplexed bitstream (CODE bit low).
  1 - Serial port-only bitstream (CODE bit high), or a Video-CD sectors bitstream (CODE bit low).

- **VIDENT** (bit 1) - Video start-up point for random access selection.

  This bit defines the nature of the video start-up point for random access (a sequence header or an I-picture header).

  0 - Video start-up point is an I-picture header, GOP header or sequence header, whichever is encountered first.

  1 - Video start-up point is a sequence header.

- **LPIC** (bit 0) - Display after sequence end.

  This bit defines what is displayed on the video output bus after the ZR36110 decodes a sequence_end_code in the bitstream, and the last decoded picture (in display order) of the sequence has been displayed.

  0 - The background color is displayed after the last picture.

  1 - The last decoded picture (in display order) is displayed indefinitely.

VIDMODE

This byte configures the video post-processor and output interface. See Table 6 and 7 in the *Video Interface* section for the allowed combinations of VIDMODE's sub-fields.

- **VSIZ** (bit 7) - Video output size and scan mode selection.

  This bit defines the video output (display) scan mode and size option: either interlaced CCIR-size, or progressive SIF-size.

  0 - Video output is interlaced CCIR-size (mandatory for high-resolution still images).

  1 - Video output is progressive SIF-size.

  This parameter must be fixed.

  If the enabled video interface mode is used, VSIZ must be 1.

- **VINT** (bit 6) -Video horizontal interpolation.

  This bit defines whether the horizontal re-registration of the U and V samples from the native MPEG SIF picture format, and the horizontal size doubling of the Y, U, and V components, are done by replication or by linear interpolation.

  0 - Interpolation.

  1 - Replication.

- **VCLR** (bit 5) - Video output color space selection.

  This bit defines the color space of the video output: either YUV or RGB.

  0 - Video output color space is YUV.

  1 - Video output color space is RGB.

- **VIWD** (bits 4,3) - Video output color depth.

  For RGB color space, these bits define the color depth (in bits) of the video output.

  00 - RGB width is 24 bits.

  01 - RGB width is 16 bits (5,6,5).

  10 - RGB width is 15 bits (5,5,5).

  11 - Reserved.

  When the output color space is YUV, VIWD must be 00.

- **VSMP** (bit 2) - Video output component sub-sampling structure.

  This bit specifies 4:1:1 or 4:2:2 video output sub-sampling for interlaced CCIR-size video output, when YUV color space is selected.

  0 -YUV format is 4:2:2.

  1 -YUV format is 4:1:1.

  This parameter must be fixed.

  If the video output mode is not interlaced CCIR-size, or if the output color space is RGB, VSMP must be 0.

- **VBUV** (bit 1) - Video output with biased U and V.

  This bit defines whether the U and V video outputs for YUV color space are un-biased (i.e. in the range 0 to 255) or biased (i.e. in the range -128 to 127). The values for the biased case are the values of the unbiased case with 128 subtracted.

  0 - U and V are un-biased.

  1 - U and V are biased.

  If the output color space is RGB, VBUV must be 0.

- **VBLN** (bit 0) - Composite blanking output signal.

  This bit defines whether the FI_EN signal, when output and when HRS=0 (HRS is defined below), is a field index indicator or a composite blanking signal.

  0 - FI_EN is field index.

  1 - FI_EN is composite blanking.

  If the sync signals are defined to be inputs, or when HRS=1, or if the Enabled video interface mode is used, VBLN must be 0.

SYNMODE

This byte configures the video synchronization signals. It contains the following sub-fields. *Note*: Bits 1 to 6 must be set properly even when the SYNC signals are input.

- **SDIR** (bit 7) - Video sync signals direction.

  This bit determines whether the video sync signals (VSYNC, HSYNC, FI_EN) are input or output (i.e., generated by the ZR36110).

  0 - Sync signals are input.

  1 - Sync signals are output.

  When the Enabled video interface mode is used (VIDB = 1), SDIR must be 1. In this mode, VSYNC and HSYNC are outputs, and FI_EN is an input even though SDIR = 1.

  Default is 0 (the sync signals are input).

- **HSHL** (bit 6) - HSYNC signal level.

  This bit defines whether the HSYNC signal is active high or active low.

  0 - HSYNC is active low.

  1 - HSYNC is active high.

  This parameter must be fixed.

- **VSHL** (bit 5) - VSYNC signal level.

  This bit defines whether the VSYNC signal is active high or active low.

  0 - VSYNC is active low.

  1 - VSYNC is active high.

  This parameter must be fixed.

- **FIHL** (bit 4) - FI_EN signal level.

  This bit defines whether the FI_EN, when used as a field index signal, is high or low during field I. During field II the level is the complement of the level during field I.

  0 - FI_EN is low during field I.

  1 - FI_EN is high during field I.

  This parameter must be fixed. If VIDB=1, VBLN=1 or HRS=1, FIHL must be 0.

- **HSLN** (bit 3) - HSYNC signal length selection.

  This bit defines the length of the HSYNC signal: Either short (Sync) or long (Blanking). The length of HSYNC is HSW pixels when short, or NBP+NBPF pixels when long (HSW, NBP and NBPF are defined below).

  0 - HSYNC is short (Sync pulse).

  1 - HSYNC is long (Blanking pulse).

  This parameter must be fixed.

  If the Enabled video interface mode is used, HSLN must be 1.

- **VSLN** (bit 2) - VSYNC signal length.

  This bit defines the length of the VSYNC signal: Either short (Sync) or long (Blanking). The length of VSYNC is VSW*NTP pixels when short, or (NBL+NBLF)*NTP+NBP+NBPF pixels when long (VSW, NTP, NBL, NBLF, NBP and NBPF are defined below).

  0 - VSYNC is short (Sync pulse).

  1 - VSYNC is long (Blanking pulse).

  This parameter must be fixed.

  If the Enabled video interface mode is used, VSLN must be 1.

- **VFAC** (bit 1) - First (top) field active video output.

  This bit defines whether (for interlaced CCIR-size output) the first field (or the top field, for high-resolution still images) of an active video frame is output during field I or field II. *Note*: If the NBL set-up parameter (see below) specifies an integer number of lines (as required for NTSC), the first (top) field should be output during field I. If the NBL set-up parameter specifies a non-integer number of lines (as required for PAL), the first (top) field should be output during field II.

  0 - First (top) field is output during field I.

  1 - First (top) field is output during field II.

  This parameter must be fixed.

  If the video output mode is not interlaced CCIR-size, VFAC must be 0.

- **VCRS** (bit 0) - Video clock pin selection.

  This bit defines whether, for progressive SIF-size output, VCLK or QCLK_V (1/4 the frequency of VCLK) is used as the pixel clock. See the *Video Interface* section.

  0 - VCLK is the pixel clock.

  1 - QCLK_V is the pixel clock.

  This parameter must be fixed.

  If the video output mode is interlaced CCIR-size, VCRS must be 0. If the Enabled video interface mode is used, VCRS must be 1.

EXTMODE

This byte is an extension of the other mode bytes which set up the system, video output, and video synchronization.

- Reserved (bits 7 - 2) - Must be 0.

  1 - FI_EN has other functions.

- **MPA** (bit 1) - MPEG-1 coded audio bitstream indication.

  This bit defines (when the CODE and XCODE bits of the SYSMODE parameter are both 1) whether the serial port-only bitstream input is an MPEG-1 coded audio stream or not.

  0 - The serial port-only bitstream is not an MPEG-1 coded audio stream.

  1 - The serial port-only bitstream is an MPEG-1 coded audio stream.

- **HRS** (bit 0) - High resolution indication.

  This bit determines whether the FI_EN signal (when output) indicates that the video output was derived from high resolution pictures, or has other functions (field indication, composite blank, or video output enable).

  0 - FI_EN indicates high or normal resolution.

  1 - FI_EN has other functions.

SPOMODE

The SPOMODE byte sets the serial port modes.

- **S2FT** (bit 7) - SP2FRM signal type.

  This bit, along with the S2FS bit, defines whether the SP2FRM signal type is pulse, transition, or window. The signal types are specified in the *Serial Ports Interface* section.

  0 - SP2FRM signal is pulse type.

  1 - SP2FRM signal is transition or window type.

  This parameter must be fixed.

  If serial port 2 is not active (S2AC=0), S2FT must be 0.

- **S2CD** (bit 6) - SP2CLK signal direction.

  This bit defines whether the SP2CLK clock signal is an input or an output.

  0 - SP2CLK clock signal is an input.

  1 - SP2CLK clock signal is an output.

  Default is 0, input clock.

  If serial port 2 is not active (S2AC=0), S2CD must be 0.

- **S2FS** (bit 5) - SP2FRM signal type sub-selection.
  This bit determines whether the SP2FRM signal type is transition or window.
  0 - SP2FRM signal type is transition.
  1 - SP2FRM signal type is window.
  This parameter must be fixed.
  If the serial port 2 signal is pulse type (S2FT=0), S2FS must be 0.
- **S2AC** (bit 4) - Serial port 2 active.
  This bit determines whether there is active data output from serial port 2.
  0 - No active data output (serial port pins are floating).
  1 - Active data output (the stream I.D. is defined by the SP2SID set-up parameter).
- **S1FT** (bit 3) - SP1FRM signal type.
  This bit, together with the S1FS bit, define whether the SP1FRM signal type is pulse, transition, or window.
  0 - SP1FRM signal is pulse.
  1 - SP1FRM signal is transition or window.
  This parameter must be fixed.
  If serial port 1 is not active (S1AC=0), S1FT must be 0.
- **S1CD** (bit 2) - SP1CLK signal direction.
  This bit determines whether the SP1CLK signal is input or output.
  0 - SP1CLK signal is input.
  1 - SP1CLK signal is output.
  Default is 0 (input).
  If serial port 1 is not active (S1AC=0), S1CD must be 0.
- **S1FS** (bit 1) - SP1FRM signal type sub-selection.
  This bit determines whether the SP1FRM signal is transition or window.
  0 - SP1FRM signal is transition.
  1 - SP1FRM signal is window.
  This parameter must be fixed.
  If the serial port 1 signal is pulse type (S1FT=0), S1FS must be 0.
- **S1AC** (bit 0) - Serial port 1 active.
  This bit determines whether there is active data output from serial port 1.
  0 - No active data output (serial port pins are floating).
  1 - Active data output (stream I.D. defined by the SP1SID set-up parameter).

Display Control Parameters

The first four display parameters define the "active region" of the decoded picture, the portion of the picture that is actually displayed. Refer to Figure 4 and Table 14 in the *Video Interface* section.

NAP

Defines the width in pixels of the active region of the decoded picture. These 2 bytes are treated as a 16-bit unsigned integer.

NAL

Defines the height in lines of the active region of the decoded picture. These 2 bytes are treated as a 16-bit unsigned integer.

NOP

Defines the offset in pixels of the active region from the left side of the decoded picture. These 2 bytes are treated as a 16-bit unsigned integer.

NOL

Defines the offset in lines of the active region from the top of the decoded picture. These 2 bytes are treated as a 16-bit unsigned integer.

Note: For high resolution pictures, these parameters should be set to half the actual value.

The following eight parameters specify the positioning of the active and background video in the display, relative to the raster defined by the sync signals. These parameters have different interpretations for the two display sizes and formats: interlaced CCIR-size or progressive SIF-size, as illustrated in Figures 12 and 13. For the restrictions on the values of these parameters, see Tables 15, 16, and 17 in the *Video Interface* section.

Note: Unless otherwise indicated, the values of these parameters must be set properly even when the sync signals are input.

NTP

Defines the number of pixels per displayed line, (i.e. the number of VCLK or QCLK_V periods, depending on the video output format; see the discussion of the pixel clock in the *Video Interface* section) between the leading edges of two consecutive HSYNC pulses. These 2 bytes are treated as a 16-bit unsigned integer.
This parameter must be fixed.

NTL

Defines the number of lines per frame, i.e. the number of HSYNC activations between the leading edges of consecutive VSYNC pulses (for progressive SIF-size output) or alternate VSYNC pulses (for interlaced CCIR-size output). These 2 bytes are treated as a 16-bit unsigned integer.
This parameter must be fixed.

NBP

Specifies the blanking region (number of blank pixels) at the beginning of each line.These 2 bytes are treated as a16-bit unsigned integer. Not applicable for long input HSYNC, and must be set to 0 in this case. For long input HSYNC, the blanking region at the beginning of each line ends with the deactivation of HSYNC. Also, for long output HSYNC, NBP+NBPF specifies the width of the HSYNC pulse.
This parameter must be fixed.

NBL

Specifies the blanking region (number of blank lines) at the beginning of each field or frame. These 2 bytes are treated as a 16-bit unsigned fraction, with 15 integer bits and 1 bit

after the binary point. Not applicable for long input VSYNC, and must be set to 0 in this case. For long input VSYNC, the blanking region at the beginning of each field ends with the deactivation of VSYNC. Also, for long output VSYNC, NBL+NBLF lines plus NBP+NBPF pixels specifies the width of the VSYNC pulse.

This parameter must be fixed.

NBPF

Specifies the blanking region (number of blank pixels) at the end of each line. These 2 bytes are treated as a 16-bit unsigned integer. Not applicable for long input HSYNC (and must be set to 0 in this case). Also, for long output HSYNC, NBP+NBPF specifies the width of the HSYNC pulse.

This parameter must be fixed.

NBLF

Specifies the blanking region (number of blank lines) at the end of each field or frame. These 2 bytes are treated as a 16-bit unsigned fraction, with 15 integer bits and 1 bit after the binary point. Not applicable for long input VSYNC (and must be set to 0 in this case). Also, for long output VSYNC, NBL+NBLF lines plus NBP+NBPF pixels specifies the width of the VSYNC pulse.

This parameter must be fixed.

NDP

Defines the number of background pixels on each line prior to (that is, to the left of) the active region. The 2 bytes of NDP are treated as a 16-bit unsigned integer.

NDL

Defines the number of background lines prior to (that is, above) the active region per field or frame. These 2 bytes are treated as a 16-bit unsigned integer.

The next two parameters specify the width of the video sync signals when they are output and short. Otherwise, they must be set to 0. Restrictions on the values of these parameters can be found in Table 16 in the *Video Interface* section. See also Figures 5 and 8.

HSW

Specifies the width of the horizontal sync signal (HSYNC), in pixels, when it is a short output. This byte is treated as an 8-bit unsigned integer.

This parameter must be fixed.

VSW

Specifies the width of the vertical sync signal (VSYNC), in lines, when it is a short output. This byte is treated as an 8-bit unsigned fraction with 7 integer bits and 1 bit after the binary point.

This parameter must be fixed.

The following four parameters define the color space conversion coefficients.

CRV

Defines the value of the V to R color space conversion coefficient. These two bytes are treated as a 16-bit two's complement fraction with 6 integer bits and 10 fractional bits.

Minimum value is 0. Maximum value is (2-1/1024). *Note*: CCIR 601 value is 1.402.

CBU

Defines the value of the U to B color conversion coefficient. These two bytes are treated as a 16-bit two's complement fraction with 6 integer bits and 10 fractional bits.

Minimum value is 0. Maximum value is (2-1/1024). *Note*: CCIR 601 value is 1.772.

CGV

Defines the value of the V to G color conversion coefficient. These two bytes are treated as a 16-bit two's complement fraction with 6 integer bits and 10 fractional bits.

Minimum value is -1. Maximum value is 0. *Note*: CCIR 601 value is -0.714.

CGU

Defines the value of the U to G color conversion coefficient. These two bytes are treated as a 16-bit two's complement fraction with 6 integer bits and 10 fractional bits.

Minimum value is -1. Maximum value is 0. CCIR 601 value is -0.344.

Note: If the output color space is YUV (VCLR=0), the values of the conversion coefficients must be zero.

The next four parameters define background color, and the value of the upper byte of the video bus for 16-, 15-, or 12-bit video output. The background color values are not modified by the color space conversion (parameter VCLR), or the biasing of U and V (VBUV), so they must be specified in the output color space, and with the desired bias if applicable. They are, however, post processed according to the settings of VSMP and VIWD when applicable.

BGRV

The value of the R component of the background color if VCLR = 1, or the value of the V component of the background color, if VCLR =0.

BGGY

The value of the G component of the background color if VCLR = 1, or the value of the Y component of the background color, if VCLR =0.

BGBU

The value of the B component of the background color if VCLR = 1, or the value of the U component of the background color, if VCLR =0.

FIL

The value output on bits [23:16] of the VIDOUT bus when one of the YUV, 15-bit, or 16-bit RGB formats is used.

Timing Parameters

The following parameters define the timing of the serial ports, presentation delays of the video and serial port data, and the frequency of VCLK.

SP1CD, SP2CD

These parameters specify the integer divisors of VLCK, used to specify the frequency of SP1CLK and SP2CLK respectively, when they are outputs.

The resulting serial port clock rates should be equal to or above the bit rates of the streams specified for the serial ports.

These are 2-byte parameters, treated as 16-bit unsigned integers. Minimum value is 4. Maximum value is 1023 (the most significant 6 bits must always be zero). If a serial port is inactive (S1AC=0 or S2AC=0), or the serial port clock is an input (S1CD=0 or S2CD=0), the corresponding divisor value must be 0.

When the output from a serial port is an MPEG-1 coded audio elementary stream, the parameter can be set to zero. In this case, the value of the divisor is calculated internally from the stream data.

SP1BR, SP2BR

These parameters specify the ratios of bit rate to clock rate for serial ports 1 and 2 respectively. The ZR36110 maintains average serial port bit rates as defined by these two parameters, if the clock rates, generated by using SP1CD or SP2CD (or the external clocks), are equal to or higher than the bit rates specified for the serial ports.

These are 3-byte parameters treated as 24-bit unsigned fractions with 5 integer bits and 19 fractional bits. Minimum value is 1/64. Maximum value is 1.0 (the most significant 4 bits must be zero). If a serial port is inactive, the corresponding value of SP1BR or SP2BR must be zero.

These parameters must be chosen so that the actual serial port bit rate is equal (to within the available precision) to the desired bit rate, which is usually equal to the bit rate of the audio stream assigned to the serial port. For example, if ABR is the bit rate of the audio stream assigned to serial port 2, F_{VCLK} is the frequency of VCLK, and the serial port clock is configured to be an output so that its frequency is F_{VCLK} / SP2CD, SP2BR = (ABR * SP2CD) / F_{VCLK}

When the output from a serial port is an MPEG-1 coded audio elementary stream, the parameter can be set to zero. In this case the value of the ratio is calculated internally from the stream data.

SP1DL, SP2DL

These parameters specify the delays in the audio decoders (or other processors) connected to serial port 1 and serial port 2. The delay is defined as the time between the reception of the first bit of the code of a presentation unit and the output of the first sample of this presentation unit to the user. The ZR36110 compensates for this delay when timing the output of the video and the serial port, to maintain synchronization with the video relative to the perception of the user.

These two-byte parameters (treated as 16-bit unsigned integers) measure the delay in units of 90KHz clock. The value of the parameter must be zero when its serial port is inactive.

These parameters must be fixed.

VOD

This parameter specifies the delay in a possible display processor connected to the video output, between reception of the first sample of a presentation unit into that device and the output of the first sample of this presentation unit to the user. The ZR36110 compensates for this delay when timing the output of the video and the serial ports, to maintain synchronization with the video relative to the perception of the user. The value of the parameter must be zero when there is no video output.

This 2-byte parameter (treated as a 16-bit unsigned integer) measures the delay in units of 90 KHz clock.

This parameter must be fixed.

VCLK

This parameter must be set to the nominal frequency of the video input clock (VCLK). VCLK is 3-byte parameter treated as a 24-bit unsigned integer, representing the frequency of the VCLK input signal in units of Hertz.

The VCLK parameter is used in the transformation of the time stamps and delay information from a 90KHz clock to a clock derived from VCLK.

This parameter must be fixed.

Stream Selection Parameters

When playing back an MPEG system bitstream that contains multiple video and/or multiple audio streams, the video stream to be decoded and/or the audio, private1, or private2 streams to be output on a serial port are selected based on the settings of the CODE and XCODE bits of the SYSMODE parameter.

The SP1SID and SP2SID parameters designate the stream I.D. for serial ports 1 and 2, respectively. VIDSID designates the video stream I.D.

SP1SID, SP2SID

- **SP1SID** and **SP2SID** - stream I.D. for serial port 1 and 2, respectively.

  The legal values, in hexadecimal, are shown below. All other values are illegal.

  00 - First audio stream encountered.

  C0 to DF - Audio streams.

  BD - Private1 stream.

  BF - Private2 stream (when CODE is low), or serial port-only stream (when CODE and XCODE are both high).

  FF - No active output.

  If SP1SID and SP2SID are both not equal to FF, they must be different.

VIDSID

- **VIDSID** - Stream I.D. for video.

  The legal values, in hexadecimal, are shown below. All other values are illegal.

  00 - First video stream encountered.

  E0 - Video stream (when CODE is low), or video (only) stream (when CODE is high and XCODE is low).

  E1 to EF - Video streams.

  FF - No active video output.

ON-LINE COMMANDS

Once it has been initialized, by the procedure described in the *Initialization* section, subsequent behavior of the ZR36110 is controlled by the host by means of on-line commands. On-line commands are written into the ZR36110 via an I/O address reserved for this purpose, as described in the *Host Interface* section.

An on-line command always consists of two bytes, and unless otherwise noted, the m.s. byte is zero. Note that when the host interface operates in 16-bit mode (BSWD=1), the byte order of the command must match the setting of the BSOR set-up parameter. Also note that when the host interface operates in 8-bit mode (BSWD=0), the command must be written with no intervening bitstream data transfers between the two bytes of the command. This restriction must be observed in both modes of bitstream transfer, DMA and programmed I/O.

Table 2 lists the supported on-line commands, with the least significant byte of the code for each command. All least significant byte values not listed in the table are reserved, and may be assigned functions in future releases of microcode. The most current assignments are documented in the ZR36110 microcode release notes.

Table 2. On-line commands

Command Name	Least Significant Byte Value
Go	0000 0000
Pause Stream	0001 0000
Decode to First I-Picture and Pause Stream	0010 0000
Single Step	0011 0000
Decode to Next I-Picture and Pause Stream	0100 0000
Slow Motion	0101 0bbb
Freeze Frame	0110 0000
Fast Search	0111 0bbb

Table 2. On-line commands (continued)

Command Name	Least Significant Byte Value
End Decoding	1000 00bb
Continue	1001 0000
Change Stream I.D.	1010 0bbb
Change Brightness	1011 0000
Change Contrast	1100 0000
End Decoding on GOP	1110 0000

Host on-line commands are divided into two groups: mode change commands and parameter change commands. After the Go command, the ZR36110 operates in normal speed playback mode. During normal speed playback mode, the host can command the ZR36110 to switch to some of the special operation modes, using the appropriate host on-line mode change commands.

The ZR36110 has a register which holds one mode change host on-line command. The OCLR bit of STATUS1 indicates whether the mode change host on-line command register is empty (meaning the next on-line command can be sent) or is not empty. If a host on-line command is written to the ZR36110 when the register is not empty, the command currently residing in the register is overwritten.

If the register is empty, the ZR36110 continues to execute in the same mode as before. If the register is not empty, the ZR36110 may change its operating mode based on the current mode, the host on-line command in the register, and the existence of internal on-line commands generated in some of the special modes. Based on the same data, the ZR36110 decides whether or not to remove the host on-line command from the register. Mode change commands which are not authorized in a particular mode are removed from the register, with no effect on ZR36110 operation.

The following is a concise description of the behavior in response to each of the on-line commands. More detailed information can be found in the *Playback Operation* section.

Go

Commands the ZR36110 to start bitstream consumption and playback. The Go command is allowed only when the decoder is idle (as indicated by the IDLE signal or status register bit), and is the only command allowed when the decoder is idle.

Pause Stream

When the ZR36110 executes the Pause Stream on-line command, it pauses video decoding and serial port output, and displays the current picture indefinitely (that is, until another command is executed). If an audio processor is

connected to one of the serial ports, it should stop decoding when its coded bitstream stops and mute its output.

Decode to First I-Picture and Pause Stream

When it executes this command, the ZR36110 continues normal decoding and display until it begins to display an I-picture.Then it pauses as for the Pause Stream command, and displays the I-picture indefinitely.

Single Step

When it executes this command, the ZR36110 steps to the next picture. That is, it resumes decoding, decodes and displays one picture, then pauses, and displays the new picture indefinitely. If an audio processor is connected to one of the serial ports, its output should be muted during the execution of Single Step command.

Decode to Next I-Picture and Pause Stream

When it executes this command, the ZR36110 steps to the next I-picture. That is, it resumes decoding, but without changing the picture being displayed, until display of the next I-Picture is scheduled to begin. Then it pauses, and displays the new I-picture indefinitely.

Freeze Frame

When the ZR36110 executes this command, it freezes the display, i.e., continues to display the same frame. Decoding and serial port output are not affected.

Slow Motion

When the ZR36110 executes this command, it decodes the pictures from the bitstream at a rate that is slowed down from the nominal by an integer factor, given by the "bbb" field of the command word. This is implemented by stepping to the next picture, pausing for bbb-1 frames, stepping again and pausing for bbb-1 frames, and so on indefinitely. If an audio processor is connected to one of the serial ports, its output should be muted during the execution of a Slow Motion command.

Continue

When the ZR36110 executes this command, it resumes normal playback.

Fast Search

When the ZR36110 executes this command, it continues to decode and display the video and begins analyzing the video coded data before it is stored in the DRAM. All non-video packets and some of the picture data (as specified by the on-line command) are discarded. The ZR36110 then stores any pictures not discarded, together with any sequence and GOP headers and sequence_end_code, in DRAM. If an audio processor is connected to one of the serial ports, its output should be muted during the execution of a Fast Search command. Based on the "bbb" bits of the command word, the Fast Search command is executed as follows:

bbb=000, forbidden.

bbb=001, discard some B pictures.

bbb=002, discard all B pictures.

bbb=003, discard all B and P pictures.

bbb=004:007, reserved.

End Decoding

When the ZR36110 executes this command, it terminates decoding, and when the last coded picture has been displayed, activates the IDLE signal and status bit, and goes into the idle state. The content of the display after this is specified by the "bb" bits of the command word:

bb=10, display the last picture (in coded order).

bb=00, display the last picture (in display order).

bb=01, display the background color.

bb=11, display the last picture (in display order) for one frame period, then the background color.

Note that this specification overrides the LPIC bit of the SYSMODE set-up parameter, if the video sequence happened to end at the same time.

End Decoding on GOP

When the ZR36110 executes this command, it terminates decoding as if a video sequence end code has been received after the last picture of the current GOP, and for system-multiplexed bitstreams, it is followed by a 11172_end_code. This command should only be used when there is an active video stream.

Change Stream I.D.

When the ZR36110 executes this command, it stops one of the serial ports or video streams and/or restarts one of these streams after resynchronization. The new video stream I.D., which has the same legal values as the VIDSID set-up parameter, and the new serial port stream I.D., which has the same legal values as the SP1SID (or SP2SID) set-up parameter, are used until the set-up parameters are reloaded or another change is requested by a Change Stream I.D. on-line command. The command word "bbb" bits determine the setting:

bbb=100, restart video playback (with the new video stream I.D. specified in the m.s. byte).

bbb=001 (or 011), stop transfer of serial port 1 (or 2) data to the DRAM and flush the DRAM buffer.

bbb=000 (or 010), reinitialize serial port 1 (or 2) (with the new serial port stream I.D. specified in the m.s. byte).

Change Brightness and Contrast

When the color space of the video output is YUV (i.e., bit VCLR of the VIDMODE set-up parameter is low), these commands can be used to change the video output. The only value affected is Y, where

Y'=int(CON*(Y-128)+BRT)

Y is limited to the range 0 to 255 and output. CON is an 8.6 2's complement fraction stored in the m.s. byte of the Change Contrast command (range: 2-1/64 to 1/64). BRT is an 8 bit unsigned integer stored in the m.s. byte of the Change Brightness command. The new brightness and contrast parameters are used until the set-up parameters are loaded or another change is requested by a Change Brightness or Change Contrast on-line command. CON and

BRT are reset internally to 1.0 and 128, respectively, when the set-up parameters are loaded.

Synchronization of video and serial port outputs

When the Go on-line command is executed, the ZR36110 goes through a phase of decoding start-up, and, if a system bitstream is being decoded and a serial port is active, synchronization of the serial output stream with the video display. The mechanism of start-up and synchronization is described in detail in the *Playback Operation* section. Here it is sufficient to note that once synchronization is established, it is maintained automatically.

Whenever decoding is suspended during execution of an on-line command, serial port output is also suspended. And when normal decoding resumes, whether indefinitely as after a Continue command, or transiently as in the Single Step, Slow Motion and Decode to Next I-Picture commands, serial port output also resumes. Thus, synchronization is maintained during execution of all on-line commands.

Mode Change On-Line Command Order

There are restrictions on the allowed order of mode change on-line commands. Table 3 shows which commands are allowed to succeed each command (an "X" indicates a legal succession). The table can also be used to determine which commands are allowed to precede any given command.

Random Access

After a Go command, the ZR36110 is capable of starting up and synchronizing when the bitstream is fed to it starting either at the beginning of the stream, as defined in the ISO-11172 standard, or at any randomly chosen byte-aligned entry point. Also, when the ZR36110 goes idle after an End Decoding command, all remaining data in the video and serial port stream buffers is flushed. This can be used to implement a random access or seek function in the host software driver, by terminating decoding with an End Decoding command, and then when the device is idle, restarting it with a Go command, feeding the bitstream from the desired entry point.

Table 3. Mode Change On-Line Command Order

	Succeeding Command									
	Go[1]	**Pause**	**End Decoding[2]**	**Freeze**	**Continue**	**Single Step**	**Slow Motion**	**Decode to First I-Picture**	**Decode to Next I-Picture**	**Fast Search**
Preceding Command										
Go		X	X	X				X		X
Pause			X	X	X	X	X			
End Decoding	X									
Freeze		X	X		X					
Continue		X	X	X				X		X
Single Step			X	X	X	X	X			
Slow Motion			X	X	X	X	X			
Decode to First I-Picture			X	X	X	X	X		X	
Decode to Next I-Picture			X	X	X	X	X		X	
Fast Search			X							

[1] A Go command is allowed only when the ZR36110 is idle, as indicated by the IDLE signal and status register bit.
[2] Including End Decoding on GOP.

HOST INTERFACE

The host interface is used for the following functions:

- Microcode load
- Set-up parameters load
- On-line commands
- MPEG bitstream transfer
- Status readout
- User data readout

Two mechanisms are available for the bitstream transfer, programmed I/O and DMA. Microcode load, set-up parameters load and on-line commands use programmed I/O writes. Status is read from the ZR36110 back to the host using programmed I/O read. The I/O and DMA cycles are compatible with the ISA bus, but can operate at a much faster rate.

Host Interface Signals

The host interface comprises a 16-bit data bus (BUSDAT), a two-bit address bus (BUSADD), and 6 control signals: $\overline{\text{BUSRD}}$, $\overline{\text{BUSWR}}$, $\overline{\text{BUSCS}}$, DREQ and $\overline{\text{DACK}}$. The host interface operates asynchronously with the clocks of the ZR36110.

Host Interface Configuration

Table 4 shows the six legal combinations of the three sub-fields of the BUSMODE parameter used to configure the host bus interface. The default configuration after a cold reset is 8 bit, programmed I/O transfer. Note that all host interface write transactions (microcode load, set-up parameters load and on-line commands, as well as bitstream transfer) are affected by BSWD and BSOR.

In the 16 bit modes, the order of the bytes can be either "Motorola" or "Intel" style, which in effect determines which byte of the host data bus carries the earlier byte in the bitstream, the lower-numbered byte of the microcode or set-up parameters, or the most significant byte of an on-line command. For Motorola style, bits 15:8 of the host bus contain this byte. For Intel style, bits 7:0 of the host bus contain this byte. In the 8 bit modes, only bits (7:0) of the host bus are used; note that in this mode, the most significant byte of an on-line command precedes the least significant byte. Status is always read on bits (7:0).

I/O Write

The host performs programmed I/O writes by activating the $\overline{\text{BUSCS}}$ signal, and specifying the destination of the data with BUSADD (1:0). The falling edge of the $\overline{\text{BUSWR}}$ signal latches $\overline{\text{BUSCS}}$ and BUSADD. Data is then strobed into the ZR36110 using the rising edge of the $\overline{\text{BUSWR}}$ signal. See the "I/O Write Timing" diagram in the *AC Characteristics* section.

The two BUSADD bits define four write ports, which have different purposes during the initialization phase (when the ZR36110 is idle, that is, after a cold reset, or after decoding of a sequence has ended and IDLE is active) and the playback phase (between the Go on-line command and activation of IDLE). This is shown in Table 5.

Loading of microcode and set-up parameters is described in the *Initialization* section of this document.

When transferring the MPEG bitstream using programmed I/O (in I/O-only mode), the ZR36110 and the host employ a handshaking mechanism which regulates the rate that data is loaded in to the ZR36110. This handshaking mechanism uses the READY status bit (or the equivalent READY signal), and the 5-bit BSLN field of the BUSMODE set-up parameter. When the READY status bit (or the READY signal) is active (high), this indicates that the ZR36110 is ready to accept a burst of data. BSLN defines the maximum burst length, that is, the number of write cycles the host can perform after detecting READY active, before checking READY again. The READY signal and the READY bit of the STATUS1 register are updated only 100 nanoseconds after deactivation of the $\overline{\text{BUSWR}}$ which generated the update.

Note: $\overline{\text{DACK}}$ must not be active when $\overline{\text{BUSCS}}$ is active.

Note: After finishing the transfer of a system bitstream in 8-bit modes, the host must transfer one more byte of any value, unless it can be assured that the length of the bitstream was an even number of bytes.

Table 4. Host Interface

BSWD	BSOR	BSTM	Host Interface Configuration
0	0	0	8 bit, programmed I/O bitstream transfer[1]
0	0	1	8 bit, DMA bitstream transfer
1	0	0	16 bit, Motorola style, programmed I/O bitstream transfer
1	0	1	16 bit, Motorola style, DMA bitstream transfer
1	1	0	16 bit, Intel style, programmed I/O bitstream transfer
1	1	1	16 bit, Intel style, DMA bitstream transfer

[1] *Default mode after cold reset.*

Table 5. Write ports defined by BUSADD

Phase of Operation	BUSADD(1:0)	Destination of Port Data
Initialization Phase	00	set-up parameters
	01	first part of microcode
	10	Go on-line command
	11	second and third parts of microcode
Playback Phase	00	MPEG bitstream in I/O-only mode, not used in mixed mode
	01	not used
	10	on-line commands
	11	not used

DMA Transfers

In DMA mode, the ZR36110 requests the bitstream by activating DREQ continuously for at most BSLN DMA write cycles. The host responds to DREQ by activating $\overline{\text{DACK}}$ and writing the data using the rising edge of $\overline{\text{BUSWR}}$. A single DMA cycle is illustrated in the "DMA Timing" diagram in the AC Characteristics section of this document. $\overline{\text{DACK}}$ is sampled by the ZR36110 only on the falling edge of $\overline{\text{BUSWR}}$, and a write cycle is completed on the rising edge of $\overline{\text{BUSWR}}$ without regard to $\overline{\text{DACK}}$, so $\overline{\text{DACK}}$ may remain active or pulsed between bus cycles as desired. The BUSOFF parameter ensures that the ZR36110 does not monopolize the host bus in DMA transfer mode, by forcing it to refrain from re-activating DREQ for at least the specified amount of time after each de-activation of DREQ.

Note: DREQ may remain active after the last byte of a normally ending bitstream (the last byte of an iso_11172_ end_code or a sequence_end_code) has been transferred. This can happen if the last burst of data was shorter than BSLN. The work around for this is for the DMA controller to continue to supply data, of any value, until the ZR36110 deactivates DREQ.

Status Read (I/O Read)

To read the STATUS registers, the host selects the ZR36110 by activating $\overline{\text{BUSCS}}$ and specifying the status register to be read by BUSADD (1:0). The falling edge of $\overline{\text{BUSRD}}$ latches $\overline{\text{BUSCS}}$ and BUSADD and then the host reads the status using the rising edge of $\overline{\text{BUSRD}}$.

There are three eight-bit status registers, STATUS0, STATUS1, and STATUS2. Each register is connected to BUSDAT (7:0) during I/O read when its address is selected. The status registers are assigned to the following addresses:

STATUS0 - 00.
STATUS1 - 01.
STATUS2 - 10.

STATUS0

- Reserved (bit 7) - Return zero.
- **DEVI** (bits 6, 5) - Device identification.
  The values of these bits are fixed.
  00 - ZR36100.
  01 - ZR36110, step A.
  10 - Reserved.
  11 - Reserved.
- Reserved (bit 4) - Return zero.
- **C-STATE** (bits 3 - 0) - Internal state.
  These bits define the internal state of the video decoder. A change of state is caused by an end of bitstream indication or a mode change on-line command.
  0000 - Init state - After reset, during set-up parameter loading, or during playback of serial port (only) bitstreams.
  0001 - Idle state - After set-up parameter loading or upon completion of playback.
  0010 - Normal speed playback state.
  0011 - Pause state.
  0100 - Single step state.
  0101 - Reserved.
  0110 - Decode to first I state.
  0111 - Decode to next I state - During decode to next I-picture or Freeze Frame playback.
  1000 - End state - After decoding a video sequence end code or receiving an End Decoding on-line command (before playback is complete).
  Note: Slow motion is implemented as a series of single steps.

STATUS1

- **OLCR** (bit 7) - Mode change (excluding Go and Fast Search) host on-line command register status.
  This bit determines whether the host on-line command register is full (i.e., holding an on-line command which has not been executed) or empty.
  0 - On-line command register is empty.
  1 - On-line command register is full.
- **STRP** (bit 6) - Code buffer "starving" Pause.
  This bit indicates when the ZR36110 is paused (video only or audio and video pausing), due to code buffer starving (see Playback Operation).
  0 - Regular operation.
  1 - Paused due to code buffer starving.
- **PTYP** (bits 5, 4) - Decoded picture type.
  These bits define the type of picture currently being decoded. If the display is interlaced, it is set to one of the four values below upon activation of the VSYNC signal (after decoding of the first block of that picture begins) and is reset upon the next activation of the VSYNC signal. For progressive display, PTYP is set to one of the four values shown below upon each activation of the VSYNC signal.

00 - No picture currently being decoded.

01 - Picture currently being decoded is an I-picture.

10 - Picture currently being decoded is a P-picture.

11 - Picture currently being decoded is a B-picture.

- **READY** (bit 3) - Copies the READY signal.

  This bit determines whether the ZR36110 is ready to receive more input when in I/O mode.

  0 - Ready to receive input.

  1 - Not ready to receive input.

- **IDLE** (bit 2) - Copies the IDLE signal.

  This bit determines whether the ZR36110 is idle or in playback.

  0 - Playback.

  1 - Idle.

  Default is high (idle).

- **DRBF** (bit 1) - DRAM code buffer full indication.

  This bit is set by the ZR36110 when at least one of the code buffers in the DRAM becomes full. It is reset when the host reads the STATUS1 register.

  0 - DRAM code buffers not full.

  1 - At least one DRAM code buffer has become full since the last time the STATUS1 register was read by the host.

- **TRGR** (bit 0) - Video-CD trigger bit value.

  This bit is set when the value of the trigger bit (in the header of the current sector being played) is set. A sector is considered played back when the first video picture header after that sector header is decoded. It is reset when the host reads the STATUS1 register.

  0 - No trigger bits in played back sectors since the last time STATUS1 was read by the host.

  1 - Trigger bit appeared in a played back sector since the last time STATUS1 was read by the host.

STATUS2

- **USRNEW** (bit 7) - New user data.

  This bit indicates that new user data is stored in the internal buffer. USRNEW is set after the user data of a picture header is written to the user data buffer. If there is no data in a picture header, USRNEW is not set for that picture. It is reset the first time the buffer is read or when the picture start code is decoded.

  0 - No new user data in the buffer.

  1 - New user data in the buffer.

- **USRVAL** (bit 6) - Invalid user data.

  This bit indicates whether user data read from the internal buffer is valid or invalid. USRVAL is set when an attempt is made to simultaneously read and write the user data buffer (data written to the user data buffer is valid - only the data being read is invalid). USRVAL is reset when the host reads the STATUS2 register.

  0 - User data read from the internal buffer is valid.

  1 - User data read from the internal buffer is invalid.

- **GPFL** [3:0] (bits 5 - 2) - Communication flags.

  These bits function as four general purpose flags used for communication between the host and the microcode. The microcode sets and resets the GPFL bits. GPFL functions are defined in the latest version of the microcode.

- **HRSI** (bit 1) - High resolution still image display.

  This bit is set when the picture size parameters in the decoded sequence header indicate a high resolution sequence. HRSI is reset when the picture size parameters in the decoded sequence header indicate a normal resolution sequence. In system-multiplexed bitstreams, all video sequences should have the same picture size parameters.

  0 - Decoded video sequence is normal resolution.

  1 - Decoded video sequence is high resolution still image.

- **LDPF** (bit 0) - Microcode loading failure.

  This bit indicates that microcode loading to address 01 or 11 has succeeded or failed.

  0 - Microcode loading failed.

  1 - Microcode loading succeeded.

  Default is high (after failure, LPDF is not set again until a cold RESET is performed).

User Data

The ZR36110 stores the first 64 bytes from the user data area of the picture header in an internal buffer. The USRNEW and USRVAL status bits in the STATUS2 register should be used by the host to make sure all 64 bytes of information read from the internal buffer are valid and come from the same picture header. The host should examine the STATUS2 register upon each VSYNC activation and should read all the data in the buffer within 10 mSec. After reading the data, the host reads the USRVAL status bit, to make sure the data just read was valid. If the data is not valid, the host should try again after the next VSYNC activation. Reading of the user data by the host is similar to reading the status registers. The assigned address is -11.

VIDEO INTERFACE

The video interface consists of a 24 bit output data bus (VIDOUT), three bidirectional video synchronization signals (HSYNC, VSYNC and FI_EN) and two clock signals: one input (VCLK), and one output (QCLK_V).

Video Interface Configurations

In both the interlaced CCIR-size and progressive SIF-size configurations, the video interface operates as a conventional digital video source, with HSYNC and VSYNC defining the raster, the VIDOUT bus being driven continuously by the ZR36110, and the data being provided at a constant pixel clock rate along each line.

The video interface can also be configured to operate in a special Enabled video output mode, in which the ZR36110 drives the bus and provides the data in bursts, whose timing is controlled from the outside. This allows the VIDOUT bus to be shared. The Enabled mode is described in detail later in this section.

The parameter settings for each of the configurations are summarized in Table 6. The color space, bus width, and sub-sampling can be any of those shown in Table 7. The interlaced CCIR-size configuration of the video interface must also be used when decoding a high-resolution still image sequence (see the *High-Resolution Still Images* section)..

Table 6. Legal set-up parameters for video interface configurations

Configu -ration	VSIZ[6]	VIDB[4]	VINT[6]	VCLR[6]	VIWD[6]	VSMP[6]	VBUV[6]	VCRS[7]	SDIR[7]	HSLN[7]	VSLN[7]	HRS[8]	VBLN[6]	VFAC[7]
Interlaced CCIR-size	0	0	0/1	Any of formats 1, 2, 3, 4, 5 in Table 7				0	0	Input syncs[1]		0	0[3]	0/1
									1	Output syncs[2]		0/1[9]	0/1[9]	
Progressive SIF-size	1	0	0/1	Any of formats 1, 3, 4, 5 in Table 7				0/1	0	Input syncs[1]		0	0[9]	0
									1	Output syncs[2]		0	0/1	
Enabled	1	1	0	0	0	0	0/1	1	1	1	1	0	0[5]	0

[1] Any combination of [HSLN, VSLN] except [0,1].

[2] Any combination of [HSLN, VSLN].

[3] When the syncs are inputs in interlaced CCIR-size, the field index FI_EN is also required.

[4] Parameter field is located in SYSMODE set-up parameter

[5] FI_EN is an input which enables the video output.

[6] Parameter field is located in VIDMODE set-up parameter.

[7] Parameter field is located in SYNMODE set-up parameter.

[8] Parameter field is located in EXMODE set-up parameter.

[9] Any combination of [HRS, VBLN] except [1,1].

Video Data Bus Format Options

Prior to being output on the VIDOUT bus, the active region of the decoded picture is translated from the native MPEG-1 format into one of the color space, component sub-sampling, and color depth formats shown in Table 7. The table summarizes the legal set-up parameter combinations for each video data format. For YUV color spaces, the VBUV set-up parameter determines whether the U and V components will be output in a biased or unbiased format. For RGB color spaces, the conversion between YUV and RGB is performed using the coefficients in the CRV, CBU, CGV, and CGU set-up parameters. The conversion formulas are as follows, where U and V are in the unbiased representation:

R = Y + CRV*(V-128)
B = Y + CBU*(U-128)
G = Y + CGV*(V-128) + CGU*(U-128)

Table 7. Video data formats

Video Data Format	VCLR	VIWD	VSMP	VBUV	Description		
					Color Space	Component Sub-Sampling	Color Depth (bits)
1	0	00	0	0/1	YUV	4:2:2 (2:1:1)	16
2	0	00	1	0/1	YUV	4:1:1	12
3	1	00	0	0	RGB	4:4:4 (2:2:2)	24
4	1	01	0	0	RGB	4:4:4 (2:2:2)	16 (5,6,5)
5	1	10	0	0	RGB	4:4:4 (2:2:2)	15 (5,5,5)

Note: 5,5,5 and 5,6,5 RBG are obtained by truncation of 8,8,8 (24-bit) RGB.
Note: Format 2 is supported only in the interlaced CCIR-size configuration. In the Enabled configuration, only format 1 is supported.

The sample arrangements on the video data bus for the five video data formats are given in the following tables. The most significant bit of each color component is aligned with the m.s. byte of the VIDOUT sub-field on which it is output. A special case is the bit alignment for the UV color components in video format 2; this is shown in Table 9.

Table 8. Video format 1: YUV 4:2:2 (or 2:1:1)

VIDOUT bus	Pixel time slot							
	0	1	2	3	4	5	6	7
bits 23:16	FIL[1]							
bits 15:8	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
bits 7:0	U0	V0	U2	V2	U4	V4	U6	V6

[1] The value in the FIL set-up parameter is output on bits 23:16.

Table 9. Video format 2: YUV 4:1:1

VIDOUT bus	Pixel time slot							
	0	1	2	3	4	5	6	7
bits 23:16	FIL							
bits 15:8	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
bit 7	U0,7	U0,5	U0,3	U0,1	U4,7	U4,5	V4,3	V4,1
bit 6	U0,6	U0,4	U0,2	U0,0	U4,6	U4,4	V4,2	V4,0
bit 5	V0,7	V0,5	V0,3	V0,1	V4,7	V4,5	V4,3	V4,1
bit 4	V0,6	V0,4	V0,2	V0,0	V4,6	V4,4	V4,2	V4,0
bits 3:0	Zero							

Note: V0,7 indicates bit 7 of V component; sample 0.

Table 10. Video format 3: 24 bit RGB

	Pixel time slot							
VIDOUT bus.	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
bits 23:16	R0	R1	R2	R3	R4	R5	R6	R7
bits 15:8	G0	G1	G2	G3	G4	G5	G6	G7
bits 7:0	B0	B1	B2	B3	B4	B5	B6	B7

Table 11. Video format 4: 16 bit RGB

	Pixel time slot							
VIDOUT bus	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
bits 23:16	FIL							
bits 15:11	R0	R1	R2	R3	R4	R5	R6	R7
bits 10:5	G0	G1	G2	G3	G4	G5	G6	G7
bits 4:0	B0	B1	B2	B3	B4	B5	B6	B7

Table 12. Video format 5: 15 bit RGB

	Pixel time slot							
VIDOUT bus	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
bits 23:16	FIL							
bit 15	Zero							
bits 14:10	R0	R1	R2	R3	R4	R5	R6	R7
bits 9:5	G0	G1	G2	G3	G4	G5	G6	G7
bits 4:0	B0	B1	B2	B3	B4	B5	B6	B7

Video Clocks (VCLK, QCLK_V)

In the interlaced CCIR-size interface configuration, VCLK is the pixel clock, and the video data bus and video sync signals are synchronized to the rising edge of VLCK.

In the progressive SIF-size configuration, there are two options: with parameter VCRS = 0, VCLK is the pixel clock, and the video bus and sync signals are synchronized to the rising edge of VLCK; with VCRS = 1, QCLK_V is the pixel clock, and the video bus and sync signals are synchronized to the rising edge of QCLK_V.

In the Enabled configuration, QCLK_V indicates that the video output contains valid data for at least 8 pixels. Pixels are output in bursts at the VCLK rate and synchronized to VCLK. As far as the sync generator is concerned, however, the pixel clock frequency is QCLK_V (effectively VCLK/4), and this should be used as the pixel rate when determining values for the display timing parameters.

The table below specifies the maximum VCLK frequency allowed in each configuration.

Table 13. Maximum VCLK Frequencies

Configuration	Max. VCLK Frequency	Pixel Rate
Interlaced CCIR-size	PCLK/4	VCLK
Progressive SIF-size (VCRS=0)	PCLK/16	VCLK
Progressive SIF-size (VCRS=1)	PCLK/4	1/4 VCLK (in sync with QCLK_V)
Enabled	PCLK/4	VCLK[1]

[1] In the Enabled video interface configuration, the sync generator is clocked at a frequency of VCLK/4.

Active Region of the Decoded Picture

The decoded picture can be cropped to an "active region" prior to being displayed, as illustrated in Figure 4.

The size of the decoded picture is defined by the horizontal size (HS) and vertical size (VS) parameters given in the sequence header of the video stream. The active region of the decoded picture (the subregion within the decoded picture which will be post processed and output on the VIDOUT bus) is defined by the NAP, NAL, NOP, and NOL set-up parameters. Restrictions on legal values for these parameters are given in Table 14.

Table 14. Legal NAP, NAL, NOP, NOL values

Parameter	Video Interface Configuration	Restrictions		
		Minimum value	Maximum value	Other
NAP[1]	All except Enabled	24	4*int(HS/4)	Multiple of 4
	Enabled			Multiple of 8
NAL	All		VS	none
NOP	All	0	4*int(HS/4)-NAP	Multiple of 4
NOL[2]	All	0	Smaller of VS-NAL, or 254	Even

[1] For high-resolution, NAP must be even (it need not be a multiple of 4).
[2] For high-resolution, NOL need not be even.

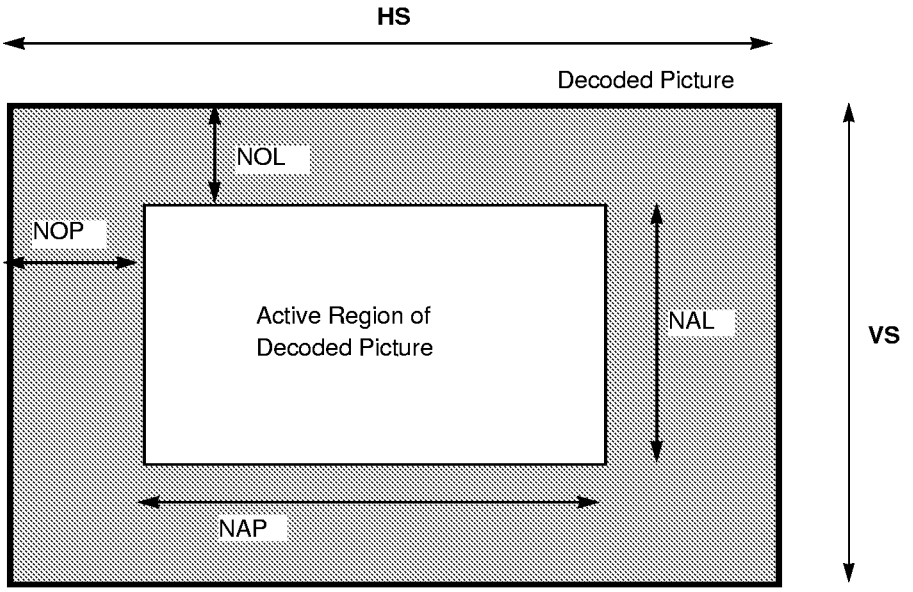


Figure 4. Decoded Picture and Active Region

Note: HS = Horizontal size, VS = Vertical size
HS and VS are found in the video sequence header

Video Sync Signals

Note: In all the diagrams in this section, those specifying the timing of the sync signals and those illustrating their interrelationships, active low sync signals are depicted. These diagrams apply equally well, with reversed polarity of the wave forms, to active high sync signals.

The HSYNC and VSYNC signals are both either inputs or outputs, as specified by the VDIR set-up parameter. The polarities of the HSYNC and VSYNC signals are selected independently using the HSHL and VSHL set-up parameters respectively. HSYNC and VSYNC are selected independently to be short (sync) or long (blanking) waveforms using the HSLN and VSLN fields of the VIDMODE parameter, respectively; but note that the combination of short input HSYNC and long input VSYNC is not allowed.

The set-up parameters NTP, NTL, NBP, NBPF, NDP, NBL, NBLF, NDL, HSW and VSW specify the sync signal waveforms. Table 15, Table 16 and Table 17, at the end of this subsection, show the restrictions on the values of these parameters. These restrictions are required to ensure that the parameters are consistent with one another, and with the other parameters that control the video display. Note that the parameters that specify horizontal timing are always specified in units of pixel periods (for the pixel period effective in each of the interface configurations; see above, under *Video Clocks*).

The timing for a short, active low, output HSYNC is given in Figure 5. In this figure, HSYNC is active for HSW pixel periods. The timing for a long, active low, output HSYNC is given in Figure 6. In this figure, HSYNC is active for NBP + NBPF pixels. HSYNC has a period of NTP pixels.

Figure 7 shows the HSYNC signal (short or long input). HSYNC must have a period of NTP pixels.

The timing for a short, active low output VSYNC is given in Figure 8. In this figure VSYNC is low for VSW lines. The timing for a long, active low, output VSYNC is given in Figure 9. In this figure VSYNC is low for (NBL + NBLF) lines + (NBP + NBPF) pixels. VSYNC has a period of NTL/2 lines for the interlaced CCIR-size configuration, and NTL lines for the progressive SIF-size or Enabled configurations.

Figure 10 shows the timing for short and long, active low input VSYNC signals. VSYNC must have a period of NTL/2 lines for the interlaced CCIR-size configuration, and NTL lines for the progressive SIF-size configuration.

Whenever the edges of long input HSYNC and long input VSYNC should ideally coincide, the edges of VSYNC must not jitter outside the active part of HSYNC.

Note that in order to generate and receive sync signals which comply with the interlaced NTSC and PAL standards, the width of the VSYNC pulse can be defined with resolution of half a line.

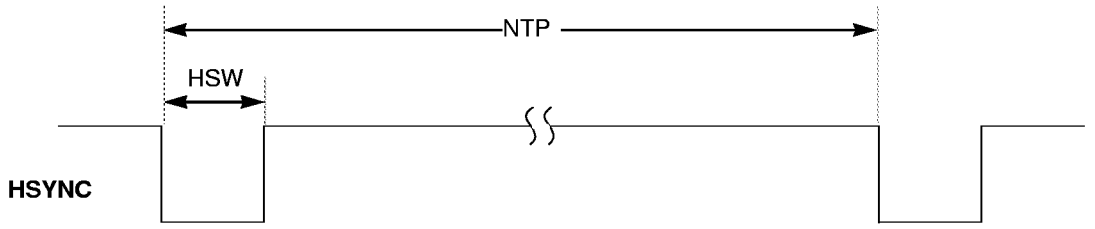


Figure 5. Short output HSYNC

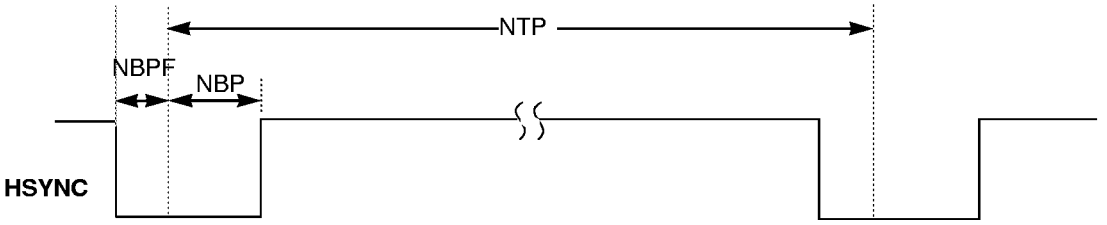


Figure 6. Long output HSYNC

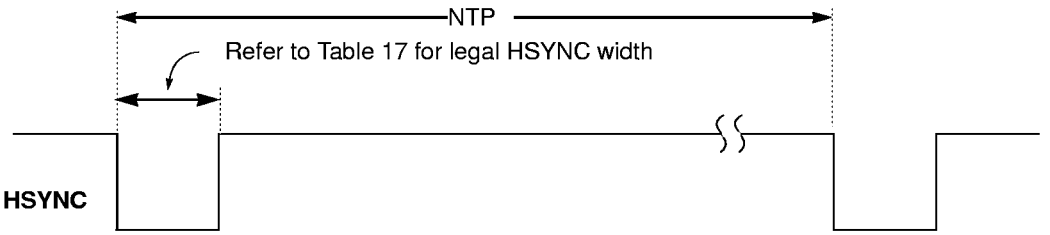


Figure 7. Input HSYNC

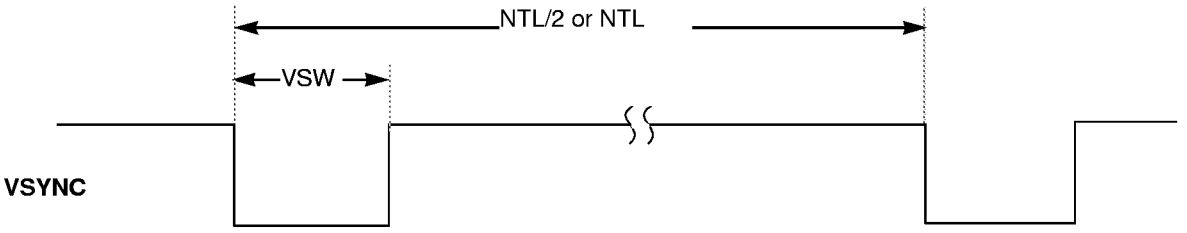


Figure 8. Short output VSYNC

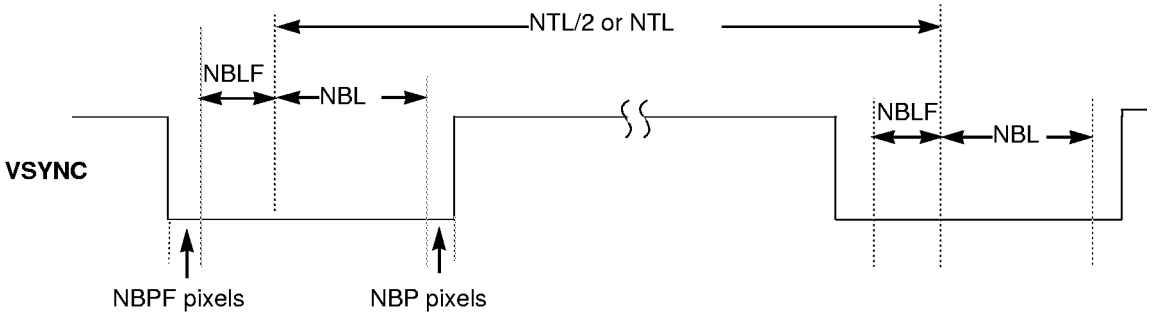


Figure 9. Long output VSYNC

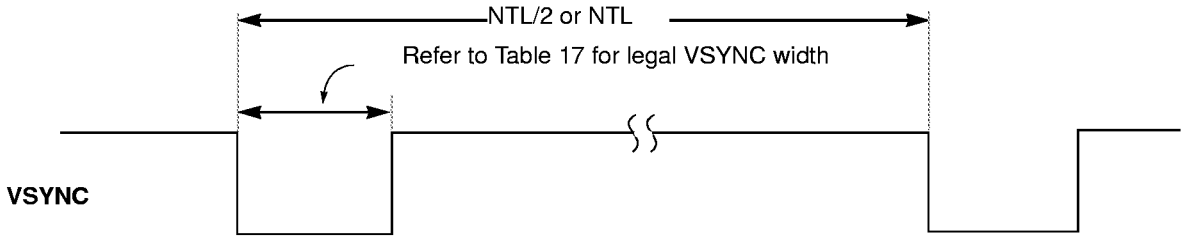


Figure 10. Input VSYNC

Table 15. Restrictions on legal values for NTP and NTL

Parameter	Interface Configuration	Restrictions		
		Minimum	Maximum	Other
NTP[1]	Interlaced CCIR-size; Output HSYNC	NBPF+NBP+NDP+ 2*NAP	1023	must be even
	Interlaced CCIR-size; Input HSYNC	Number of pixels between leading edges of two HSYNCs (maximum of 1023)		must be even
	Progressive SIF-size or Enabled; Output HSYNC	NBPF+NBP+NDP+NAP	1023	none
	Progressive SIF-size; Input HSYNC	Number of pixels between leading edges of two HSYNCs (maximum of 1023)		none
NTL[1]	Interlaced CCIR-size; Output VSYNC	2*(NBLF+NBL+NDL+ NAL)	1023	must be odd
	Interlaced CCIR-size; Input VSYNC	Number of lines between leading edges of alternate VSYNCs (maximum of 1023)		must be odd
	Progressive SIF-size or Enabled; Output VSYNC	NBLF+NBL+NDL+NAL	1023	none
	Progressive SIF-size; Input VSYNC	Number of lines between leading edges of consecutive VSYNCs (maximum of 1023)		none

[1] NTP*NTL*FPS=VCLK rate (or QCLK_V rate if VCRS = 1), where FPS is the display frame rate, based on the VIDS set-up parameter.

Table 16 specifies the restrictions on the relevant set-up parameters for the output sync combinations.

Table 16. Restrictions on legal values for output sync parameters

Sync Combination	Parameters							
	NBP	NBPF	HSW	NDP	NBL	NBLF	VSW	NDL
H-short V-short	a	e	b	f	c, i	i, k	g	h
H-short V-long	a	e	b	f	i, j	i, k	=0	h
H-long V-short	d	e	=0	f	c, i	i, k	g	h
H-long V-long	d	e	=0	f	i, j	i, k	=0	h
Enabled	d	e	=0	=0	i, j	i, k	=0	=0

For the following notes, the notation ( ), [ ] signifies the restrictions relevant to (interlaced CCIR-size), [progressive SIF-size or Enabled] configurations. When a restriction is shown without brackets or parentheses, it applies to all video interface configurations.

a. Minimum = HSW, maximum = NTP/2 or (NTP-2*NAP), [NTP-NAP] whichever is smaller.

b. Minimum = 4.0, maximum = NBP.

c. Minimum = 2.0 or VSW, whichever is larger. Maximum = (int (NTL/2)-NAL), [NTL-NAL].

d. Minimum = 4.0, maximum = NTP/2 or (NTP-2*NAP), [NTP-NAP] whichever is smaller.

e. Minimum = 2, maximum = NTP/2 or (NTP-2*NAP-NBP), [NTP-NAP-NBP], whichever is smaller.

f. Multiple of 4, minimum = 0, maximum = (NTP-2*NAP-NBP-NBPF), [NTP-NAP-NBP-NBPF].

g. Minimum = 2.0, maximum = NBL.

h. Minimum = 0, maximum = (int (NTL/2)-NAL-NBL-NBLF), [NTL-NAL-NBL-NBLF].

i. The sum of NBL and NBLF is restricted to be an integer.

j. Minimum = 2.0.

k. Minimum = 1.0, maximum = (int (NTL/2)-NAL-NBL), [NTL-NAL-NBL].

Table 17 specifies the restrictions on the relevant set-up parameters for the input sync combinations.

Table 17. Restrictions on legal values for input sync parameters

Sync Combination	Parameters							
	NBP	NBPF	HSW	NDP	NBL	NBLF	VSW	NDL
H-short V-short	a	d	=0	e	b, c	c, f	=0	g
H-long V-short	=0	=0	=0	e	b, c	c, f	=0	g
H-long V-long	=0	=0	=0	e	=0	=0	=0	g

For the following notes, the notation ( ), [ ] signifies the restrictions relevant to (interlaced CCIR-size), [progressive SIF-size] configurations. When a restriction is shown without brackets or parentheses, it applies to all video interface configurations.

a. Minimum = width of input HSYNC, maximum = NTP/2 or (NTP-2*NAP), [NTP-NAP] whichever is smaller.

b. Minimum = actual width of input VSYNC or 2, whichever is larger. Maximum = (int (NTL/-2)-NAL), [NTL-NAL].

c. The sum of NBL and NBLF is restricted to be an integer.
d. Minimum = 2.0, maximum = NTP/2 or (NTP-2*NAP-NBP), [NTP-NAP-NBP], whichever is smaller.
e. Multiple of 4, minimum = 0, maximum = (NTP-2*NAP-NBP-NBPF), [NTP-NAP-NBP-NBPF].
f. Minimum =1.0, maximum = (int (NTL/2)-NAL-NBL), [NTL-NAL-NBL]).
g. Minimum =0, maximum = (int (NTL/2)-NAL-NBL-NBLF), [NTL-NAL-NBL-NBLF].

Note: The restrictions on the actual widths of input HSYNC and VSYNC pulses are identical to those for output HSYNC and VSYNC, as specified in the notes to Table 16.

Effective Blanking Interval and Extended Blanking Interval

The specification of the Video Display regions in the next subsection requires the definition of the following terms:

- Effective Blanking Interval
  - The Effective Blanking Interval is related to VSYNC. For a short VSYNC signal, the effective blanking interval begins NBLF lines before the active edge of VSYNC, and continues for NBL lines following the active edge of VSYNC. For long VSYNC, the effective blanking interval is the same as the active period of the VSYNC signal.
- Complete line
  - A Complete Line is all the VCLKs between leading edges of two successive HSYNC signals.
- Extended Blanking Interval.
  - The Extended Blanking Interval is derived from the effective blanking interval as follows. When the effective blanking interval ends in the middle of a complete line (e.g. because of odd NTL in interlaced output, or non-integer NBL) it is extended until the end of the complete line. When the effective blanking interval starts in the middle of a complete line (for the same reasons), and the VSYNC is other than the long input case, the effective blanking interval is extended to cover also the preceding part of the complete line. This is illustrated in Figure 11.

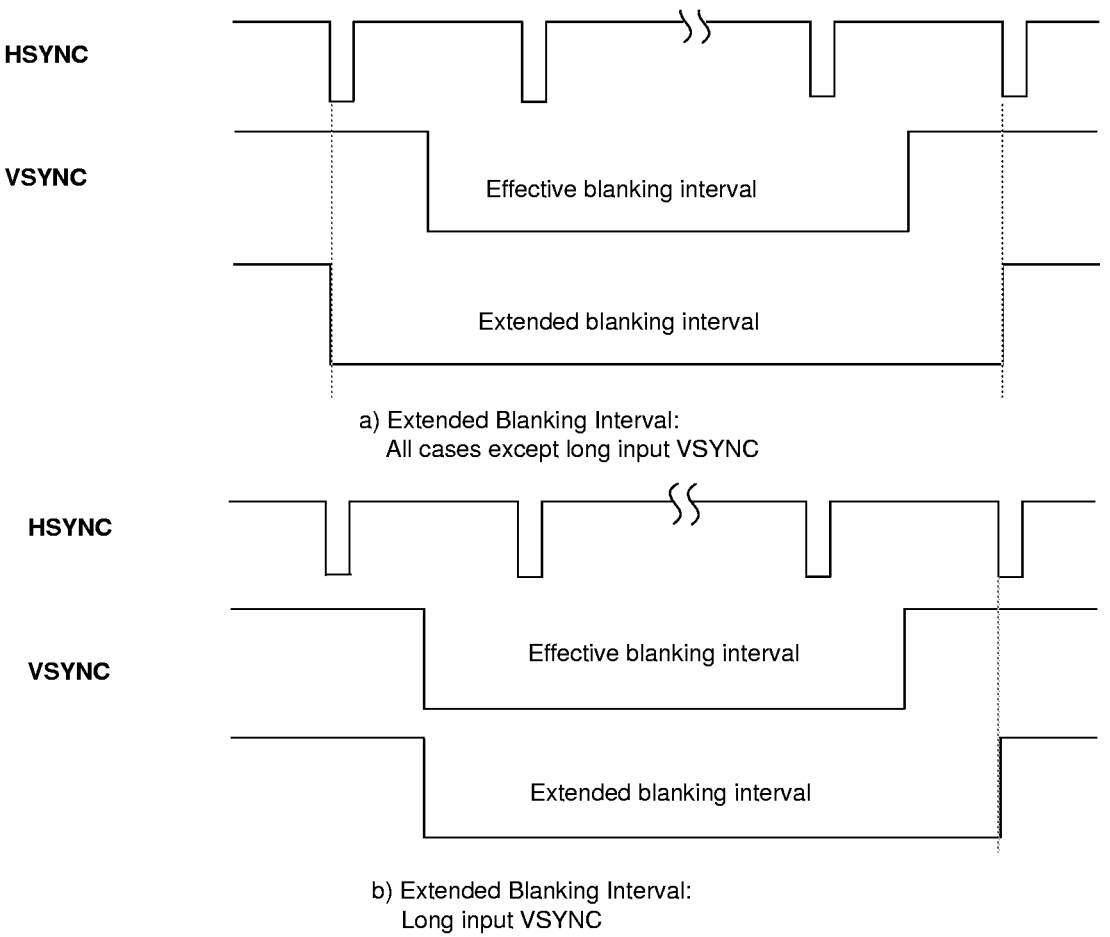


Figure 11. Extended blanking interval derivation from effective blanking interval

Video Display Regions

There are three data regions within a field or frame defined for the VIDOUT data: Active Region, Blanking Region, and Background Color Region. For interlaced CCIR-size configuration, refer to Figure 12. For progressive SIF-size or Enabled configuration, refer to Figure 13.

The set-up parameters NBP, NBPF, NBL, and NBLF define the Blanking Region. The VIDOUT bus is driven to zero in this region.

The set-up parameters NDP and NDL define the horizontal and vertical offsets from the end of the Blanking Region to the start of the Active Region. The Active Region is 2xNAP (for interlaced CCIR-size) or NAP (for progressive SIF-size or Enabled) pixels wide by NAL lines high. The VIDOUT bus is driven with active picture data in the active region.

The Background Color Region is the region between the Blanking Region and the Active Region. The VIDOUT bus is driven with the values specified in the BGRV, BGGY, BGBU set-up parameters.

A special condition exists when HSYNC is a long input. In this case, the Blanking Region is extended by four pixels following the activation of the HSYNC signal. NDP is counted after these four pixels. Also, the first four pixels following the deactivation of HSYNC will be background color. If VCRS = 1, this delay is two pixels instead of four.

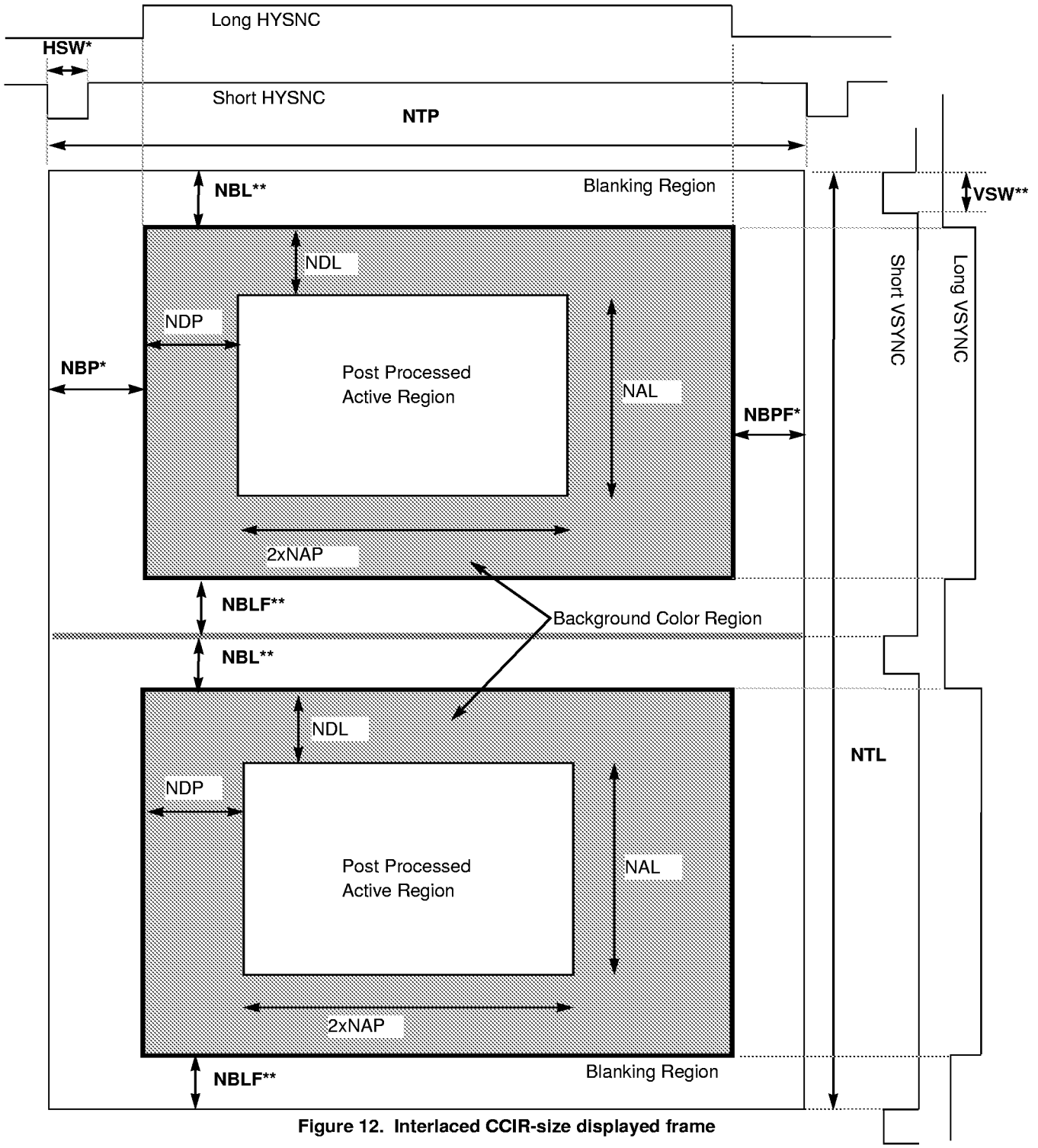


Figure 12. Interlaced CCIR-size displayed frame

* Not applicable when HSYNC signal is long input. In this case, these parameters are set to zero and the HSYNC waveform is determined by the source.
** Not applicable when VSYNC signal is long input. In this case, these parameters are set to zero and the VSYNC waveform is determined by the source.
Note also that the vertical parameters NBL, NBLF or the long input VSYNC are the extended versions, as described above.

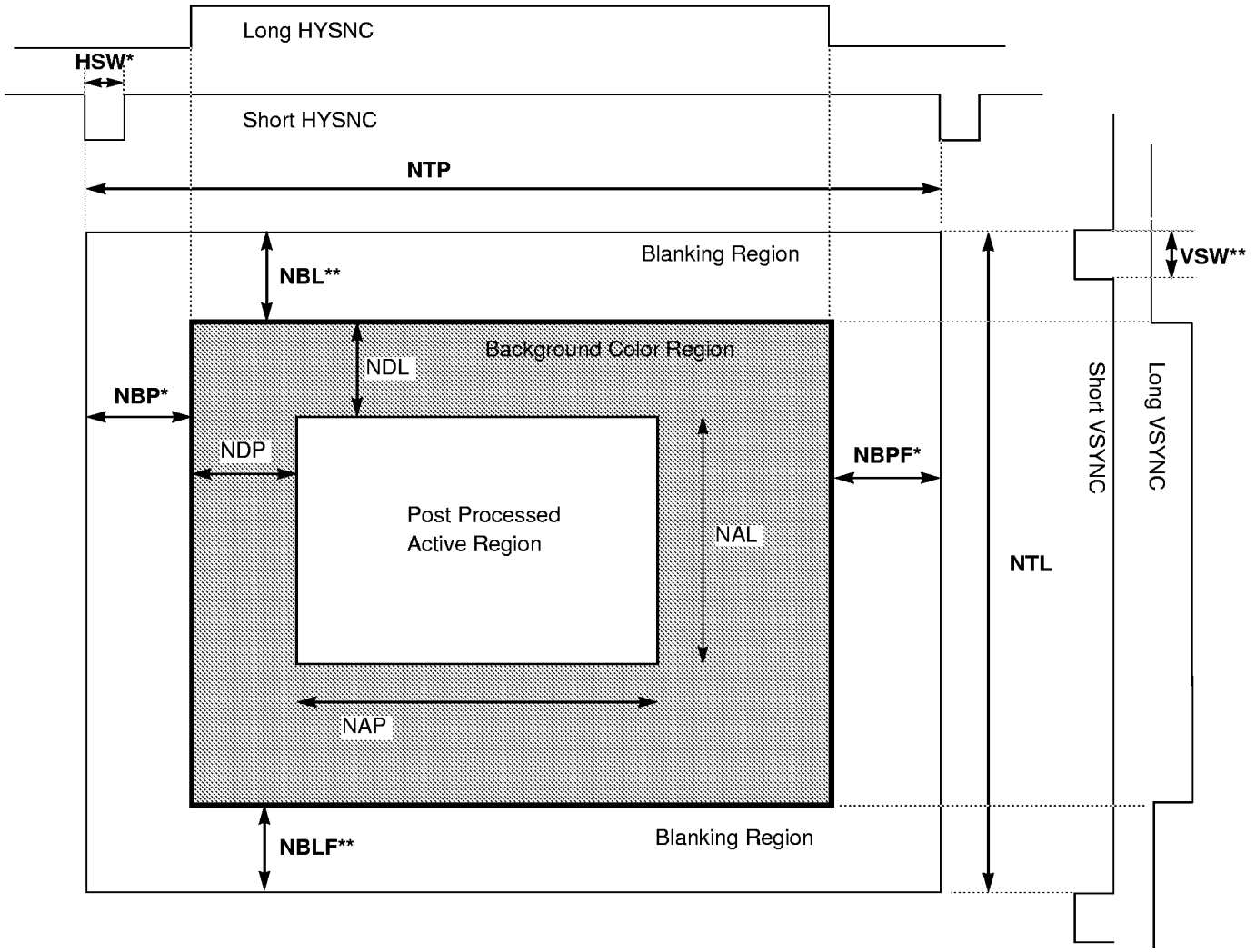


Figure 13. Progressive SIF-size or Enabled mode displayed frames

* Not applicable when HSYNC signal is long input. In this case, these parameters are set to zero and the HSYNC waveform is determined by the source.
** Not applicable when VSYNC signal is long input. In this case, these parameters are set to zero and the VSYNC waveform is determined by the source.
Note also that the vertical parameters NBL, NBLF or the long input VSYNC are the extended versions, as described above.

The FI_EN signal

For interlaced CCIR-size configuration with output syncs, FI_EN can be a field index, a composite blanking signal, or a high-resolution display indicator, as determined by the VBLN and HRS set-up parameters. With input syncs it is required to be a field index.

When FI_EN is defined to be a composite blanking signal, it is driven active in the Blanking region defined in Figure 12.

When FI_EN is defined as a high-resolution display indicator, FI_EN is an active low signal indicating high-resolution display output.

When FI_EN is defined to be a field index signal, it is active during field I and inactive during field II. When the sync signals are output, FI_EN is driven by the ZR36110; when the sync signals are inputs, FI_EN must be driven externally. (Recall that field I is defined to be the field that starts at HSYNC, while field II is defined to start in the middle of a line.)

Figures 14 through 21 show the relation of FI_EN (as field index) and VSYNC to HSYNC under several different conditions. The conditions depend on the type of HSYNC and VSYNC (long or short) being used, and on whether non integer VSW or NBL/NBLF (e.g., for NTSC) or integer VSW or NBL/NBLF (e.g., for PAL) output video format is being used. All these examples show active-low syncs, and FI_EN low during Field I, but apply equally well to the complementary cases.

Enabled Video Interface Configuration

In Enabled configuration, the video output is progressive and SIF-sized, the pixel format is YUV 2:1:1, and HSYNC and VSYNC must be outputs and long. The U and V components can be selected to be either biased or unbiased.

The FI_EN signal is an input which enables the video output. The active region of the decoded picture is output with the original resolution. Video is output only when enabled by the FI_EN input signal, starting one VCLK cycle following the activation of FI_EN. When FI_EN is de-activated, the VIDOUT bus floats, starting one VCLK cycle following the de-activation of FI_EN. Whenever there are at least 8 valid pixels in the video output FIFO, the QCLK_V signal is driven high, and 8 pixels can be read out in a burst by enabling FI_EN, before QCLK_V needs to be checked again.

All the pixels of the picture must be read out in the interval between the trailing edge of VSYNC and the leading edge of the next VSYNC; HSYNC can be disregarded. It is the responsibility of the circuits which generate the enable signal to make sure that the average pixel rate is maintained over the frame, when the averaging period is a quarter of the frame. The receiver of the video output data must count the number of active pixels per line and number of active lines to determine when all data of a picture have been read out.

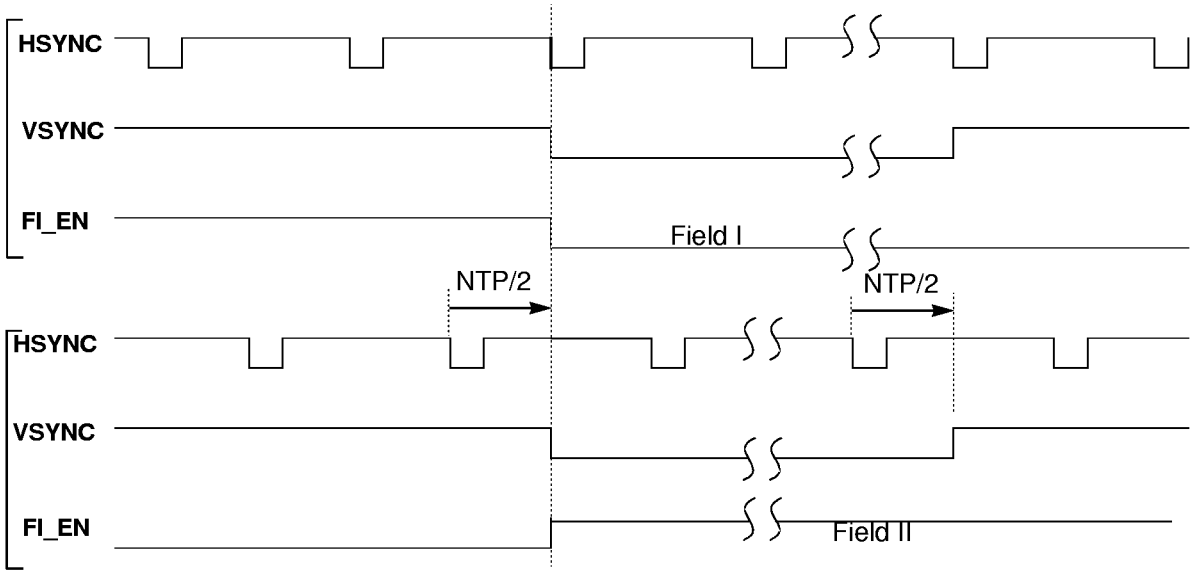


Figure 14. Field Index: (short HSYNC, short VSYNC, width of VSYNC is integer number of lines)

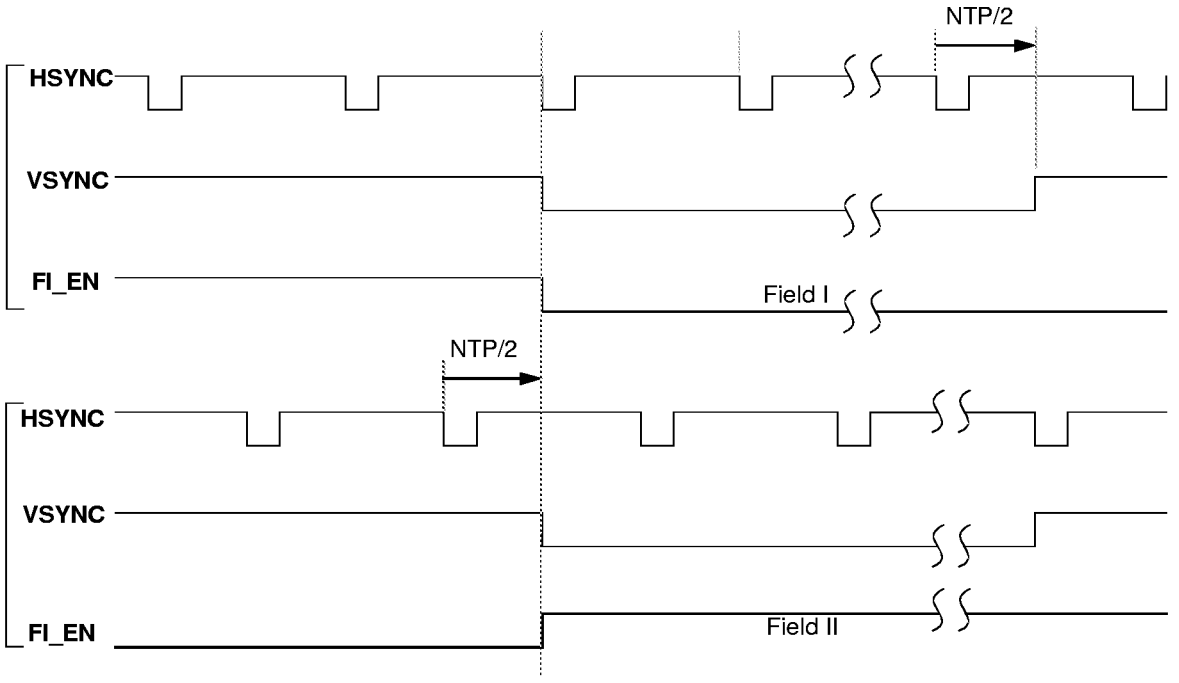


Figure 15. Field Index: (short HYSYNC, short VSYNC, width of VSYNC is non-integer number of lines)

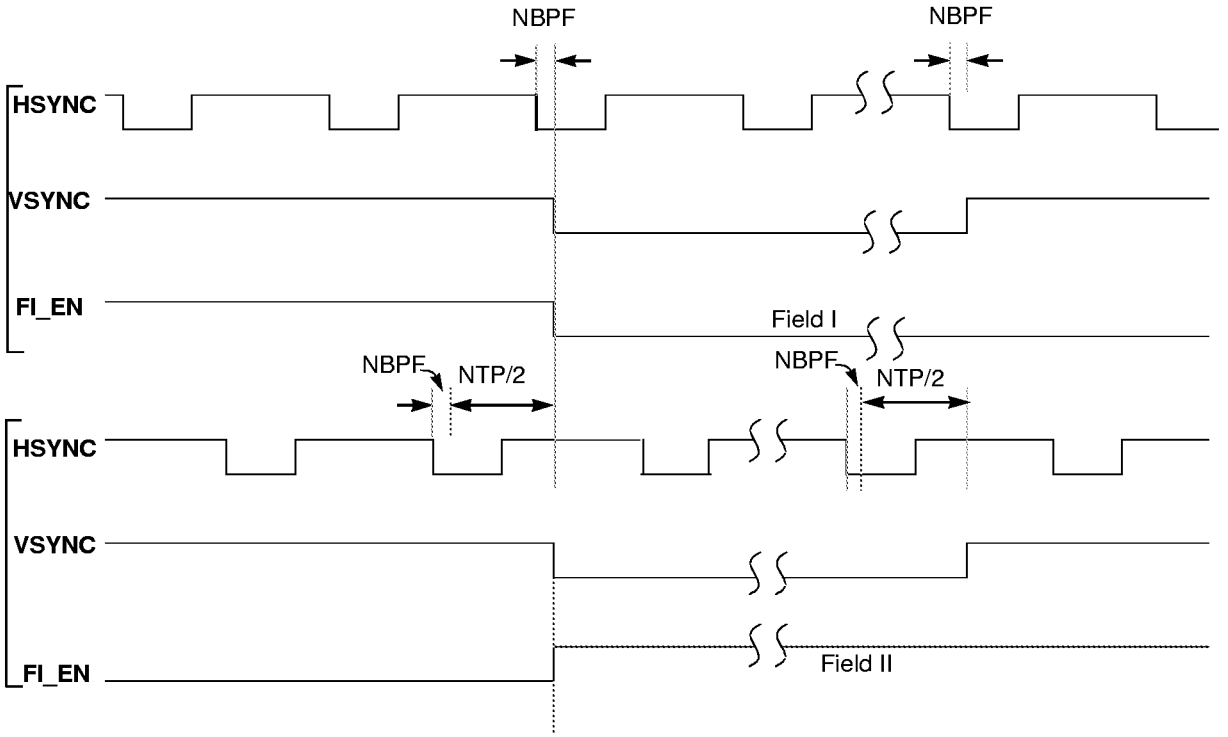


Figure 16. Field Index Signal: (long HSYNC, short VSYNC, width of VSYNC is integer number of lines)

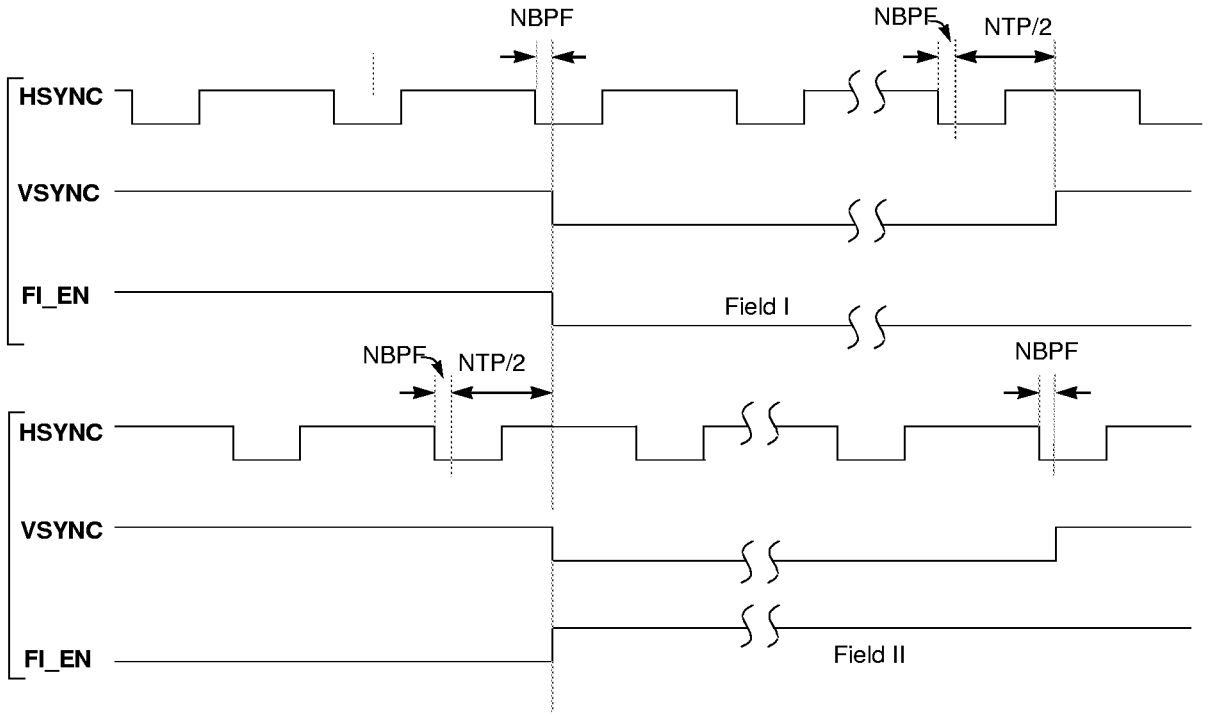


Figure 17. Field Index: (long HSYNC, short VSYNC, width of VSYNC is non-integer number of lines)

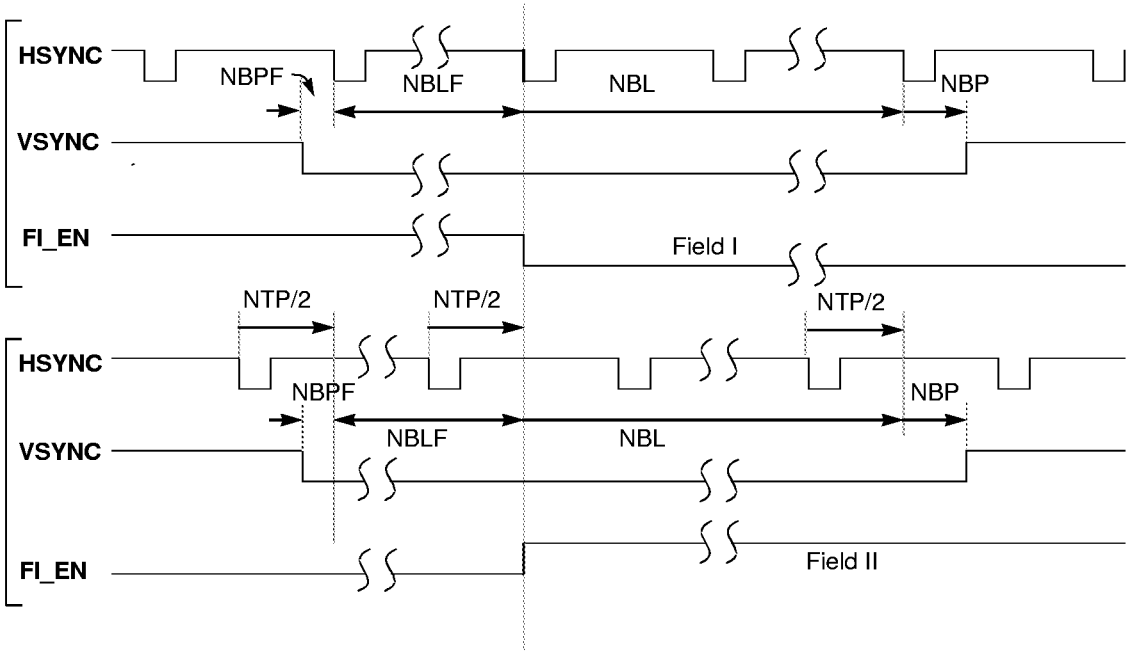


Figure 18. Field Index: (short HSYNC, long VSYNC, width of NBL is integer number of lines)
Note: Sync. signals are always output for the short HSYNC, long VSYNC case

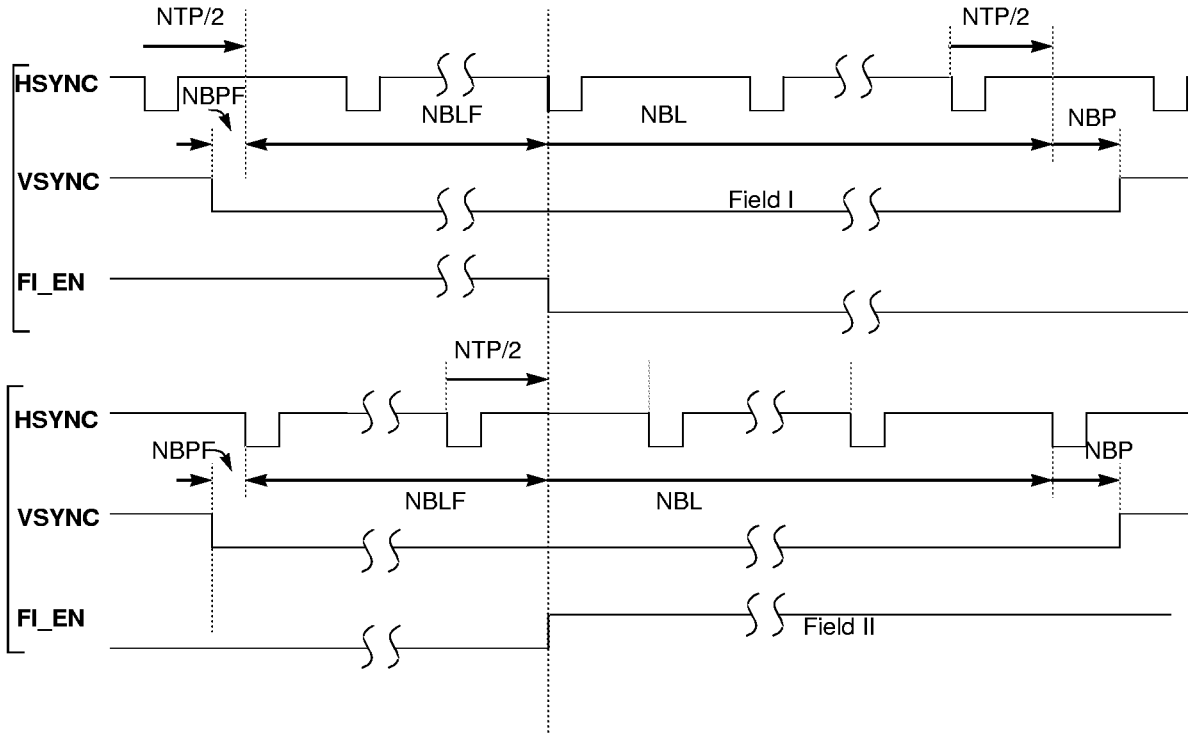


Figure 19. Field Index: (short HSYNC, long VSYNC, width of NBL is non-integer number of lines)
Note: Sync. signals are always outputs for the short HSYNC, long VSYNC case.

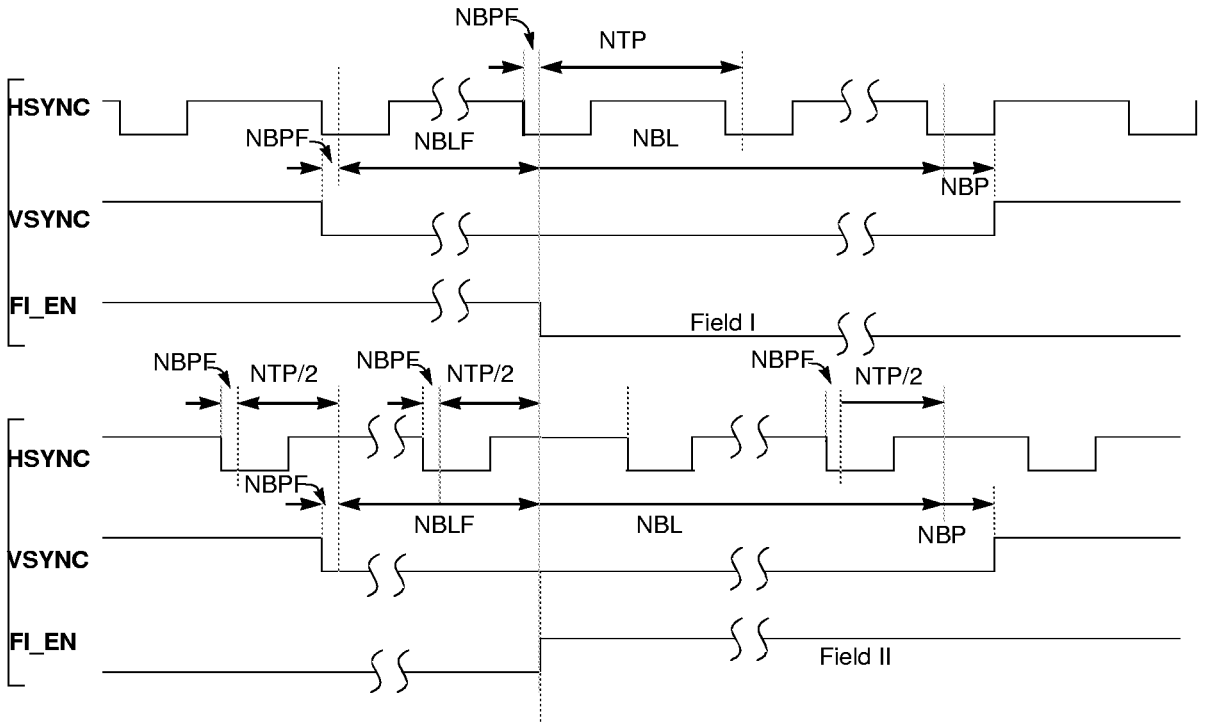


Figure 20. Field Index: (long HSYNC, long VSYNC, width of NBL is integer number of lines)

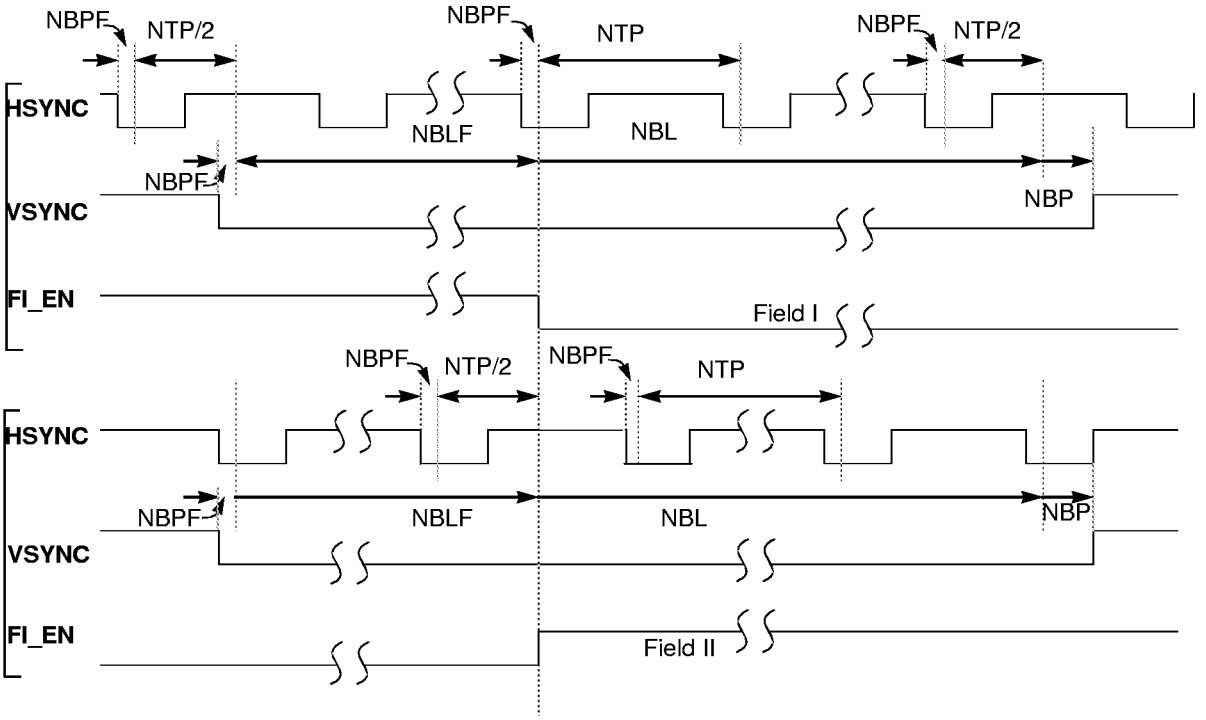


Figure 21. Field Index: (long HSYNC, long VSYNC, width of NBL is non-integer number of lines)

SERIAL PORTS INTERFACE

The ZR36110 has two serial output ports that operate independently of each other. These serial ports can be used to transfer the audio or private streams embedded in a system bitstream to decoders for these streams.

Each serial port has one data line (SP1DAT and SP2DAT), used to transfer the bitstream, one frame synchronization line (SP1FRM and SP2FRM) and one clock line (SP1CLK and SP2CLK). The transfers of data are done in 16-bit groups, which are called frames. The SP1FRM and SP2FRM signals synchronize the transfer of these frames.

Serial Port Modes

The S2FT, S2CD, S2FS, and S2AC fields of the SPOMODE set-up parameter specify serial port 2, while the S1FT, S1CD, S1FS, and S1AC fields specify serial port 1.

The clock signals can be specified as inputs or as outputs, as specified in the SPOMODE set-up parameter. The *frame synchronization* signals can be specified as pulse type, transition type, or window type; these signal types are described below.

Each serial port can be specified to be active or inactive. When active, a serial port will output the bitstream assigned by the SP1SID or SP2SID parameters, respectively. When defined to be inactive, a serial port does not output data. When decoding a video-only bitstream, both serial ports must be defined to be inactive.

Serial Port Transfer Rate

When the clock signal of a serial port is defined to be an output, the clock frequency is specified to be an integral divisor of the VCLK frequency via the SP1CD or SP2CD parameter. When the parameter is not zero, the specified frequency must be equal to or above the bit rate specifications of the stream assigned to the port.

SP1BR or SP2BR (when not zero) should be programmed or calculated to be the ratio of the bit rate to the serial port clock frequency. The ZR36110 uses this value to generate a constant average data transfer rate from the serial port equal to this bit rate.

Frame Synchronization Signal

The frame synchronization signal indicates the beginning of a serial port frame (16 bits of data). The signal is activated whenever there is a 16-bit word of bitstream data to be clocked out. The two frame synchronization signals may be independently selected to be either pulse type, transition type, or window type. Pulse type frame synchronization signals are active high for one serial port clock period, which precedes the first (earliest) bit of the frame. The pulse type frame synchronization signal is activated and deactivated with the rising edge of the clock signal of the same port. The transition type frame synchronization signal changes levels at the beginning of each frame. The transition is concurrent with the falling edge of the clock and precedes the first (earliest) data bit by one clock cycle. Before the first activation, the signal is low, and the first transition (before the first word is output) is from low to high. The window type signal is activated and deactivated concurrently with the falling edge of the clock, and has a width of 16 serial port clock periods.

The length of a frame, that is, the interval between two activations (or transitions) of the frame synchronization signal, is at least 16 serial port clock periods, but may be larger depending on the value of SP1BR or SP2BR. When data is being output from the port, the interval typically fluctuates between two intervals that differ by one serial port clock period. For example, if SP2BR is 1.0, all frames are exactly 16 clocks long. If SP2BR is 0.5, all frames are 32 clocks long. If SP2BR is slightly larger than 0.5, say 0.5 + 1/128, the frame length fluctuates between 31 and 32 clocks.

The SP1FRM (or SP2FRM) signal is activated whenever there is a word of bitstream data to be clocked out from port 1 (or port 2).

Figure 22 and Figure 23 illustrate the timing relationships at the beginning of a serial port frame, with transition-type frame sync, for two representative cases. In the first case, the length of the previous frame was exactly 16 clocks, and in the second case it was greater than 16 clocks, specifically 18 clocks. Figure 24 and Figure 25 show the same examples for pulse-type frame sync. Figure 26 and 27 illustrate window-type frame sync, with the same two representative cases. These figures show the signals of serial port 1, but are equally valid for the corresponding signals of serial port 2.

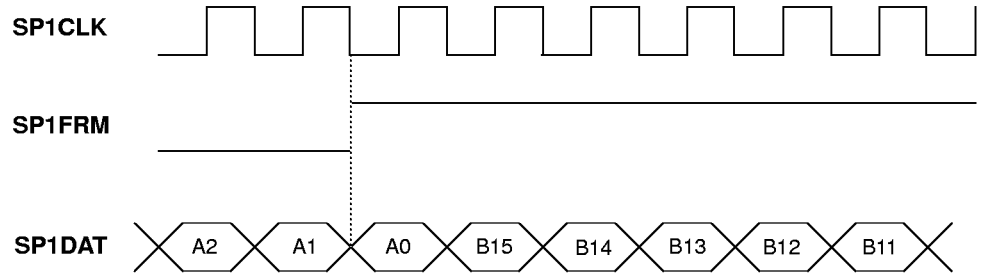


Figure 22. Beginning of serial port frame with transition frame sync signal, length of previous frame is 16 clocks

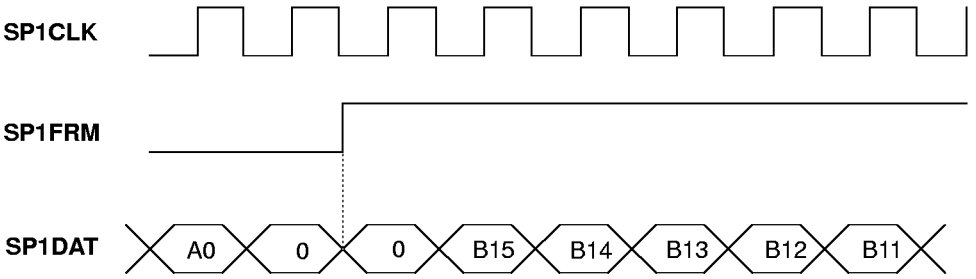


Figure 23. Beginning of serial port frame with transition frame sync signal, length of previous frame is 18 clocks

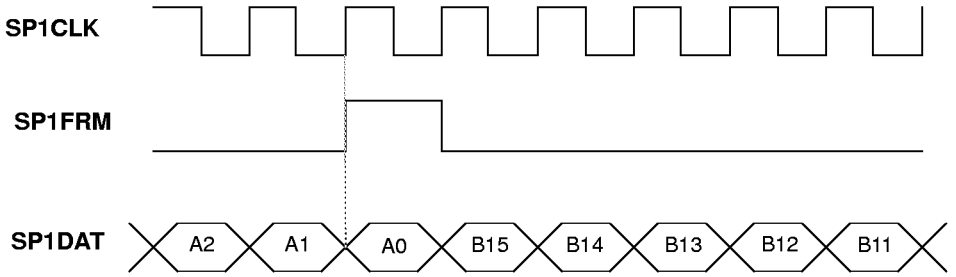
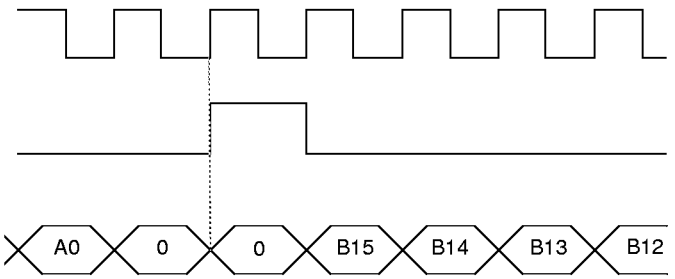
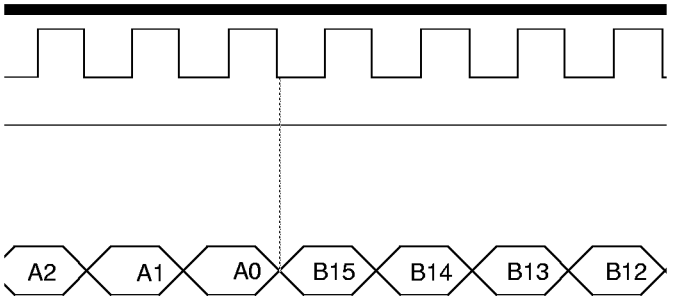


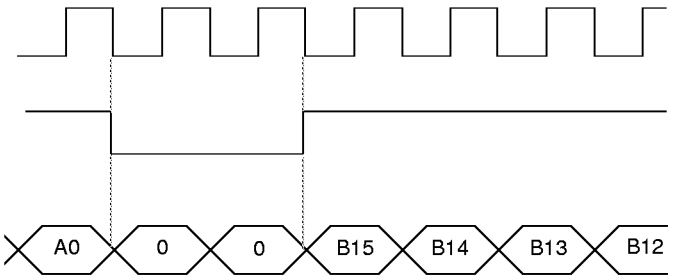
Figure 24. Beginning of serial port frame with pulse frame sync signal, length of previous frame is 16 clocks



25. Beginning of serial port frame with pulse frame sync length of previous frame is 18 clocks



26. Beginning of serial port frame with window type SP1F length of previous frame is 16 clocks



7. Beginning of serial port frame with window type SP1FR length of previous frame is 18 clocks

DRAM INTERFACE

The ZR36110 uses external DRAM to buffer the video and serial port data streams and to store decoded pictures. The timing specifications for the DRAM interface support typical devices of 80ns speed or faster. The DRAM interface circuits in the ZR36110 assume that the DRAM structure is symmetric, 512 rows by 512 cells each. Based on this assumption of DRAM structure symmetry, only nine address lines are used. The DRAM must be configured as a 256K x 16 memory and therefore can use either four 256K x 4 devices or one 256K x 16 device.

For CCIR-PAL, 2 DRAM banks are required for full resolution storage of high-resolution still images. If there is only one DRAM bank, or when the HHRS set-up parameter is set, only one field of the decoded CCIR-PAL image is stored.

The DRAM interface consists of a 16-line data bus (RAMDAT), a 9-line address bus (RAMADD) and four control lines ($\overline{RAS}$, $\overline{CAS1}$, $\overline{CAS2}$, and $\overline{WE}$).

The write and read operations are in the "fast page" mode. The ZR36110 indicates a write cycle by activating the $\overline{WE}$ signal, otherwise the cycle is a read. The output enable pin of the DRAM must be tied active.

The DRAMs are refreshed at rate not less than 512 rows in 8 milliseconds. The timing for the refreshes is given in the *AC Characteristics* section.

Note that the DRAM cannot be accessed by the host, either directly or indirectly, but only by the internal MPEG decoding circuitry of the ZR36110.

CLOCK INPUTS

The ZR36110 requires a general clock, GCLK, that is used as the reference clock for an internal PLL clock multiplier. The output of the clock multiplier (available on the PCLK pin; but note that this signal is provided for monitoring purposes only, and must not be loaded) is used to run the internal processing circuits, and to derive the DRAM interface timing. By means of the $\overline{MB4}$ pin, the PLL can be configured to multiply GCLK by 4 ($\overline{MB4}$ low) or 4.5 ($\overline{MB4}$ high). This allows the attainment of a PCLK frequency in the required range, when GCLK is one of a number of frequencies commonly available in video circuits.

As an alternative to using an external clock generator, an internal crystal oscillator can be used to generate GCLK. For this, a crystal of the appropriate resonant frequency is connected between the GCLK and XT pins, with a 20pF capacitor connected from each terminal to ground.

The other clock that must be provided to the ZR36110 is the video clock VCLK, which is used as the timing reference for the video interface and the video sync generator. VCLK is also the reference from which the time delays required for video and audio synchronization are derived. VCLK can be asynchronous with and independent of GCLK, but it is legitimate for GCLK and VCLK to be connected to the same clock generator if this is convenient.

RESET AND STANDBY

Activation of the $\overline{\text{RESET}}$ pin of the ZR36110 affects the device as follows:

- If $\overline{\text{RESET}}$ is active for 160 or more GCLK periods, this is called a "cold reset".
- If $\overline{\text{RESET}}$ is active for at least 32 and less than 129 GCLK periods, this is called a "warm reset", which is used for testing only.
- If $\overline{\text{RESET}}$ is active for between 129 and 159 GCLK periods, behavior of the device is unpredictable.
- If $\overline{\text{RESET}}$ is active for less than 32 GCLK periods, there is no effect.

Cold Reset

A cold reset causes the PLL to lock on the frequency of GCLK. It also initializes the set-up parameters to their default values. It is *required* after any of the following events that invalidate the PLL lock:

- Power-up
- Deactivation of the $\overline{\text{STDBY}}$ signal
- A change in the frequency of GCLK (greater than the drift of a typical crystal oscillator)
- A change in the $\overline{\text{MB4}}$ input signal

A cold reset *must* also precede either of the following initialization changes:

- Any change to one or more of the "fixed" set-up parameters
- Loading a different version of the first microcode program (described in the *Initialization* section)

If $\overline{\text{RESET}}$ is active (low) at power up, it must remain active for at least 2.5 milliseconds after VCC, GCLK, $\overline{\text{MB4}}$, and $\overline{\text{STDBY}}$ have stabilized, to ensure that the PLL locks correctly. If $\overline{\text{RESET}}$ is high at power up, it must remain high for at least 2.5 milliseconds, after VCC, GCLK, $\overline{\text{MB4}}$, and $\overline{\text{STDBY}}$ have stabilized, before a cold reset pulse is applied to trigger the PLL to lock.

The PLL lock procedure starts when $\overline{\text{RESET}}$ goes high, and terminates not more than 5000 GCLK periods thereafter. When the PLL is locked, the READY and IDLE signals and status bits are high, indicating that the device is ready for initialization *as described in the Initialization section.*

Standby Power

The ZR36110 can be switched to Standby power, by activation of $\overline{\text{STDBY}}$, only if it is currently idle and the PLL is stable. While in the Standby state, output signals are forced to float (with suitable pull-ups or pull-downs, as described in Table 18). The external DRAM is not refreshed, so its contents are lost. In this state the ZR36110 consumes a minimum amount of power.

After the de-activation of $\overline{\text{STDBY}}$, a cold reset is required before the ZR36110 can be operated.

If $\overline{\text{RESET}}$ and $\overline{\text{STDBY}}$ are both active, the ZR36110 consumes more than the specified standby power. Note that for the device to recover correctly from this condition, $\overline{\text{RESET}}$ must be activated after $\overline{\text{STDBY}}$ is activated, and must be deactivated before $\overline{\text{STDBY}}$ is deactivated.

Signal States Under Standby and Reset Conditions

Table 17 shows the states of output and bidirectional signal pins under the following conditions:

- *Standby, when* $\overline{\text{STDBY}}$ *is active and* $\overline{\text{RESET}}$ *is inactive,*
- *Cold Reset,* starting when $\overline{\text{RESET}}$ has been deactivated and ending at most 5000 GCLK periods after its deactivation, when the PLL is locked,
- Standby with reset, when $\overline{\text{RESET}}$ and $\overline{\text{STDBY}}$ are both active,
- After a cold reset, when the PLL is locked and READY is active.

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Table 18. Signal States Under Standby and Reset Conditions [1] [2] [3] [4]

Name	Type O: output B: Bidirectional	Standby	Cold Reset	Standby + Reset	After Cold Reset
IDLE	O	floating+weak pullup	high	floating	high
VIDOUT	O	floating+weak pulldown	floating +weak pulldown	floating	floating +weak pulldown
QCLK_V	O	floating+weak pulldown	low	floating	VCLK/4
HSYNC	B	floating+weak retention	input enable	floating	input
VSYNC	B	floating+weak retention	input enable	floating	input
FI_EN	B	floating+weak retention	input enable	floating	input
BUSDAT	I/B	floating+weak retention	floating +weak retention	floating	input (while $\overline{\text{BUSCS}}$ is high)
DREQ	O	floating+weak pulldown	low	floating	low
READY	O	floating+weak pulldown	low	floating	high
RAMDAT	B	floating +weak pulldown	floating +weak pulldown	floating	unknown output
RAMADD	O	floating +weak pulldown	floating +weak pulldown	floating	unknown
$\overline{\text{RAS}}$	O	floating+weak pullup	high	floating	high
$\overline{\text{CAS}}$	O	floating+weak pullup	high	floating	high
$\overline{\text{WE}}$	O	floating+weak pullup	high	floating	high
SP1DAT	O	floating+weak pulldown	floating +weak pulldown	floating	low
SP1CLK	B	disable+internal retention	input enable	enable	input
SP1FRM	O	floating+weak pulldown	floating +weak pulldown	floating	low
SP2DAT	O	floating +weak pulldown	floating +weak pulldown	floating	low
SP2CLK	B	disable+internal retention	input enable	enable	input
SP2FRM	O	floating+weak pulldown	floating +weak pulldown	floating	low

1. A weak pullup is implemented as a weakly conducting P channel transistor. Pullup current is less than 70 microamps.
2. A weak pulldown is implemented as a weakly conducting N channel transistor. Pulldown current is less than 70 microamps.
3. An internal pullup is used only to prevent excessive current consumption when an input pin is disabled. Leakage current from this pullup or pulldown is not measured at the input pin. All input-only pins have internal pullups or pulldowns in Standby.
4. Retention means that the pin is pulled in the direction of the level (high or low) that the pin had when entering the state.

INITIALIZATION

Before it can start decoding an MPEG bitstream, the ZR36110 must be initialized by loading the microcode and set-up parameters. Microcode is provided in three parts: the first part consists of 4096 bytes, the second of 3584 bytes, and the third of 3584 bytes. Each part may have more than one variant, to support different types of applications.

A complete initialization is required in the following circumstances:

- After power-up.
- When the first part of the microcode must be changed.
- Whenever a cold reset is performed for any reason.

When only the second part, and/or the set-up parameters, and/or the third part of the microcode must be changed, a partial re-initialization suffices, as described below.

A complete initialization procedure begins with a cold reset of the ZR36110, and continues in the following sequence:

1. When the cold reset ends and the PLL is locked, the READY signal and the READY status bit go active. The host must wait for this before proceeding with the initialization. Note that the host bus is in its default configuration after cold reset: I/O mode, 8-bit bus width, BSLN=16.
2. When READY is active, the host can load the first part of the microcode. This is done by writing the 4096 bytes to address 01. There is no need to recheck the READY signal at any time during the load, so the microcode can be loaded in a single burst if so desired.
3. Following the loading of the first part of the microcode, the LDPF status bit can be read. If it is 1, the microcode load was successful and initialization can continue. If it is 0, the load failed, and the initialization procedure must be restarted with a cold reset (the only way to restore the state of the test bit to 1).
4. The host then loads the second part of the microcode by writing the 3584 bytes to address 11. The state of READY is not relevant for this microcode load.
5. Following the loading of the second part of the microcode, the LDPF status bit can be read. If it is 1, the load was successful. If it is 0, the load failed, and the initialization procedure must be restarted with a cold reset.
6. After loading the second part of the microcode, the host must load the set-up parameters (the complete set of 128 bytes). This is done using writes to address 00. The data must be transferred to the ZR36110 in bursts of at most BSLN writes; prior to each burst, the host must check that the READY status bit or the READY signal line is active. Note that if the set-up parameters define a change of the host bus configuration, this change takes effect only *after* the next Go on-line command; the initialization continues with the prevailing host bus configuration. Other interface signal changes affected by the set-up parameters take effect soon after the parameters are loaded.
7. As the final step in the initialization, the host loads the third part of the microcode by writing the 3584 bytes to address 11. The host must wait until READY is active before starting this microcode load, but after that READY and BSLN are irrelevant and the microcode can be loaded in a single burst. The LDPF status bit is also an indication of correct loading of the third part of the microcode, exactly as for the second part.

If it is necessary to change only the second part, the set-up parameters, or the third part of the microcode, a cold reset is not required. Only a partial re-initialization, consisting of reloading the second part of the microcode, loading the set-up parameters (all 128 bytes), and loading the third part of the microcode, must be performed. The partial re-initialization uses the prevailing host bus configuration (bus width, byte order and BSLN). Before starting a partial re-initialization, IDLE and READY must be active; subsequently the sequence can proceed according to stages 4 - 7 above.

Note: After the set-up parameters are loaded, the display always reverts to the background color.

PLAYBACK OPERATION

This section describes how the ZR36110 operates after it has been initialized (as described in the *Initialization* section). It covers the behavior of the device in response to each of the on-line commands mentioned in the *On-Line Commands* section.

General principles

Decoding and display of the video, and consumption of the MPEG bitstream, are tightly synchronized to VSYNC, the vertical sync signal, in the following way.

In the simplest case, the picture rate defined in the bitstream is the same as the video output frame rate defined by VSYNC; for example, a 29.97 pictures-per-second bitstream with 29.97 frames per second NTSC display, or a 25 pictures-per-second bitstream with 25 frames per second PAL display. Every video frame, a new decoded picture is read out from the DRAM and displayed. This effectively determines that the picture decoding rate must be the same as the display frame rate, since a new picture must be ready to be displayed at the beginning of every frame. (If the video interface is configured for progressive SIF-size, a frame begins every VSYNC; if it is configured for interlaced CCIR-size, a frame begins every second VSYNC.) This rate of picture decoding in turn ensures that the bitstream will, on the average, be consumed at its nominal bit rate. This is

illustrated in Figure 28, where the marks on the time lines indicate the scheduled decoding and display start times.

As indicated in the figure, because of the presence of B-pictures requiring prediction from both an earlier and a later reference frame, the order in which the pictures are encoded in the bitstream is not the same as the display order. A typical display order is $I_1B_1B_2P_1B_3B_4P_2$..., and the corresponding decoding

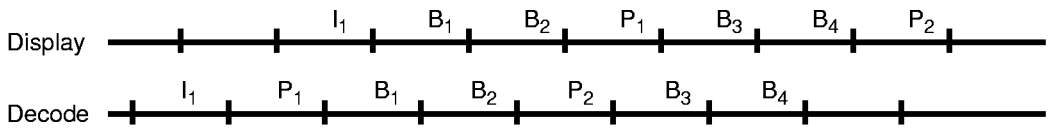


Figure 28. Decoding and Display

order is $I_1P_1B_1B_2P_2B_3B_4$.... (The picture indices here and in the figures have no meaning and are for illustration only.) Thus, I- and P-pictures are completely buffered in DRAM before they are displayed whereas B-pictures do not need to be. The ZR36110 starts to display a B-picture soon after starting to decode it, but I-pictures and P-pictures, after decoding, are displayed at intervals that depend on the arrangement of encoded pictures.

When playing back a bitstream in which the picture rate is not the same as the display frame rate, the ZR36110 can exactly compensate for the difference, for all the common picture rates, with standard NTSC or PAL display frame rates. Consequently, the correct relationships of display, decoding and bitstream consumption rates are preserved, on the average (see *Frame Rate Conversion*).

In the interests of clarity, all the illustrations in this section assume that the display frame rate is equal to the bitstream picture rate.

While normal playback is in progress, the on-line command register is checked at every decoding start time, and if there is a pending command, it is executed immediately. While execution of a command is in progress, the register is checked only when the command has completed execution, or for certain commands at other times, as indicated below.

Bitstream Buffering

When decoding a system multiplexed bitstream or video-CD sectors, the ZR36110 demultiplexes the video, audio and private streams and stores them in separate buffers of the DRAM. As long as no buffers are full, the ZR36110 requests additional bitstream transfers by activating DREQ (in DMA transfer mode) or READY (in I/O transfer mode). If one of these buffers is full, the ZR36110 stops requesting data until all buffers are not full. A buffer full condition is indicated by bit DRBF of STATUS1. It is the responsibility of the host I/O or DMA controller to ensure that the buffers do not underflow.

When the host is unable to keep the average input bitstream rate as needed, code buffer "starving" may result. When a starving condition occurs, the ZR36110 pauses either the video only or both the video and the audio, as needed, until there is enough coded data in the code buffer. Such a pause is indicated by bit STRP of STATUS1.

If the bitstream is provided to the ZR36110 at a constant rate which is exactly equal to the encoded bit rate, the VSYNC clock should be locked to the bit rate.

In the case of a video-only or serial port-only bitstream, no demultiplexing takes place and the entire bitstream is stored in the buffer.

Note that an on-line command, such as Pause, that causes playback to pause, does not necessarily cause the ZR36110 to stop requesting the bitstream immediately, but only when one of the buffers fills up.

For system-multiplexed bitstreams, the audio and private bitstreams are mapped to serial ports 1 and 2, as determined by the SP1SID and SP2SID set-up parameters. The ZR36110 will only buffer, decode and output a stream on a serial port if the Serial Port Active bit (S1AC or S2AC) is set for that port. Otherwise, the audio and/or private data packets will be discarded. When decoding a video-only bitstream, both serial ports must be disabled by zeroing S1AC and S2AC.

When the XCODE bit of the SYSMODE parameter is reset, the information transferred by the host is in system-multiplexed format. When the XCODE bit of the SYSMODE parameter is reset,

information transferred by the host consists of Video-CD sectors. These sectors are comprised of the system-multiplexed bitstream, divided into sequential pieces. Each sector contains a header, a single piece of the system-multiplexed bitstream, and a trailer. The ZR36110 removes the headers and trailers and recombines the pieces, in order, to get back the system-multiplexed bitstream. The value of the Trigger bit in the sector's header is copied to the TRGR bit (bit 6) of the STATUS1 register.

The Go command and playback start-up

The Go on-line command signals the ZR36110 to commence playback of a bitstream. It is legal only when the device is idle, as indicated by the IDLE pin and status bit being active, and is the only valid command in the idle state. (The ZR36110 is in the idle state after a complete or partial initialization. It goes idle after decoding the end of an MPEG sequence, or after playback was aborted by the End Decoding command.)

Immediately after the Go command, the ZR36110 enters a start-up phase. The start-up procedure depends on the type of bitstream, and whether serial port output is enabled or not, but in all cases it begins with a search for a suitable start-up point; all data from the bitstream entry point (the first byte transferred after the Go command) to the start-up point is discarded. In the case of a system bitstream with video and audio streams, and an active serial port, the procedure includes the synchronization of the video with the audio.

Video-only bitstream

In the case of a video-only bitstream, if the VIDENT bit of the SYSMODE parameter is 1, the start-up point is the first sequence header encountered. If VIDENT is 0, the start-up point is the first sequence header or the first I-picture header, whichever comes first. When the start-up point is a sequence header, the horizontal and vertical sizes, picture rate and quantizer matrices are extracted from the sequence header and stored for use in the decoding.

When the start-up point is an I-picture header, the pictures will be decoded correctly only if the sequence header parameters stored from the previous sequence header are still valid. If they are not, a mechanism is provided to allow them to be specified by the host. To make use of that feature, the following 148 bytes of data must be transferred to the ZR36110 as the first part of the bitstream data:

Description	Size of data
000001FA	4 bytes
horizontal_size	12 bits
vertical_size	12 bits
picture_rate	1 byte
000001FA	4 bytes
intra_quantizer_matrix	64 bytes
non_intra_quantizer_matrix	64 bytes
horizontal_size	12 bits
vertical_size	12 bits
picture_rate	1 byte
reserved	4 bytes (zero bytes)

System bitstream

In the case of a system bitstream, the start-up point for an active audio or private1 bitstream is the first packet header which is preceded by at least one pack header and includes a PTS (presentation time stamp).The start-up point for an active private2 bitstream is the first packet header which is preceded by at least one pack header.

If the VIDENT bit of the SYSMODE parameter is 1, the start-up point of the active video stream is the first sequence header encountered, which is preceded by at least one PTS associated with this stream, which is in turn preceded by at least one pack header. If VIDENT is 0, the start-up point is the first sequence header or the first I-picture header of the active video stream, whichever comes first, and which is preceded by at least one PTS associated with this stream, which is in turn preceded by at least one pack header.

When the start-up point is a sequence header, the horizontal and vertical sizes, picture rate and quantizer matrices are extracted from the sequence header and stored for use in the decoding.

When the start-up point is an I-picture header, the pictures will be decoded correctly only if the sequence header parameters stored from the previous sequence header are still valid. If they are not, the mechanism described for the video-only bitstream should be used to provide the correct parameters.

Note: After the Go command, and before starting to decode the active video stream, the only legal mode change on-line commands are: Pause Stream, Continue and End Decoding, which only affect the audio or private streams if any of them started to be output from the serial port.

Once proper synchronization of audio and video has been achieved as described above, video decoding and serial port output proceed in lock-step, provided that the serial port bit rate parameter SP1BR or SP2BR is set to the correct value. Whenever there is a pause in playback as a result of an on-line command being executed, serial port output is paused and restarted in step with the pausing and restarting of the video decoding, and synchronization is maintained.

Serial port-only bitstream

In the case of a serial port-only bitstream, the start-up point is the first byte of the bitstream. There is no parsing or decoding of the bitstream by the ZR36110. Whatever data is transferred by the host is buffered in the audio bitstream buffer, and shortly after the data is first available in the buffer, serial port output commences.

Should the bitstream be designated an MPEG-1 coded audio stream by bit MPA of the EXTMODE parameter, the beginning of the bitstream is analyzed until the bit rate value is extracted, to be used for internal calculation of the clock divisors and ratios, if needed.

The ZR36110 plays back the serial port-only bitstream until it receives an End Decoding on-line command from the host. The only other legal mode change on-line commands in this case are Pause and Continue.

Playback termination and End Decoding command

In the absence of on-line commands, normal playback continues until the bitstream ends. Video decoding terminates when the last picture has been decoded and the sequence_end_code is decoded, serial port output stops when there is no more data to be output. The ZR36110 stops requesting a system bitstream when the iso_11172_end_code is decoded, and a video-only bitstream when the sequence_end_code is decoded. The IDLE signal and status register bit are activated after the last picture has been decoded and all decoded pictures have been displayed, and all serial port data has been output. After IDLE has been activated, the ZR36110 continuously displays the last picture or the background color, as determined by the LPIC bit of the SYSMODE set-up parameter.

Since no termination code is present in an audio-only bitstream, the ZR36110 must be put into the idle state by means of an End Decoding command.

The above behavior in response to the end codes applies equally when they are encountered while the ZR36110 is in the process of executing an on-line command.

The End Decoding command is used when it is desired to preemptively terminate playback and put the ZR36110 into the idle state. When executing the End Decoding command, the ZR36110 terminates decoding immediately, and activates IDLE after displaying the pictures that were decoded up to this point, according to the two l.s. bits of the command. After IDLE has been activated, it continuously displays the last picture or the background color, as determined by a field in the command code (described in the *On-Line Commands* section). This is illustrated in Figure 29, where a Freeze command and an End Decoding command are shown being executed at consecutive decoding start times.

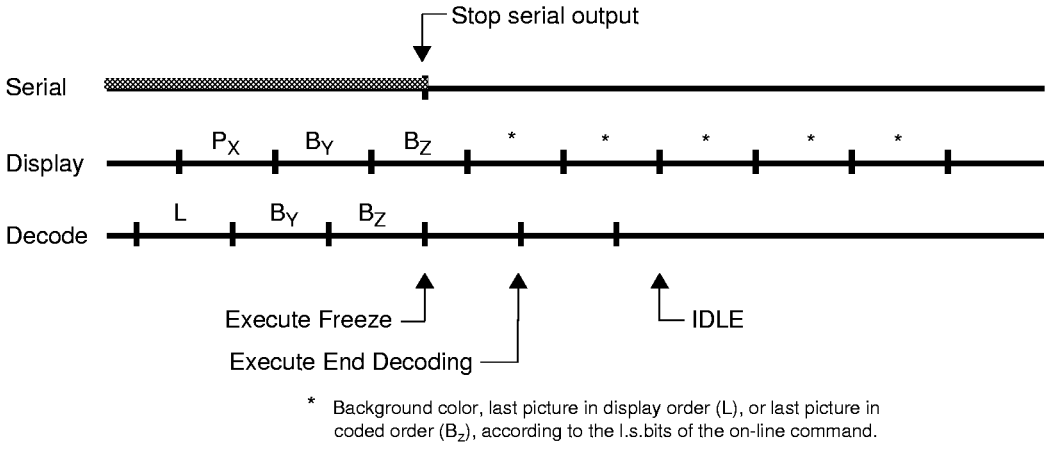


Figure 29. End Decoding

End Decoding on GOP

The End Decoding on GOP command is similar to the End Decoding command; upon receipt of an End Decoding on GOP command, the ZR36110 stops decoding, as if a video sequence end code was received after the last picture of the current GOP, followed (for system multiplexed bitstreams) by a 11172_end_code. This command should only be used if there is an active video stream; serial port-only playback can only be terminated by an End Decoding command.

The Pause, Single Step and Continue commands

The behavior of the ZR36110 when executing these commands is relatively self-explanatory. Figure 30 is an example, showing a Pause command, followed by two Single Steps and a Continue.

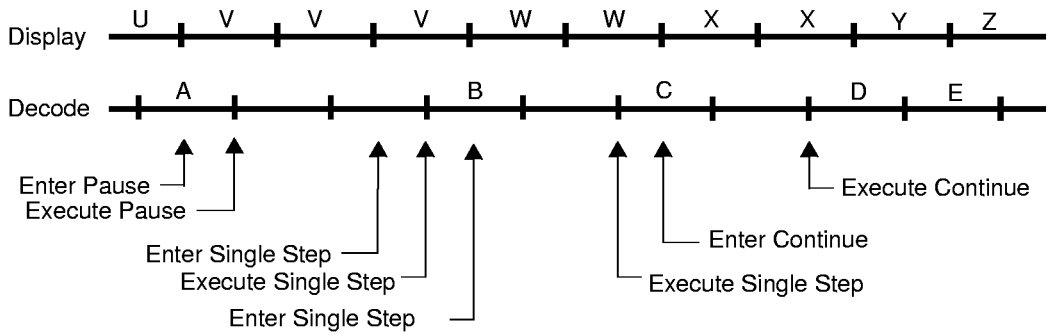


Figure 30. Pause, Single Step and Continue

The Decode-to-First-I-Picture command

The Decode-to-First-I-Picture command is entered when the ZR36110 is in normal playback mode, as illustrated in Figure 31. The ZR36110 continues decoding and displaying pictures until the next I-picture is displayed, regardless of the type of picture being displayed when the command was executed. It then pauses playback, and is ready to execute another command.

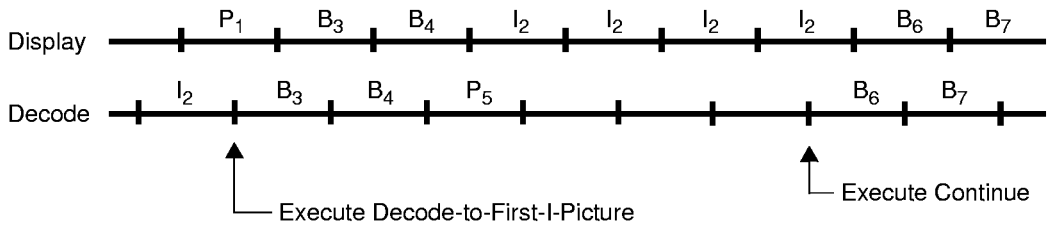


Figure 31. Decode-to-First-I-Picture

The Decode-to-Next-I-Picture command

The Decode-to-Next-I-Picture command performs a step to the next I-picture, while the currently displayed picture (the previous I-picture) remains unchanged. The display changes only when the new I-picture is displayed, as Figure 34 shows. In this example, it is assumed that the Decode-to-Next-I-Picture command was entered in place of the Continue command of the previous example.

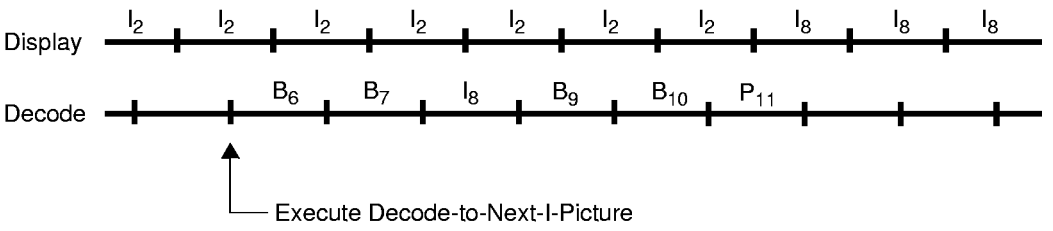
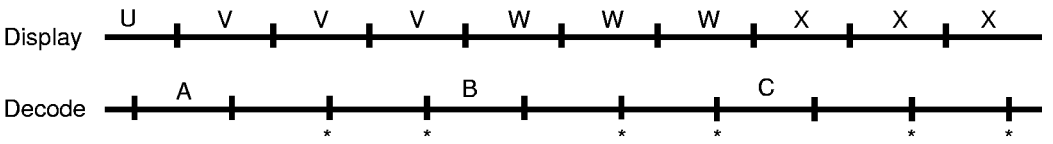


Figure 32. Decode-to-Next-I-Picture

The Slow Motion command

Execution of the Slow Motion command is a repeating sequence, each element of which entails decoding a single picture followed by a pause for the appropriate number of frame times. Slow Motion is anomalous in that it does not have a definite duration of execution like the other on-line commands. Consequently, whenever playback is paused, the command register is checked at every scheduled decoding time; only if there is no pending command will another iteration of the Slow Motion sequence be executed. An example of Slow Motion with slowdown factor of 3 is shown in Figure 33.



* Times at which the mode change on-line command register is checked for the pending command.

Figure 33. Slow Motion, with slowdown factor of 3

The Fast Search command

The Fast Search command causes the ZR36110 to discard picture coded data, as specified by the on-line command. The ZR36110 then stores coded video data (for the pictures which were not discarded) in the DRAM, along with any sequence and GOP headers and sequence_end_code (e.g., if bbb=2, the ZR36110 discards all B-pictures, and decodes and displays all I- and P-pictures). Meanwhile, the ZR36110 continues to decode and display the coded video data in the DRAM, as if in normal playback. In this way, the Fast Search command produces a “speed up” effect. The actual speed-up ratio and its stability depend on a number of factors: 1) the data transfer capacity of the host bus; 2) the arrangement of the pictures in the video sequence; and 3) and the size of the coded pictures.

Upon receipt of an End Decoding command, Fast Search is terminated. After the next external GO command, the ZR36110 reinitializes, as for random access. An example of the Fast Search command with a bbb (the 3 l.s. bits of the command) value of 3 (only I-pictures are decoded and displayed) is shown in Figure 34.

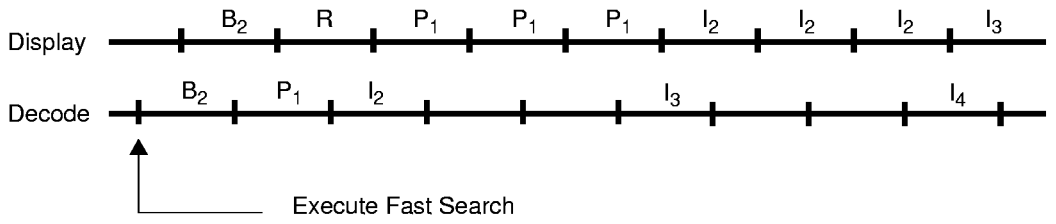


Figure 34. Fast Search

HIGH RESOLUTION STILL IMAGES

For decoding and display of high resolution still image sequences, the video interface of the ZR36110 must be configured for interlaced CCIR mode (the VSIZ bit of the VIDMODE set-up parameter should be reset to zero). After the Go command, the ZR36110 decodes and continuously displays one high resolution picture for each sequence, according to its time stamps. A new picture "waterfalls" into the previous picture.

When a bitstream of high resolution still pictures follows a bitstream of normal resolution pictures, or vice versa, the background color is displayed until the end of decoding of the first picture of the new bitstream.

If the HRS bit of the EXTMODE parameter is set, the FI_EN signal goes low when high resolution is signalled internally. The FI_EN signal goes high when the ZR36110 enters the Idle state.

Only one field of the decoded high resolution still picture is stored in the DRAM (in half high resolution format) if:

- The HHRS bit of the SYSMODE parameter is 1, OR
- The size of the decoded picture is CCIR-PAL, and the NBANK bit of the SYSMODE parameter is 0 (indicating one DRAM bank).

The stored field is output in both fields of the displayed frame.

FRAME RATE CONVERSION

The ZR36110 supports two frame rates, 25 and 29.97 fps (frames per second), as specified by the VIDS bit of the SYSMODE set-up parameter, and five picture rates, 23.976, 24, 25, 29.97, and 30 pps (pictures per second), as specified by the picture rate parameter in the sequence header of the video stream. When the picture rate and the frame rate are not the same, the ZR36110 performs frame rate conversion, from the specified picture rate to the specified frame rate. The 3/2 pulldown mechanism is used as needed.

Frame rate conversion is supported only when the video interface configuration is interlaced CCIR-size (when the VSIZ bit of VIDMODE is 0; see also the *Video Interface* section).

When the picture rate is 25 pps, the frame rate is 29.97 fps, and the height of the picture is more than 240 lines, $\overline{MB4}$ must be high and a -70 type DRAM is required.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -65°C to +150°C
Supply Voltage ..... -0.5V to +7.0V
DC Voltage Applied to outputs for High Impedance Output State ..... -0.5V to VCC +0.5V
DC Input Voltage ..... -0.5V to VCC + 0.5V
DC Output Current, into Outputs ..... 20mA/output, max 200mA
DC Input Current ..... -30mA to +5.0mA

Stresses above the values listed may cause permanent device failure.

OPERATING RANGE

Ambient Temperature ..... 0°C < Ta < 70°C
Supply Voltage ..... 4.75V < VCC < 5.25V

DC CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	Vcc + 0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA
I_{CC}	Power Supply Current		375 390	mA mA	@54.0 MHz, 5.25V @60.75 MHz, 5.25V
I_{SC}	Standby Current		50	mA	
I_{LI}	Input Leakage Current		±10	µA	0 < V_{IN} < Vcc
I_{LP}	Pull down Leakage Current		50	µA	0 < V_{IN} < Vcc
I_{LO}	Output Leakage Current		±10	µA	0 < V_{OUT} < Vcc
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O and Output Capacitance		10	pF	

AC CHARACTERISTICS

AC Characteristics over operating range

No.	Symbol	Parameter	Min.	Max.	Units	Test Conditions
General signals						
1	T_{GCP1}	GCLK Period ($\overline{MB4}$ low)	1000/15.18	1000/13.50	nsec	
1	T_{GCP2}	GCLK Period ($\overline{MB4}$ high)	1000/13.50	1000/12.00	nsec	
2	T_{GCH}	GCLK High	40	60	%	@2.0V
3	T_{GCL}	GCLK Low	40	60	%	@0.8V
4	T_{GCR}	GCLK Rise		3	nsec	0.8V to 2.0V
5	T_{GCF}	GCLK Fall		3	nsec	2.0V to 0.8V
7	T_{CRW}	Cold Reset Width	160 * T_{GCP}		nsec	
Video interface signals						
13	T_{VCP}	VCLK Period	1000/15.18	2000	nsec	
14	T_{VCH}	VCLK High	25		nsec	@2.0V
15	T_{VCL}	VCLK Low	25		nsec	@0.8V
16	T_{VCR}	VCLK Rise		3	nsec	0.8V to 2.0V
17	T_{VCF}	VCLK Fall		3	nsec	2.0V to 0.8V
18	T_{ISV}	Input setup	15		nsec	
19	T_{IHV}	Input Hold	0		nsec	
20	T_{ODV}	Output Delay	8	20	nsec	C_L = 50PF
Serial Port interface signals						
21	T_{SCP}	SPiCLK Period	280	200,000	nsec	
22	T_{SCH}	SPiCLK High	100		nsec	@2.0V
23	T_{SCL}	SPiCLK Low	100		nsec	@0.8V
24	T_{SCR}	SPiCLK Rise		5	nsec	0.8V to 2.0V
25	T_{SCF}	SPiCLK Fall		5	nsec	2.0V to 0.8V
28	T_{ODS}	Output Delay	8	50	nsec	C_L = 50PF
DRAM interface signals						
29	T_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay	3*PCLK-2		nsec	
30	T_{CAS}	$\overline{CAS}$ pulse width	2*PCLK-4	10000	nsec	
31	T_{CP}	$\overline{CAS}$ precharge time	PCLK-5		nsec	
32	T_{RP}	$\overline{RAS}$ precharge time	4*PCLK-5		nsec	
33	T_{ASC}	Column address setup time	PCLK-2		nsec	
34	T_{CAH}	Column address hold time	2*PCLK-5		nsec	

No.	Symbol	Parameter	Min.	Max.	Units	Test Conditions
35	T_{ASR}	Row address setup time	PCLK-2		nsec	
36	T_{RAH}	Row address hold time	PCLK-3		nsec	
37	T_{DS}	Data out setup time	PCLK-2		nsec	
38	T_{DH}	Data out hold time	2*PCLK-5		nsec	
39	T_{RAC}	Access from $\overline{RAS}$		80	nsec	
40	T_{AA}	Access from column address		40	nsec	
41	T_{RASP}	$\overline{RAS}$ pulse width	5*PCLK-3	10000	nsec	
42	T_{CSH}	$\overline{CAS}$ hold time	5*PCLK-2		nsec	
43	T_{PC}	cycle time	3*PCLK		nsec	
44	T_{RSH}	$\overline{RAS}$ hold time	2*PCLK-2		nsec	
45	T_{AR}	Column address hold to $\overline{RAS}$	4*PCLK-3		nsec	
46	T_{RHCP}	$\overline{RAS}$ hold time from $\overline{CAS}$	3*PCLK-3		nsec	
47	T_{OFF}	Data hold	0		nsec	
48	T_{RAD}	$\overline{RAS}$ to column add delay time	2*PCLK-5	25	nsec	
49	T_{RAL}	Column add to $\overline{RAS}$ lead time	3*PCLK-2		nsec	
Host bus interface signals						
50	T_{ISB}	Input set-up	10		nsec	
51	T_{IHB}	Input Hold	10		nsec	
52	T_{RWL}	Read/Write Low time	70		nsec	
53	T_{RWH}	Read/Write High time	PCLK+2 or 100 see note 1		nsec	
54	T_{DSB}	Data Input set-up	10		nsec	
55	T_{DHB}	Data Input Hold	5		nsec	
56	T_{DBD}	Data Bus Driven	1		nsec	C_L = 50PF
57	T_{DBV}	Data Bus Valid		50	nsec	C_L = 50PF
58	T_{DBY}	Data Bus Float Delay		10	nsec	C_L = 50PF
59	T_{WER}	Write to End of DREQ		50	nsec	
Video output in Enabled mode						
60	T_{ENS}	FI_EN setup to VCLK	20		nsec	
61	T_{VOD}	VIDOUT delay	8	20	nsec	
62	T_{VOF}	VIDOUT float	8	20	nsec	

1. The minimum value of T_{RWH} is PCLK+2ns from read to read, from write to write, or from read to write. From write to read, the minimum value of T_{RWH} is 100ns. PCLK here represents the period of PCLK.

General Signals

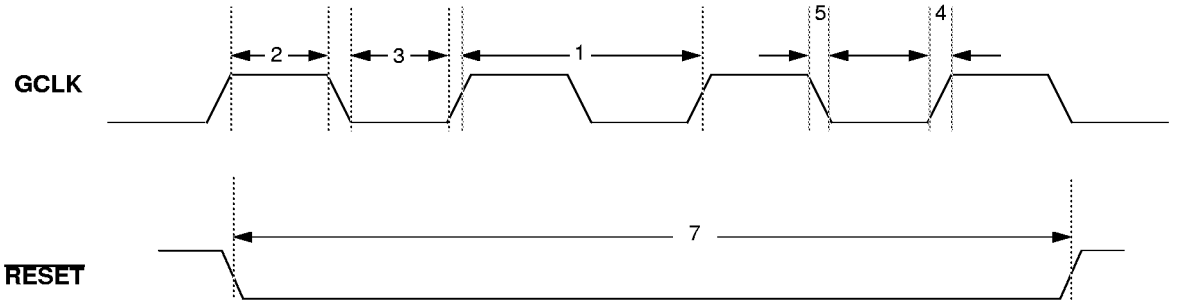


Figure 35. GCLK and $\overline{\text{RESET}}$ timing

Video Signals

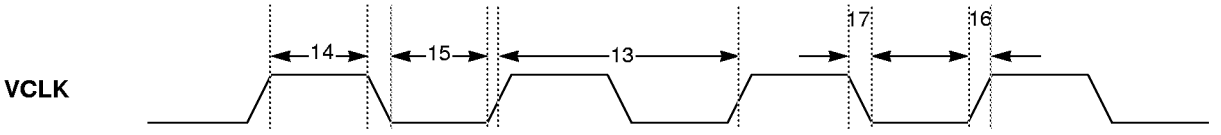


Figure 36. VCLK timing

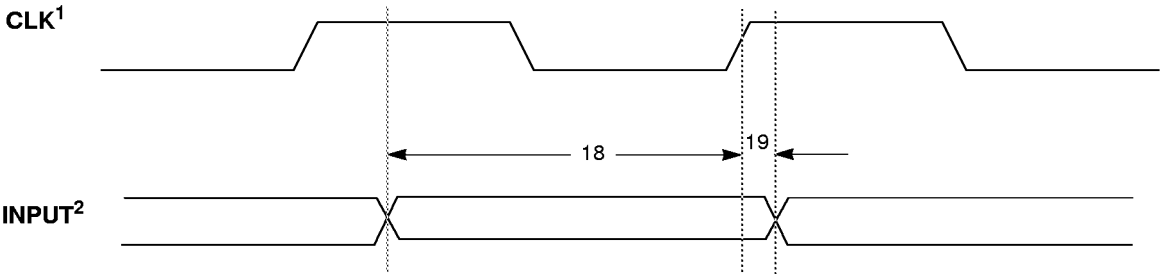


Figure 37. INPUT setup and hold timing

[1] VCLK (or QCLK_V if VCRS setup parameter is set)

[2] HSYNC, VSYNC and FI_EN; when these signals are inputs (the SDIR set-up parameter = 0)

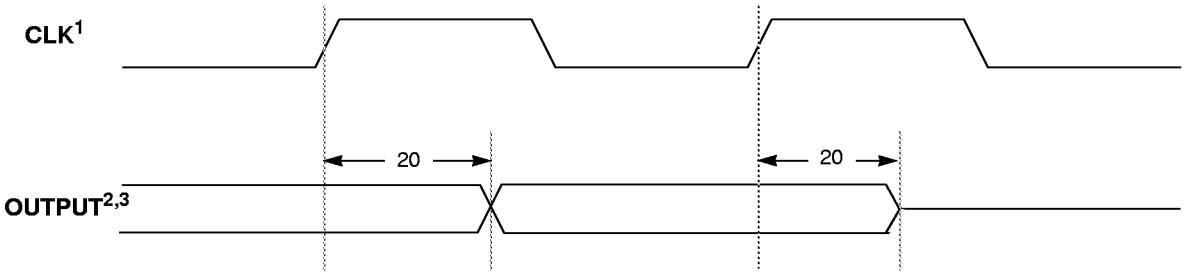


Figure 38. OUTPUT delay timing

[1] VCLK (or QCLK if VCRS setup parameter is set)
[2] HSYNC, VSYNC and FI_EN; when these signals are outputs (the SDIR set-up parameter = 1)
[3] VIDOUT

Serial Port Interface Signals

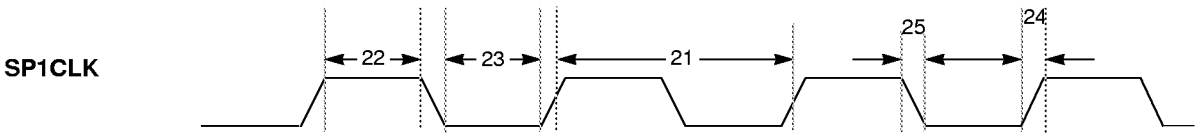


Figure 39. SP1CLK and SP2CLK timing
(SP2CLK has identical timing)

Note: Timing requirements are the same for either input or output SP1CLK

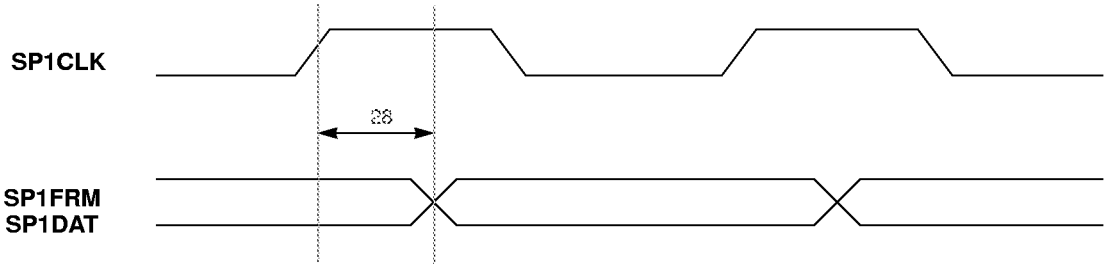


Figure 40. Serial Port 1 timing when SP1FRM is pulse type (timing is identical for serial port 2)

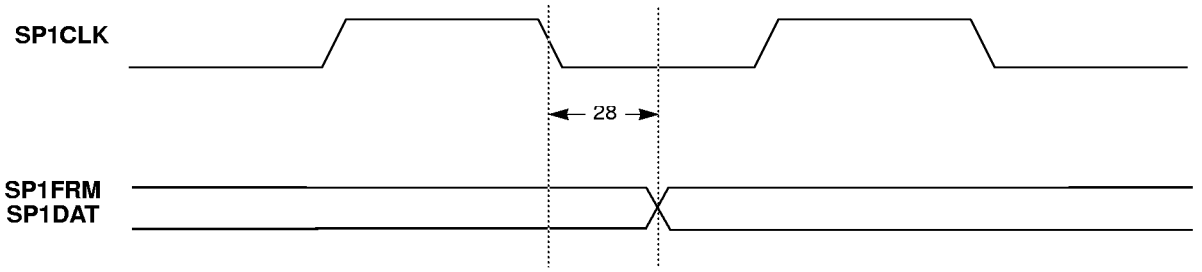


Figure 41. Serial port 1 timing when SP1FRM is transition or window type (timing is identical for serial port 2)

DRAM Interface Signals

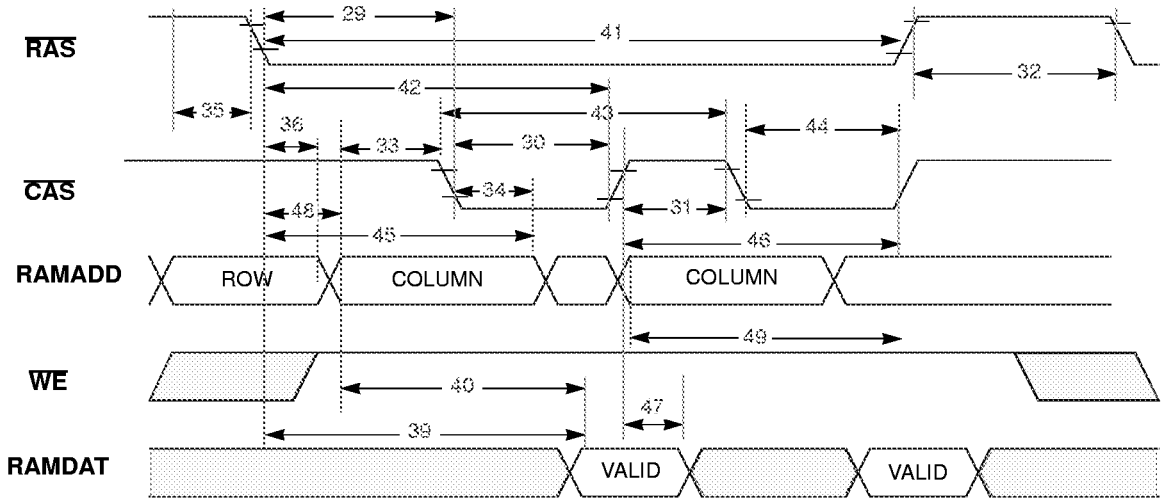


Figure 42. DRAM Fast Page Mode Read timing

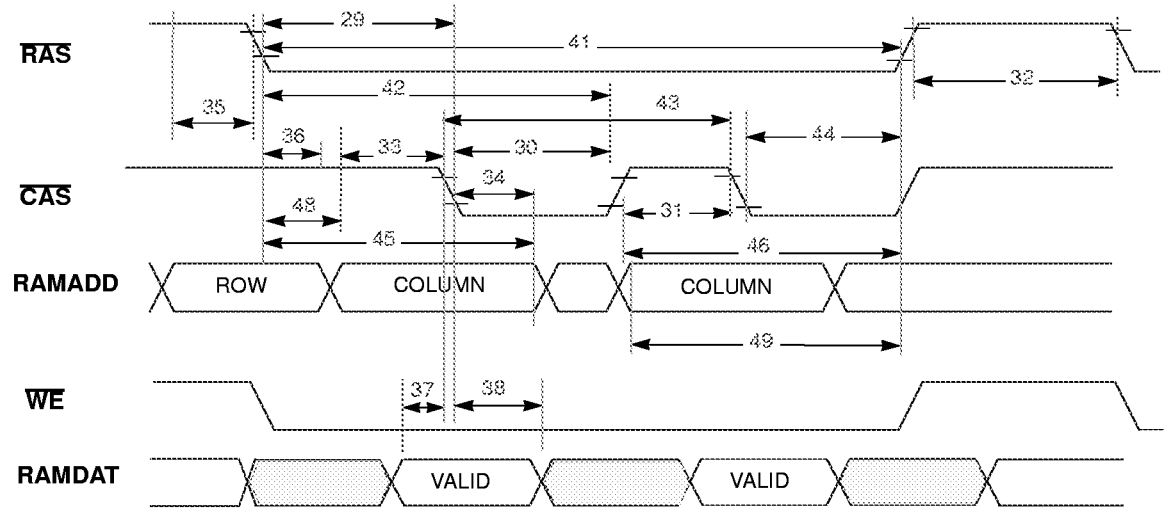


Figure 43. DRAM Fast Page Mode Write timing

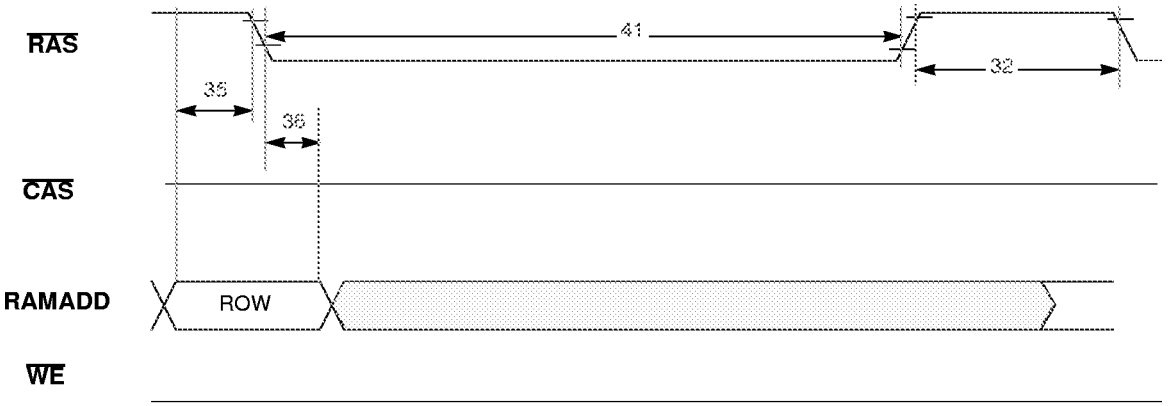


Figure 44. DRAM refresh cycle timing (RAS-only)

Host Bus Interface

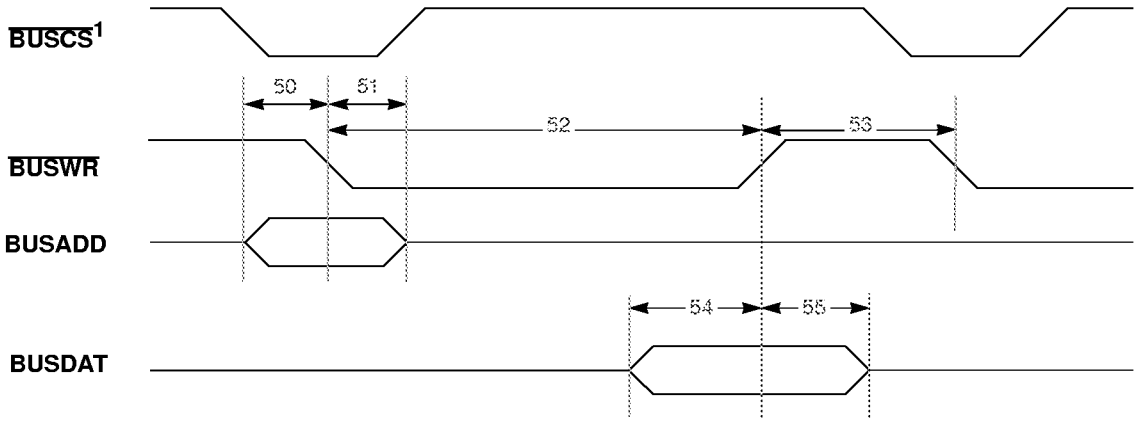


Figure 45. I/O Write timing

[1] BUSCS can remain active for multiple I/O write cycles

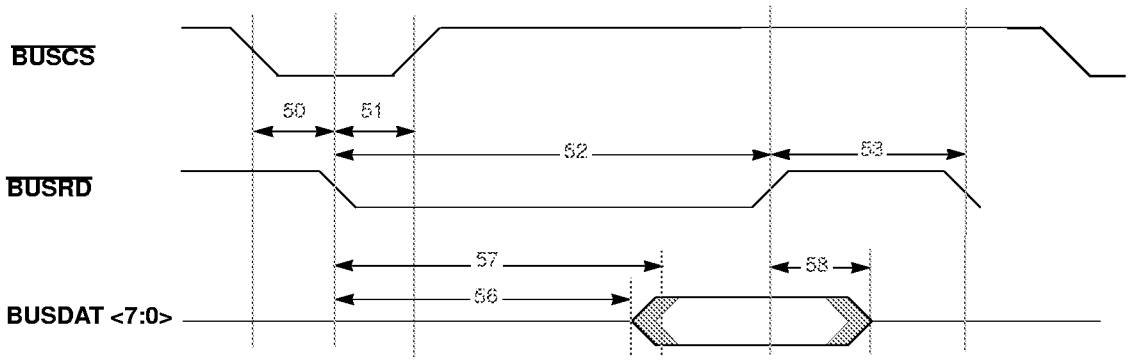


Figure 46. I/O Read timing
BUSDAT <15:8> remain at high Impedance

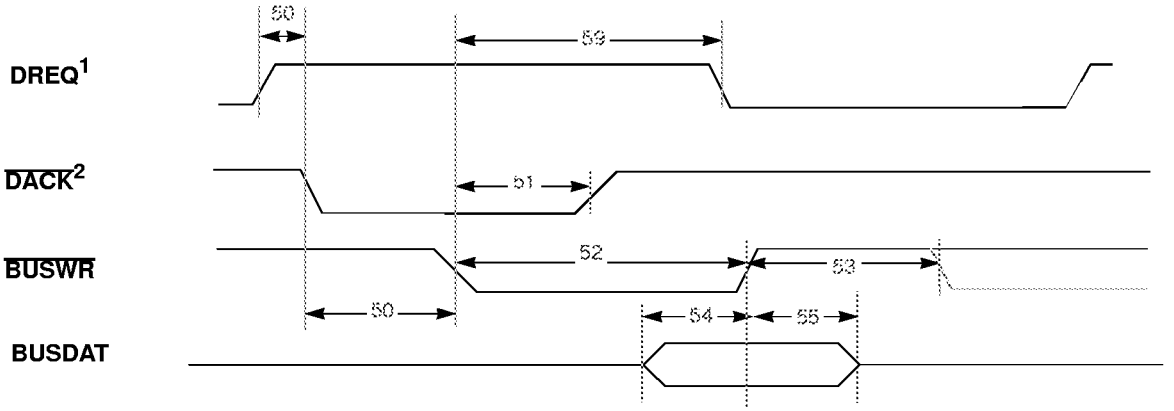


Figure 47. DMA timing (for BSLN=1)

[1] DREQ will remain active for BSLN transfer cycles
[2] $\overline{\text{DACK}}$ can remain active for BSLN transfer cycles, or can be pulsed for each transfer cycle

Video Output in Enabled Mode

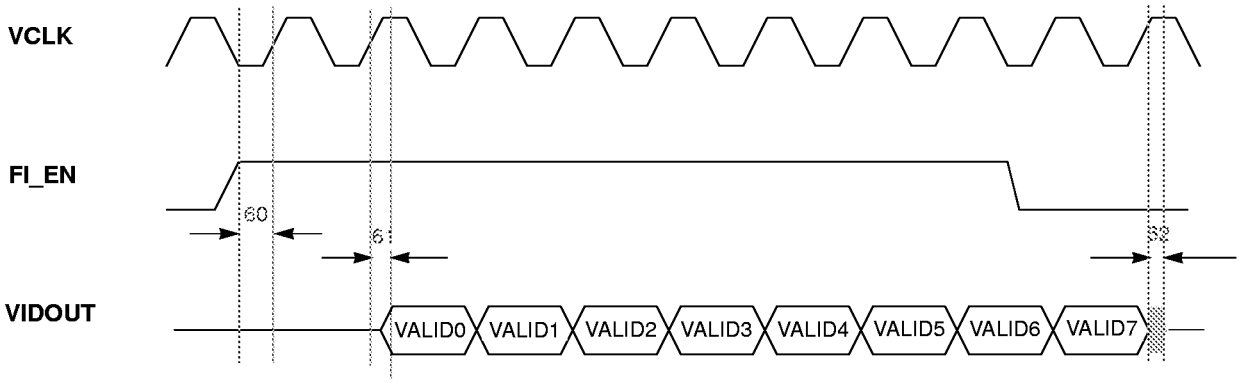


Figure 48. Video output in Enabled Mode

AC TEST CONDITIONS

During AC testing, inputs are driven at 0.4V and 2.4V levels. Input to output switching times are measured from the 1.5V level of the input to the 1.5V level at the output. Pulse widths and clock periods are measured between the 1.5V level of one output and 1.5V level of the other output.

Normal test load during AC testing is 50 pF.

Figure 49. AC Test Reference Levels

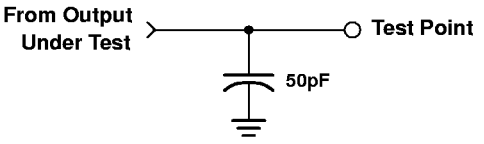


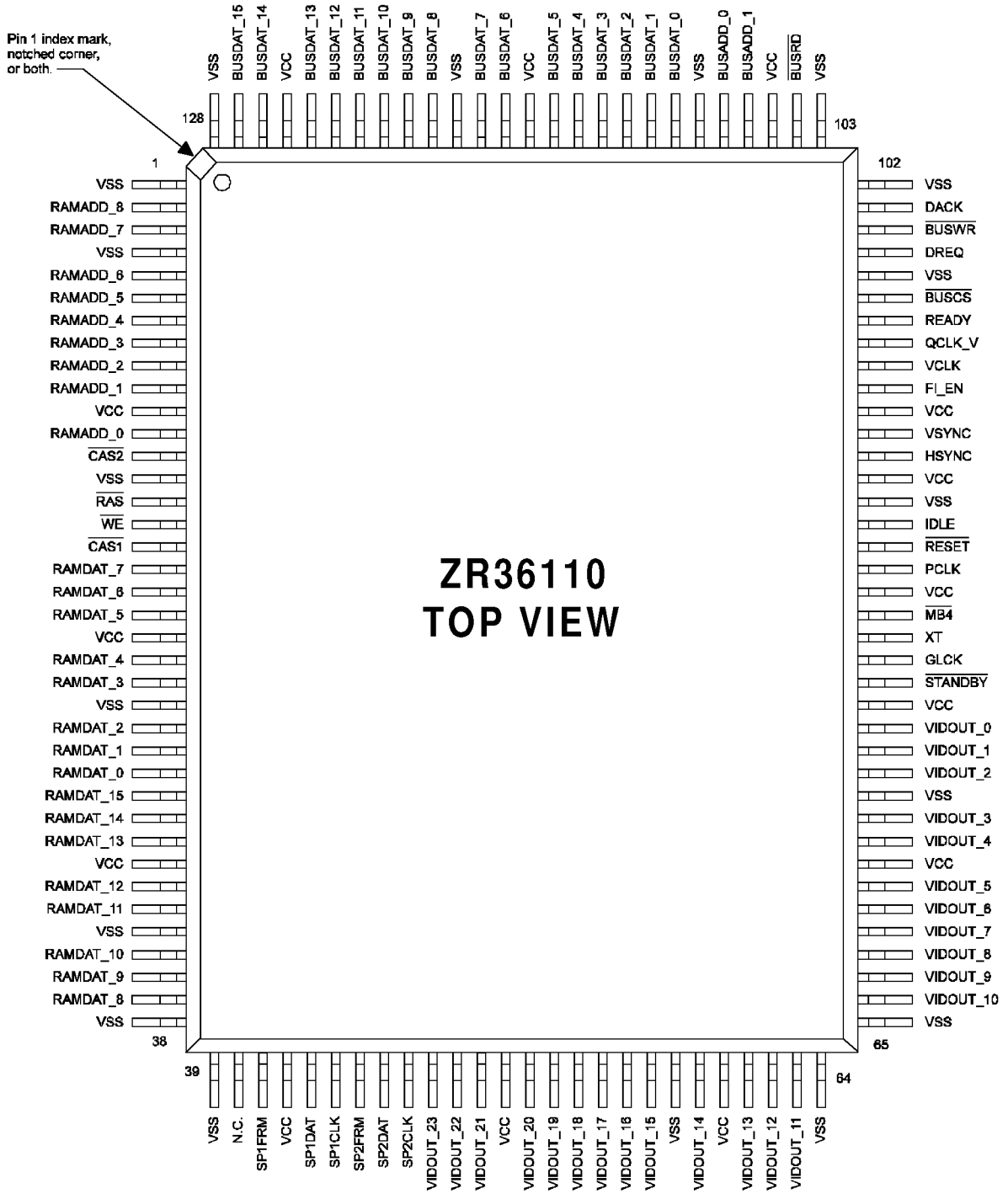
Figure 50. Normal AC Test Load

PINOUT INFORMATION

Table 19. 128-Pin QFP pin assignment

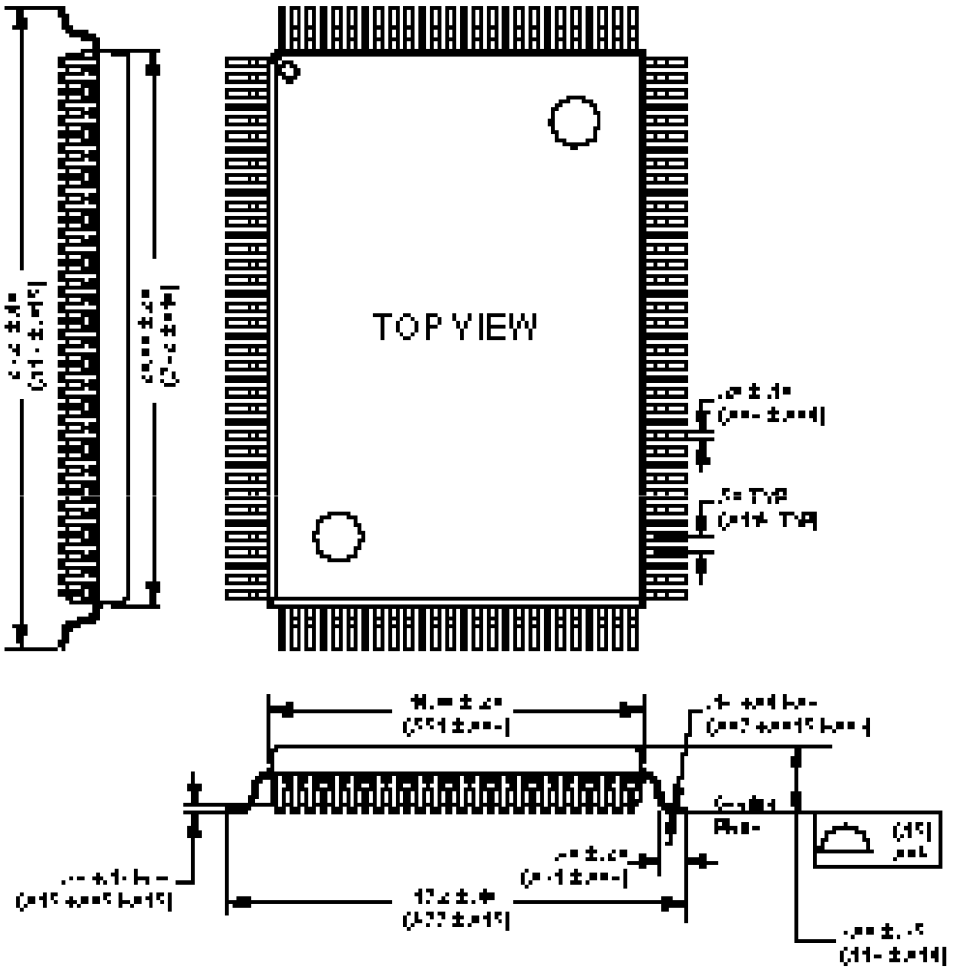
Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type	Pin No	Pin Name	Type
1	VSS	S	27	RAMDAT_0	B	53	VIDOUT_19	O	79	VCC	S	105	VCC	S
2	RAMADD_8	O	28	RAMDAT_15	B	54	VIDOUT_18	O	80	STDBY	I	106	BUSADD_1	I
3	RAMADD_7	O	29	RAMDAT_14	B	55	VIDOUT_17	O	81	GCLK	I	107	BUSADD_0	I
4	VSS	S	30	RAMDAT_13	B	56	VIDOUT_16	O	82	XT	O	108	VSS	S
5	RAMADD_6	O	31	VCC	S	57	VIDOUT_15	O	83	MB4	I	109	BUSDAT_0	I/B
6	RAMADD_5	O	32	RAMDAT_12	B	58	VSS	S	84	VSS	S	110	BUSDAT_1	I/B
7	RAMADD_4	O	33	RAMDAT_11	B	59	VIDOUT_14	O	85	PCLK	O	111	BUSDAT_2	I/B
8	RAMADD_3	O	34	VSS	S	60	VCC	S	86	RESET	I	112	BUSDAT_3	I/B
9	RAMADD_2	O	35	RAMDAT_10	B	61	VIDOUT_13	O	87	IDLE	O	113	BUSDAT_4	I/B
10	RAMADD_1	O	36	RAMDAT_9	B	62	VIDOUT_12	O	88	VSS	S	114	BUSDAT_5	I/B
11	VCC	S	37	RAMDAT_8	B	63	VIDOUT_11	O	89	VCC	S	115	VCC	S
12	RAMADD_0	O	38	VSS	S	64	VSS	S	90	HSYNC	B	116	BUSDAT_6	I/B
13	CAS2	O	39	VSS	S	65	VSS	S	91	VSYNC	B	117	BUSDAT_7	I/B
14	VSS	S	40	N.C.	-	66	VIDOUT_10	O	92	VCC	S	118	VSS	S
15	RAS	O	41	SP1FRM	O	67	VIDOUT_9	O	93	FI_EN	B	119	BUSDAT_8	I/B
16	WE	O	42	VCC	S	68	VIDOUT_8	O	94	VCLK	I	120	BUSDAT_9	I/B
17	CAS1	O	43	SP1DAT	O	69	VIDOUT_7	O	95	QCLK_V	O	121	BUSDAT_10	I/B
18	RAMDAT_7	B	44	SP1CLK	B	70	VIDOUT_6	O	96	READY	O	122	BUSDAT_11	I/B
19	RAMDAT_6	B	45	SP2FRM	O	71	VIDOUT_5	O	97	BUSCS	I	123	BUSDAT_12	I/B
20	RAMDAT_5	B	46	SP2DAT	O	72	VCC	S	98	VSS	S	124	BUSDAT_13	I/B
21	VCC	S	47	SP2CLK	B	73	VIDOUT_4	O	99	DREQ	O	125	VCC	S
22	RAMDAT_4	B	48	VIDOUT_23	O	74	VIDOUT_3	O	100	BUSWR	I	126	BUSDAT_14	I/B
23	RAMDAT_3	B	49	VIDOUT_22	O	75	VSS	S	101	DACK	I	127	BUSDAT_15	I/B
24	VSS	S	50	VIDOUT_21	O	76	VIDOUT_2	O	102	VSS	S	128	VSS	S
25	RAMDAT_2	B	51	VCC	S	77	VIDOUT_1	O	103	VSS	S			
26	RAMDAT_1	B	52	VIDOUT_20	O	78	VIDOUT_0	O	104	BUSRD	I			

Note: I = Input, O = Output, S = Supply, B = Bidirectional



NOTE: Pins identified as “N.C.” must remain completely unconnected.

PACKAGE DIMENSIONS



NOTE: Principal dimensions in millimeters, dimensions in brackets in inches.