ZR36506 USBVision

The One Chip Solution for Multi-Mode Digital Cameras

Datasheet

February 2001

Zoran Proprietary and Confidential

Rev. 1.0

Zoran reserves the right to make changes without further notice to any product herein. Zoran makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Zoran assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Zoran products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Zoran product could create a situation where personal injury or death may occur.

Table of Contents

1 INTRODUCTION

ZR36506 - Multi-mode Digital Camera Chip

Zoran's USBvision ZR36506 is a revolutionary, multi-mode digital camera chip offering integrated live digital video and audio capture functionality.

Powered by an integrated microprocessor, the chip's high level of versatility facilitates the design and implementation of multi-function digital cameras. The ZR36506 supports on-line operation (over USB, wireless or any other, non-USB connections), for such applications as live audio/video streaming and surveillance, as well as standalone applications, such as digital still cameras with audio recording capabilities.

For applications requiring alternative digital video connection schemes (wireless connections, surveillance cameras or devices lacking USB support), the ZR36506 may be integrated into camera designs built around a serial interface for transferring images, audio clips and compressed video.

Support for OEM Customizations

Zoran supplies a full reference design kit, software A/V streaming WDM driver which is Microsoft DirectShow compatible, digital camera TWAIN drivers and software API support for the ZR36506 FLASH memory – transfer and management (preview, deletion, photo album creation). The API reference kit contains header and library files, as well as sample programs demonstrating their use. Device drivers may easily be renamed (OEM USB vendor and product IDs may be programmed via a .INF file) to reflect different OEM branding schemes.

Features and Benefits

On-Line (USB, Serial, Wireless) Mode

Applications: video conferencing, live video capture and editing, video gaming and surveillance.

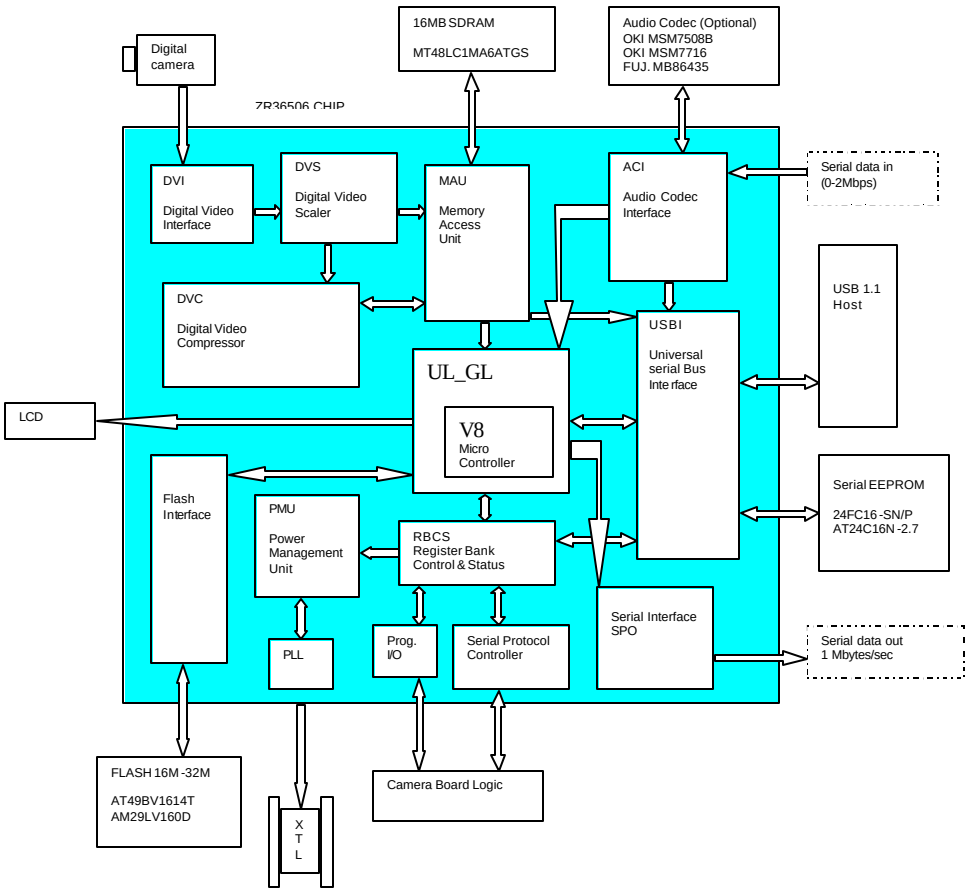
- **Full-motion, full-color video**
  Up to 30 frames per second at CIF (352 x 288) resolution; up to 15 frames per second at VGA (640 x 480) resolution. Live video may be streamed over serial connections (either wireless or wired) at up to 1 Mbyte/sec. Software controlled digital pan and zoom. Support for raw and compressed video at variable compression ratios (over USB or non-USB connections).
- **Simultaneous video and stereo audio capture**
  Full compatibility with Microsoft DirectShow WDM streaming and popular video conferencing and video editing software applications.
- **VGA (640 x 480) resolution TWAIN compatible still image capture**
  TWAIN compatibility for live still image capture and for control over digital camera flash memory: preview, transfer or erase pictures.
- **Easy Plug-and-Play operation**
  Video camera configuration is stored in external EEPROM. Powered by USB port, with adjustable USB bandwidth utilization (0.5 – 7.5 Mb/sec).

Off-Line (Standalone) Mode

Applications: digital still image and audio capture.

- **Easy digital image and audio clip capture anywhere**
  Pictures and audio clips are stored on the camera's flash memory and may be transferred to a computer or PDA via USB, wireless or other connections. An audio clip may be recorded for each picture via an integrated microphone.
- **Large storage capacity**
  Up to 4 Megabytes of flash memory accommodate up to 120 pictures at 320 x 240 QVGA, or up to 30 images at high quality, VGA resolution.
- **Built-in hardware interfaces and support for still digital camera applications**
  Built-in support for camera Capture and Function buttons. Support for two 7-segment LCD displays to indicate camera mode or status, and the number of stored images. Low power consumption and an Auto Power Off feature extend battery life.
- **Easy firmware upgradeabilty**
  Microprocessor code updates and expansions may easily be performed via the ZR36506's integrated EEPROM.

Product Description



ZR36506 Internal Block Diagram

The ZR36506 utilizes a single USB port to enable the host computer to access 4 different data channels simultaneously. These 4 channels are the Digital Video input (7.5 Mbit/sec), Digital Audio input, Serial Bulk Data input, and I/O control (internal registers, programmable I/O pins and selectable Data/Clock serial protocols).

Due to the sophisticated architecture and protocol of the USB interface, the software application is not required to handle time-sharing management of several tasks using a single serial bus. This is handled by lower-level drivers, so that the application program can access each function of the ZR36506 independently.

In normal operation, the ZR36506 performs following tasks:

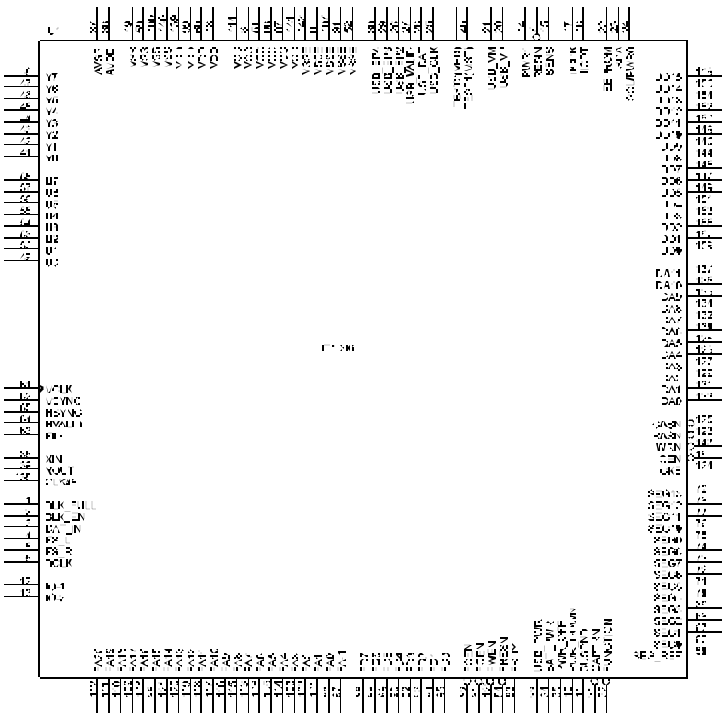
Compressed Video Channel

The ZR36506 connects to a Y/U/V digital video source, scales the image horizontally and vertically on the fly, compresses the data down to 0.5-7.5 Mbit/sec, and sends it to the host computer via the USB port. The ZR36506 scaler supports zoom-in-like effects by applying combinations of built-in zooming and cropping functions. This unique compression method is proprietary to Zoran and allows fast and easy software-only decompression.
The decompression software driver supplied with the ZR36506 will accept compressed data and convert it back to standard video formats in less time than it would take to read raw video from any external port. Still images may be captured and sent via USB in the best quality and resolution that the camera can provide.

- **Sound System**
  Some camera applications require that a microphone sound system be implemented inside the camera. Additionally, composite-video to USB adapter applications require audio recording support. The ZR36506 provides a solution for these applications by multiplexing serial digital audio input with video data that is sent via the USB port. The microphone can be located inside the camera, up to 5 meters away from the host computer. The ZR36506 does not include the audio A/D, and is designed to use an external low-cost telephony audio codec.

- **Camera Control**
  Camera (or any video source) control and status monitoring can be carried out via a built-in serial interface or direct I/O pins. The serial interface supports some common serial protocols. Control and monitoring software for other remote devices may use these ports as well. In a video conference application, this feature allows the local or remote user to set the focus, zoom and other parameters of the camera, and even switch the camera's power off. The ZR36506 also supports usage of an external capture button that is mounted on the camera board and is used for capturing video frames to the host computer hard disk (this is application dependent - the ZR36506 only delivers the capture command signaling from button to host computer via USB).

2 ZR36506 PINOUT



Pin Descriptions

Pin Number	Signal	I/O	Description
18, 60, 99, 139	VDD		2.5 V supply (for core logic).
8, 51, 87, 96, 114, 141	VCC		3.3 V supply (for I/O pins).
36	AVDD		2.5 V Analog supply for internal PLL.
19, 59, 100, 140	VSS		Digital ground connections (for core).
9, 52, 91, 107, 142	VSSE		Digital ground connections (for I/O pins).
37	AVSS		Analog ground for internal PLL.
41 – 48	Y0-Y7	I	Video Luminance input from camera. The VCLK input is used to sample the bus. Each input pin features an internal Pull-Down resistor.
49 – 50, 53 – 58	U0-U7	I	Video Chroma U or U/V-components input from camera. The VCLK input is used to sample this bus. Each input pin features an internal Pull-Down

Pin Number	Signal	I/O	Description
			resistor.
40	TEST1 (MST)	I	This pin must be connected to GND.
61	VCLK	I	Video Pixel-Clock input from camera
64	HVALID	I	Video Clock Enable input qualifier. This input pin should be connected to GND if not used.
62	VSYNC	I	Video Vertical-Sync input signal from camera. This input pin should be connected to GND if not used.
65	HSYNC	I	Video Horizontal-Sync input signal from camera. This input pin should be connected to GND if not used.
63	FID	I	Video Field-ID input signal from camera. This input pin should be connected to GND if not used.
12 – 13	IO-1 - IO-2	I/O	General Programmable I/O pins. Each of these 2 pins has an Open Drain, and is supposed to be connected to an external Pull-Up resistor. The host uses these pins as programmable output ports by writing '0' or '1'. By writing '1' and read back, the host can use these pins' input ports - as this allows any external source to force the Pull-Up resistor. These outputs are temporarily set to High-z while in Suspend mode.
38	XIN	I	Crystal Oscillator input pin (12 MHz). Crystal frequency must provide at least 100 PPM accuracy.
39	XOUT	O	Crystal Oscillator output pin (12 MHz).
1	BLK_FULL	O	"Bulk-FIFO full" indication output signal. This output signal is normally '0' and is set to '1' when the ZR36506 Bulk-FIFO is full. This output is temporarily set to '0' while in the Suspend or Power-Down position.
2	BLK_EN	I	Bulk Data Enable input. When set to '1', Bulk input data from the DAT_IN pin is sampled in by falling edge of BCLK into the ZR36506 Bulk-FIFO.
3	DAT_IN	I	Data Input pin for both Audio CODEC Tx channel and Bulk Data in. This input pin requires an external Pull-Up resistor.
4	FS_L	O	Audio Codec Frame-Sync pulse for Left channel. This signal triggers the beginning of a new audio sample (left chan). This output is temporarily set to '0' while in the Suspend or Power-Down position.
5	FS_R	O	Audio Codec Frame-Sync pulse for Right channel. This signal triggers the beginning of a new audio

Pin Number	Signal	I/O	Description
			sample (right chan). This output is temporarily set to '0' while in the Suspend or Power-Down position.
6	BCLK	O	Main Clock for both Audio CODEC and Bulk Data in. This output is temporarily set to '0' while in the Suspend or Power-Down position.
138	CLK48	O	48 MHz Clock output for SDRAM interface. This output is set to '0' while in Suspend or Power-Down modes.
159, 157, 155, 153, 151, 149, 147, 145, 144, 146, 148, 150, 152, 154, 156, 158	DD0-DD15	I/O	SDRAM Data bus input/output pins. These pins feature internal Pull-Down resistors, and are set to High-z while in Suspend or Power-Down modes.
125	CASN	O	SDRAM Column Address Select Active low. This output is set to High-z while in Suspend or Power-Down modes.
143	WRN	O	SDRAM Write Enable Active low. This output is set to High-z while in Suspend or Power-Down modes.
160	CSN	O	SDRAM Chip Select Active low. This output is set to High-z while in Suspend or Power-Down modes.
123	RASN	O	SDRAM Row Address Select Active low. This output is set to High-z while in Suspend or Power-Down mode.
133, 131, 129, 127, 126, 128, 130, 132, 134, 136, 135, 137	DA0-DA11	O	SDRAM Row/Column Address-bus. These outputs are set to '0' while in Suspend or Power-Down modes.
124	CKE	O	SDRAM Clock Enable. Active high, enable clock for SDRAM.
24	SCL/PWR0	I/O	Serial EEPROM clock signal, and LSbit of Device Power Code. If an EEPROM is detected, this pin is used as the EEPROM clock output signal; otherwise its voltage (Vdd or GND) is used as the LSbit of the Device Power Code for the USB Device Descriptor. If EEPROM is detected, this pin is temporarily set to '1' while in the Suspend position.
22	EEPROM	I	EEPROM Detect pin. If EEPROM is used, a 10 KΩ Pull-Up resistor to Vdd should be connected to this pin. Otherwise, it should be tied to GND.
23	SDA	I/O	Serial EEPROM data signal. High-z in Suspend and Power-Down modes.

Pin Number	Signal	I/O	Description
14	PWR1	I	MSbit of Device Power Code. The voltage level in this input (Vdd or GND) is used by the ZR36506 as the MSbit of the Device Power Code for the USB Device Descriptor. If an external EEPROM exists, this input is ignored.
7	RESIN	I	Power-On Reset input. This input is of Schmitt-Trigger type, and is active low. It is recommended to use a power-on RC network for proper Reset.
15	SENS	O	Serial control Enable Signaling. This pin has an Open Drain output. It should be connected to an external 3.3-10 KΩ Pull-Up resistor. This output is set to High-z while in Suspend or Power-Down modes.
16	IICDT	I/O	Camera-Control Data I/O (supports some commonly used serial protocols). This pin has an Open Drain output. It should be connected to an external 3.3-10 KΩ Pull-Up resistor. This output is temporarily set to High-z while in the Suspend or Power-Down position.
17	IICCK	O	Camera-Control Clock output (supports some commonly used serial protocols). This pin has an Open Drain output. It should be connected to an external 3.3-10 KΩ Pull-Up resistor. This output is temporarily set to High-z while in the Suspend or Power-Down position.
10	PWR_DWN	O	Camera Power-Down control. This is an Open Drain output, which is used to switch power On or Off to the camera and/or external circuit (using an external switching P-MOSFET transistor). While in Reset, the output is set to High-z (Off). It is set to High-z in Suspend mode, and remains High-z when resuming from Suspend.
11	SUSPND	O	USB Suspend mode control. This is an Open Drain output. A Power-On Reset or a USB-Reset turn the output to active low It is set to High-z in Suspend mode, and is turned to active low when Resuming from Suspend.
31	CAPTRN	I	Capture Button input. A Schmitt-Trigger input with an internal Pull-Up resistor When forced to '0', the host computer is automatically informed that a video frame capture was requested by the user.

Pin Number	Signal	I/O	Description
20	USB_VP	I/O	Universal-Serial-Bus Positive data line. This line should be connected to an external Pull-Up resistor of 1.5 KΩ. Refer to Electrical Characteristics table for pin spec. This pin is kept High-z while in the Suspend position.
21	USB_VM	I/O	Universal-Serial-Bus Negative data line. Refer to Electrical Characteristics table for pin spec. This pin is kept High-z while in the Suspend position.

Flash Memory

Pin Number	Signal	I/O	Description
97-98, 101-106, 113, 115-121, 85, 108-112	FA-1-FA20	O	Flash memory Address Bus. Can address up to 4 Mbytes. Set to '0' logic in Power-Down and Suspend modes.
95, 94, 93, 92, 90, 89, 88, 86	FD0-FD7	I/O	Flash memory Data Bus. Features internal Pull-Down resistors. High-z in Power-Down and Suspend modes.
82	FCEN	O	Flash memory Chip Enable. Active LOW. '0' logic in Power-Down and Suspend modes.
81	FOEN	O	Flash memory Output Enable. Active LOW. '0' logic in Power-Down and Suspend modes.
112	FWEN	O	Flash memory Write Enable. Active LOW. '0' logic in Power-Down and Suspend modes.
84	FRESN	O	Flash memory Reset. Active LOW. '0' logic in Power-Down and Suspend modes.
83	FRDY	I	Flash Ready input (used to indicate end of Write or Erase operations).

Power Management

Pin Number	Signal	I/O	Description
33	USB_PWR	I	'1' logic indicates that power comes from USB port. This input is sampled a few milliseconds after power-on or Reset operation.
34	BAT_PWR	I	'1' indicates that power comes from Battery. This input is sampled a few milliseconds after power-on or Reset operation.

Pin Number	Signal	I/O	Description
35	PWR_OFF	O	Auto-Power-Off indication output pin. A negative pulse on this output is used to turn-off the battery supply. It is '0' logic in Power-Down and Suspend modes.

LCD Control, Functional Button, General Purpose Pins

Pin Number	Signal	I/O	Description
66-79	SEG0-SEG13	O	Driving two 7-segment LCDs. '0' in Power-Down and Suspend modes.
80	SEG_REF	O	A Reference pin, driving two 7-segment LCDs. '0' in Power-Down and Suspend modes.
32	FUNCTION	I	Function Button input. A Schmitt-Trigger input with an internal Pull-Up resistor It is used for the Stand alone Digital Still Camera MMI.

SPO Pins

Pin Number	Signal	I/O	Description
25	USB_CLK	O	Serial Data Clock. Data is valid on Up-going edge. '0' in Power-Down and Suspend modes. Used in non USB Stand alone mode.
26	USB_DAT	O	Serial Data signal. '0' in Power-Down and Suspend modes.
27	USB_VALID	O	Serial Data Valid. Data is valid when USB_VALID='1'. '0' in Power-Down and Suspend modes.
28	USB_EP2	O	EP2 (Video) transaction indicator. '0' in Power-Down and Suspend modes.
29	USB_EP3	O	EP3 (Audio) transaction indicator. '0' in Power-Down and Suspend modes.
30	USB_EP4	O	EP4 (Bulk) transaction indicator. '0' in Power-Down and Suspend modes. Not valid in Non USB Stand alone mode.

Absolute Maximum Ratings (Voltages Referenced to GND)

Rating	Symbol	Value	Unit
Core DC Supply Voltage	V_{dd} - GND	-0.5 to 2.5	V
I/O DC Supply Voltage	V_{cc} - GND	-0.5 to +3.3	V
Voltage, any pin to GND	V	-0.5 to V_{cc}+0.5	V
DC Current Drain per Pin (Excluding V_{dd}, GND)	I	±20	mA
Junction Temperature Range	T_J	-40 to +125	^{o}C
Storage Temperature Range (plastic package)	T_{stg}	-40 to +125	^{o}C

Electrical Characteristics (V_{CC} = 3.3 V, T_A = 0 to 70^{o}C)

Characteristic	Symbol	Min	Type	Max	Unit
Core DC Supply Voltage (V_{dd} to GND)	V_{dd}	2.25	2.5	2.75	V
I/O DC Supply Voltage (Vcc to GND)	V_{cc}	3.0	3.3	3.6	V
Core DC Supply Current (@ V_{dd}=2.5 V)	I_{dd}	52	53.16	54	mA
I/O DC Supply Current (@ V_{dd}=3.3 V)	I_{CC}	12.36	12.49	12.6	mA
Suspend mode Current (@ V_{dd}=3.3 V)	$I^{Suspend}$	-	-	200	µA
High Level Input Voltage	V_{IH}	0.7xV_{cc}	-	V_{dd}+0.3	V
Low Level Input Voltage	V_{IL}	-0.3	-	0.3xV_{cc}	V
Input Current V_I = V_{cc}+0.3 or GND	I_{in}	-10	+1	+10	µA
Input Capacitance	C_{in}	-	5	16	pF
3-State Output Leakage Current V_O = V_{cc}+0.3 or GND	I_{OZ}	-10	+1	+10	µA
Output Capacitance	C_{out}	-	5	16	pF
High Level Output Voltage (@ Ioh = 0.8 mA)	V_{OH}	V_{cc}-0.1	-	-	V
Low Level Output Voltage (@ Iol = 0.8 mA)	V_{OL}	0	-	0.1	V
Pull-Up / Pull-Down Resistance	R_{PU}	25	50	200	KΩ

USB_VP/VM Pins Electrical Characteristics (V_{CC}=3.3 V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Type	Max	Unit
High-z State Data Line Leakage (@ 0<Vin<3.3 V)	I_{LO}	-10	-	+10	µA
Differential Input Sensitivity	V_{DI}	0.2	-	-	V
Differential Common Mode Range	V_{CM}	0.8	-	2.5	V
Single Ended Receiver Threshold	V_{SE}	0.8	-	2.0	V
Static Output Low (@ 1.5 KΩ Pull-Up resistor to 3.6 V)	V_{OL}	-	-	0.3	V
Static Output High (@ 15 KΩ Pull-Down resistor to GND)	V_{OH}	2.8	-	3.6	V
Capacitance	C_{IN}	-	-	20	pF
Rise Time (@ C_L =50 pF)	T_R	4	-	20	nS
Fall Time (@ C_L =50 pF)	T_F	4	-	20	nS
Driver Output Resistance (@ external serial 24 Ω resistor)	Z_{DRV}	28	-	43	Ω

Video Parameter Specifications

Parameter	Symbol	Value	Unit
Digital Video Input Format (1)	Y/U/V	-	-
Down Scaling (V/H independent and arbitrary)	-	Up to 16:1 vertical and horizontal	-
Horizontal Anti Aliasing Filter (2)	-	2-5 taps	-
Vertical Anti Aliasing Filter (2)	-	2-3 taps	-
Interpolation Phase Resolution	-	360°/4	-
Image Cropping (V/H independent and arbitrary)	-	Any window of length 1 to full image	-
Video Compression Ratio	Cr	1-8	-
Video Compressor Clock Frequency	-	48.000	MHz
Compressed Video Bit Rate	-	0.5 to 7.5 Mbit/sec	-

- **Refer to Video Channel chapter for specification of digital video input modes and waveforms.**
- **Filter uses interpolation process.**

USB Interface Parameter Specifications

Parameter	Value	Unit	USB Pipe mode
USB Maximum Data Rate	12	Mbit/sec	-
Compressed Video Maximum Data Rate	7.5	Mbit/sec	Isochronous
I/O channel Rate Capacity	0-16	Kbit/sec	Control & Bulk

I/O channel uses transactions of up to 8 bytes per package.

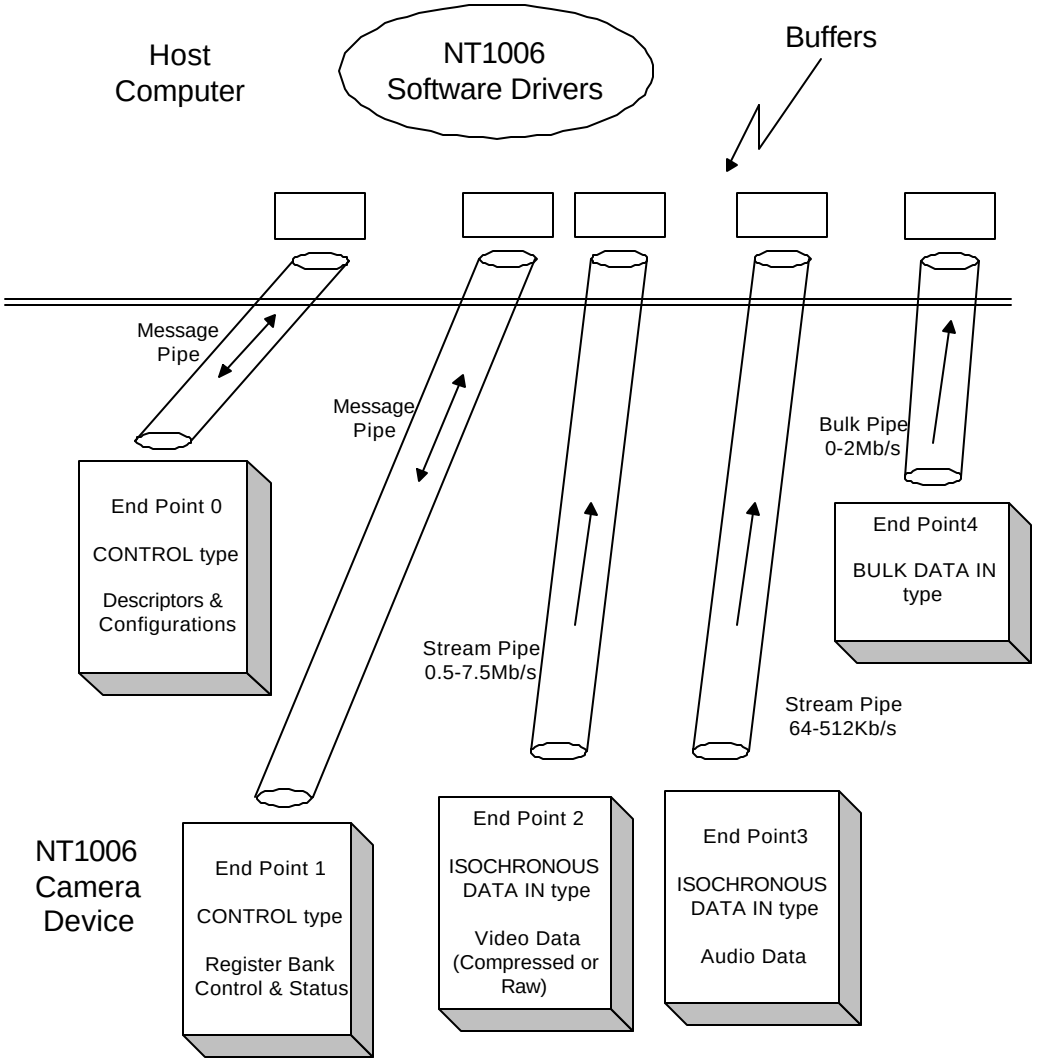
Audio Parameter Specifications

Parameter	Symbol	Value	Unit
Digital Audio Sampling Rate	Fs	8.0/16.0 ± 0.25%	KHz
Audio channel Bit Rate	-	64-512 Kb/sec µ-Law or A-Law	-
Audio CODEC clock frequency		1.536, 2.048	MHz

Audio CODEC clock frequency is programmable to either 1.536 or 2.048 MHz.

3 GENERAL ARCHITECTURE

The following diagram describes the general architecture of the ZR36506, regarding it as a standard USB device:



The ZR36506 has 5 USB End-Points located on chip:

- End-Point #0: This is the Descriptors and Configuration End-Point, which is required by the USB standard.
- End-Point #1: This is the control end-point used to access the Register Bank. The host computer uses these registers to control the ZR36506 and the camera.
- End-Point #2: This End-Point produces and sends the digital video data to the host computer. It uses 0.5 to 7.5 Mbit/s of the USB bandwidth, depending on the amount of bandwidth available to the camera.
- End-Point #3: This End-Point sends the input digital audio data to the host computer. It uses 64 to 512 Kbit/s of the USB bandwidth, depending on the audio quantization and sampling rate.
- End-Point #4: This End-Point sends the external Bulk Data input to the host computer. It uses 0 to 2 Mbit/s of the USB bandwidth, depending on the external source of data.

The ZR36506 has a default set of USB Descriptors on-chip, which are automatically used in absence of an external serial EEPROM (otherwise, all descriptors are read from the EEPROM). The default descriptors allow the host computer to select one of 4 different configurations to operate the camera.

Camera manufacturers may define new configurations (which combine only the available End-Points), using the 8-pin serial EEPROM. Additionally, string descriptors may be added (in multiple languages) to define such parameters as the camera vendor's name, product name, serial number, etc. The USB standard regards these features as optional.

The ZR36506 supports the USB Power-Management-Protocol. The camera and external circuits may be power-controlled by their vendor-specific software drivers, via serial Data/Clock and I/O ports. The PWR_DWN output pin may also be used to turn off the local power supply to these external circuits (refer to ZR36506 application notes). The ZR36506 uses a single 12 MHz crystal to derive all of its internal clock sources. Power management also involves switching of internal clock sources, which are not in use in certain modes of operation. This further reduces the device’s power consumption.

The ZR36506 has two sources of Reset control: The Power-On-Reset that comes from a dedicated input pin (RESIN), and the USB-Reset command received from the host computer. Both Reset sources produce a single Reset signal inside the ZR36506, which initializes the ZR36506. It is assumed that a Power-On-Reset is applied to the RESIN pin before any USB transaction is sent to the ZR36506 by the host. This is required so that the Serial-Interface-Engine inside the ZR36506 be able to receive any valid host command that will follow (including a USB-Reset command).

The total USB bandwidth that is consumed by the ZR36506 is mainly affected by the bandwidth of the Video Data Stream (End-Point #2). To prevent a host computer, which initially has little available bandwidth, from rejecting the camera device, the ZR36506 uses the Alternate-Interface mechanism to enable variable bandwidth. This allows the host computer to select the highest bit-rate that it can reserve for the video stream, starting from 7.5 Mbit/s down to 0.5 Mbit/s in 0.5 MHz increments (the selected bit-rate affects video quality).

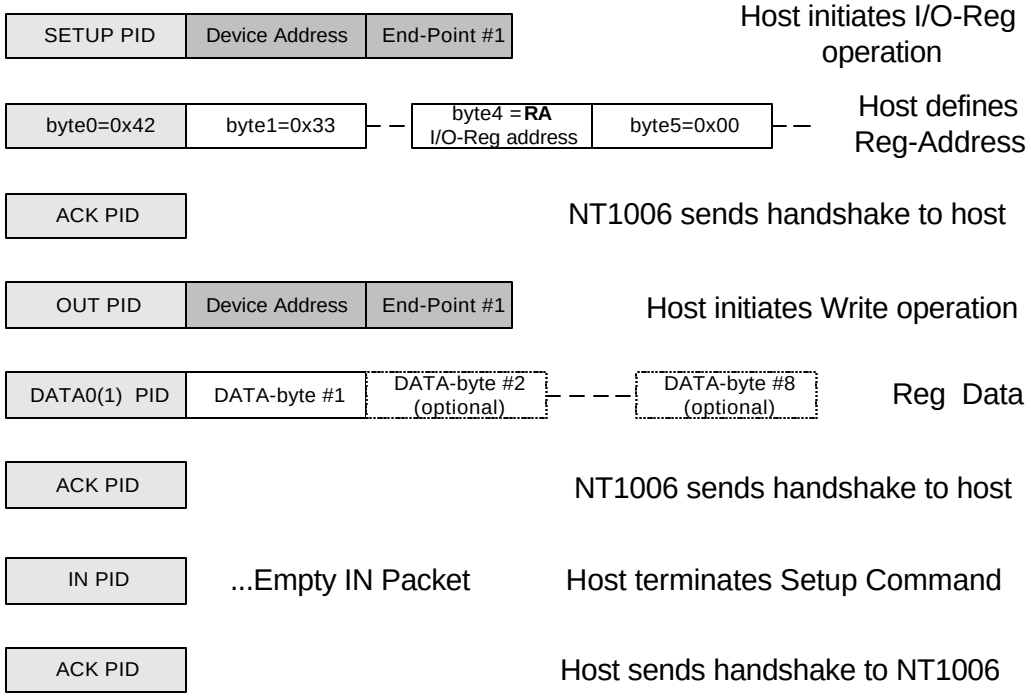
When the ZR36506 is used as a Digital Still Camera in Standalone mode, the internal microcontroller controls the chip. This includes camera initialization, setting camera control parameters that are stored in the serial EEPROM, capturing of still images and audio into Flash memory.

4 REGISTER BANK (CONTROL AND STATUS)

The ZR36506 uses the End-Point #1 message pipe for ZR36506 and camera control. As a bi-directional pipe, this channel allows the host computer to write contents to control registers, as well as to read status registers. Control registers may also be read by the host computer to check their contents. All registers are byte-oriented.

The following section defines a USB vendor-specific protocol for read and write operations applied to the ZR36506 register bank. This protocol uses a standard USB request of a vendor-specific type (defined in chapter 9.3 of USB standard rev.1.1) to perform a data transfer of up to 8 bytes to/from End-Point #1. A single write operation will write 1-8 concurrent bytes to the register bank, and a single read operation will read 1-8 concurrent bytes from the register bank. The USB Request Command always defines the address of the first I/O-register to be read or write. This address is automatically incremented by the ZR36506 for the following data bytes. The first byte of the USB Request Command defines the direction of the data transfer (0x42 for write, and 0xC2 for read). The second byte is an ZR36506-specific code - 0x33. The address of the first I/O-register in the list is defined by the wIndex parameter of the standard USB Request Command (these are bytes 4 and 5 of the command). All other bytes in the Request Command are not important to the ZR36506.

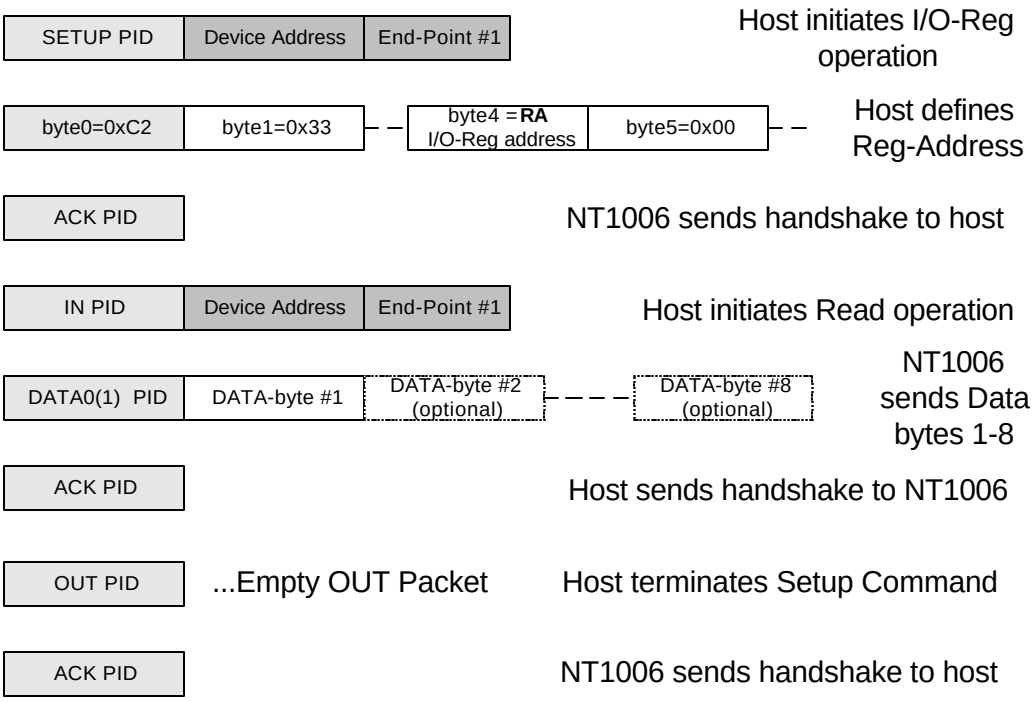
Write Transaction Protocol



The following table specifies the addresses to which the ZR36506 stores each of the bytes that appear in the data-section of the USB OUT transaction. These addresses relate to the contents of the **wIndex** parameter (bytes 4 and 5 of the SETUP command), which is denoted here by **RA**.

DATA Byte #	Contents	Description
1	Out Data	Will be stored in register at address RA.
2	Out Data	Optional. Will be stored in register at address RA+1.
3	Out Data	Optional. Will be stored in register at address RA+2.
4	Out Data	Optional. Will be stored in register at address RA+3.
5	Out Data	Optional. Will be stored in register at address RA+4.
6	Out Data	Optional. Will be stored in register at address RA+5.
7	Out Data	Optional. Will be stored in register at address RA+6.
8	Out Data	Optional. Will be stored in register at address RA+7.

Read Transaction Protocol



DATA Byte #	Contents	Description
1	Register Data	Byte read from register at address RA.
2	Register Data	Optional. Byte read from register at address RA+1.
3	Register Data	Optional. Byte read from register at address RA+2.
4	Register Data	Optional. Byte read from register at address RA+3.
5	Register Data	Optional. Byte read from register at address RA+4.
6	Register Data	Optional. Byte read from register at address RA+5.
7	Register Data	Optional. Byte read from register at address RA+6.
8	Register Data	Optional. Byte read from register at address RA+7.

Reading from an address that does not exist is legal, but will return unpredicted data.

The following tables specify all control and status registers in the ZR36506. A brief description is provided for every specific bit in these registers, and default values (after a Reset operation) are defined. For more details about a specific register, consult the appropriate session in this data sheet.

Register Address	Register Name	Function	Default Value
0	PWR_REG	d0: WD_EN: '1' Enables USB Watch-Dog timer. d1: SSPND_EN: '0' Enables Suspend-Resume logic. d2: RES2: '0' Restarts End-Point #2 logic, '1' Releases. d3: CLK48_EN: '1' Enables 48 MHz at CLK48 output pin. d4: reserved, should be '0'. d5: PWR_VID: '1' Video-logic Power-On. d6: reserved. d7: E2_EN: '1' Enables EEPROM R/W.	00H
1	CONFIG_REG	d7-d0: Configuration (set via USB). Read-Only reg.	00H

Register Address	Register Name	Function	Default Value
2	ADRS_REG	d6-d0: Device Address (set via USB). Read-Only reg. d7: '0'. reserved.	00H
3	ALTER_REG	d3-d0: Video Bandwidth (set via USB). Read-Only reg. d7-d4: '0000'. reserved.	00H
4	FORCE_ALTER_REG	d3-d0: NEW_ALT Forced Video Bandwidth. R/W reg. d7: FORCE_ALT ('1'=force, '0'=ignore). d6-d4: '000'. reserved.	00H
5	STATUS_REG	d0: VFRM_BLNK Vertical Blank (if '1'). Read-Only reg. d7-d1: '0000000'. reserved.	00H
6	IOPIN_REG	d0: IO_1 Read/Write level of ZR36506 pin IO-1. d1: IO_2 Read/Write level of ZR36506 pin IO-2. d7-d4: TEST[3..0], must be '0000' for proper operation. d3-d2: '00'. Reserved.	00H

Register Address	Register Name	Function	Default Value
7	SER_MODE	d6-d4: MODE (Soft, IICC, Cam1, Cam2). d7: Auto Bulk. '1' – Enable Bulk. '0' – Disable Bulk. **Normal operation (when not in Soft mode):** d0: CLK_RATE ('0' = 93.75 KHz, '1' =1.5 MHz). d1: CLK_POL ('0' = Normal, '1' = Inverted). d2: Must be '0' for proper operation. d3: VSYNC ('1' = wait to new input video field). **Soft mode:** d0: CLK_OUT (functional in Soft mode only). d1: DAT_IO (functional in Soft mode only). d2: SENS_OUT (functional in Soft mode only).	00H
8	SER_ADRS	d7-d0: Address of serial device/camera-param.	00H
9	SER_CONT	d2-d0: SER_LEN Number of bytes to Wr/Rd. d3: SER_DIR ('0' = Wr, '1' = Rd). d4: SER_GO/SER_BUSY. d5: NACK_RCV (Read-Only. '1' means Not Ack.). d6: CONTINUE (Do not send START signal next time). d7: NO_STOP (Do not send STOP signal this time).	00H
10	SER_DAT1	d7-d0: 1st serial byte to be sent/received.	00H
11	SER_DAT2	d7-d0: 2nd serial byte to be sent/received.	00H
12	SER_DAT3	d7-d0: 3rd serial byte to be sent/received.	00H
13	SER_DAT4	d7-d0: 4th serial byte to be sent/received.	00H

EEPROM Read / Write Registers

Register Address	Register Name	Function	Default Value
14	EE_DATA	d7-d0: EEPROM byte to be Written/Read.	00H
15	EE_LSBAD	d7-d0: 8-LSbits of byte address in EEPROM.	00H
16	EE_CONT	d2-d0: 3-MSbits of byte address in EEPROM. d3: EE_DIR ('0' = Write, '1' = Read). d4: EE_GO/EE_BUSY. d7-d5: EE_CLK_FORCE (This field is Read-Only)	00H or xxx0000 (when no EPROM)

SDRAM and Memory Buffer Setup Registers

Register Address	Register Name	Function	Default Value
18	DRM_CONT	d0: REF ('0' = 8.2 ms, refresh rate). d1: Enable operation of SDRAM. The bit SDRAM_EN is Reset to '0' by Reset, Suspend or Power-Down events. User should write '1' to enable SDRAM after these events, allowing for at least 100 uSec after Power-Up. d2: RES_UR Restart video out buffer read logic. d3: RES_FDL Restart video-frame-delay logic. d4: RES_VDW Restart video out buffer write logic. d5-d7: reserved.	00H
19	DRM_PRM1	d0-d3: Bits 19-16 of FDL_LST_WORD. d4-d7: reserved.	00H
20	DRM_PRM2	d0-d3: Bits 11-8 of FDL_1ST_ROW. d4-d7: reserved.	00H
21	DRM_PRM3	d0-d3: Bits 11-8 of VDW_LST_ROW. d4-d7: Bits 11-8 of VDW_1ST_ROW.	00H
22	DRM_PRM4	d7-d0: Bits 7-0 of FDL_1ST_ROW parameter.	00H
23	DRM_PRM5	d7-d0: Bits 7-0 of FDL_LST_WORD parameter.	00H
24	DRM_PRM6	d7-d0: Bits 15-8 of FDL_LST_WORD parameter.	00H
25	DRM_PRM7	d7-d0: Bits 7-0 of VDW_1ST_ROW parameter.	00H

26	DRM_PRM8	d7-d0: Bits 7-0 of VDW_LST_ROW parameter.	00H

Video Setup and Control Registers

Register Address	Register Name	Function	Default Value
27	VIN_REG1	d2-d0: VIN_MODE Digital video input format. d3: VSNC_POL Vertical-Sync. Pulse polarity. d4: HSNC_POL Horizontal-Sync. Pulse polarity. d5: FID_POL Field Identity signal polarity. d6: HVALID_POL Pixel Envelope polarity. d7: VCLK_POL ('1'=data valid on up-going clock).	00H
28	VIN_REG2	d0: AUTO_FID Auto Field Identity generation. When set to '1', the ZR36506 ignores the FID input from camera, and generates an internal toggling signal of its own instead. d1: NONE_INTERLACE Interlace/Non-Interlace mode. If set to '1', all input fields from the camera are processed, otherwise odd fields are ignored. d2: NO_HVALID If set to '1', HVALID input ignored. d3: UV_ID If set to '1', use V7 pin as UV-id ('1'=U). d4: FIX_2C If set to '1', U7 & V7 are inverted (2's comp). d5: SEND_FID- If set to '1', Frame_Phase[0]=FID. d6: '0' reserved. d7: KEEP_BLANK - Set to '1' to drop incoming frames.	00H
29	LXSIZE_IN	d7-d0: bits 7-0 of input video line length.	00H
30	MXSIZE_IN	d1-d0: bits 9-8 of input video line length. d7-d2: '000000' reserved.	00H
31	LYSIZE_IN	d7-d0: bits 7-0 of input video number of lines.	00H

Register Address	Register Name	Function	Default Value
32	MYSIZE_IN	d1-d0: bits 9-8 of input video number of lines. d7-d2: '000000' reserved.	00H
33	LX_OFFST	d7-d0: bits 7-0 of input video horizontal offset.	00H
34	MX_OFFST	d1-d0: bits 9-8 of input video horizontal offset. d7-d2: '000000' reserved.	00H
35	LY_OFFST	d7-d0: bits 7-0 of input video vertical offset.	00H
36	MY_OFFST	d1-d0: bits 9-8 of input video vertical offset. d7-d2: '000000' reserved.	00H
37	FRM_RATE	d4-d0: Frame-Rate factor Numerator for video data output. d6-d5: Frame-Rate factor Denumerator code: '00': 32, '01': 30, '10': 25. d7: '0' reserved.	00H
38	LXSIZE_O	d7-d0: bits 7-0 of output video line length.	00H
39	MXSIZE_O	d1-d0: bits 9-8 of output video line length. d7-d2: '000000' reserved.	00H
40	LYSIZE_O	d7-d0: bits 7-0 of output video number of lines.	00H
41	MYSIZE_O	d1-d0: bits 9-8 of output video number of lines. d7-d2: '000000' reserved.	00H
42	FILT_CONT	d2-d0: XFILT_CONT Horizontal-Filter select. d4-d3: YFILT_CONT Vertical-Filter select. d7-d5: '000' reserved.	00H
43	VO_MODE	d5-d0 Digital Video-Out format (4:2:2, 4:2:0, compression). d6: ('1' = Compressed Video, '0' = Raw). d7: '0' reserved.	00H
44	INTRA_CYC	d7-d0: Intra-Compression cycle (in frame units).	00H
45	STRIP_SZ	d3-d0: ACT_STRIP Actual Strip width (# of video lines). d7-d4: VIRT_STRIP Virtual Strip width (# of video lines).	00H

Register Address	Register Name	Function	Default Value
46	FORCE_INTRA	d0: ('1' = Force next frame Intra). d7-d4: MIN_DENUM[3..0]. d3-d1: '000' reserved.	00H
47	FORCE_UP	d0: ('1' = Force Up-mode Intra segments). d7-d1: STRIP_DAT_LIMIT[6..0].	00H
48	BUF_THR	d7-d0: Threshold for buffer space Frame-Drop decision (given in units of 2 KB).	00H
49	DVI_YUV	d2-d0: Code for YUV re-order processor. d4-d3: BUF_THR[9..8]. Extension for 16 Mbit SDRAM. d6: SLOW_CLK12 '1' Select 12 MHz for Horizontal blank. d7: SLOW_CLK16 '1' Select 16 MHz for Horizontal blank. d5: '0' reserved.	00H

Audio & Bulk-Data Port Read / Write Registers

Register Address	Register Name	Function	Default Value
50	AUDIO_CONT	d0: E_A - Enable Audio channel ('1' enables, '0' disables). d1: E_B - Enable Bulk-Data port ('1' enables, '0' disables). d3-d2: BPS - bits/samp: 00: 8b, 01: 12b, 10: 14b, 11: 16 b. d4: S/M - Select Stereo/Mono '0': Mono. '1': Stereo. d5: FS - Audio Sampling Rate '0': 8 Ks/sec. '1': 16 Ks/sec. d7-d6: BK - Bit-Clk Freq 1: 64 [KHz]. 2: 1544 [KHz]. 3: 2048 [KHz].	00H
51	AUD_PK_LEN	d7-d0: Max. number of bytes in Audio packet	00H

		(0 to 128).	
52	BLK_PK_LEN	d6-d0: Max. number of bytes in Bulk packet (0 to 64). d7: '0' reserved.	00H

USB Watch-Dog Register

Register Address	Register Name	Function	Default Value
53	WD_COUNT	d7-d0: USB_frame Watch-Dog delay parameter. A value 0x00 produces a 686 micro-seconds delay. A value of 0xE9 produces a 996 micro-seconds delay. Any value between these two values affects the delay in steps of 1.33 micro-seconds. Values higher than 0xE9 have no effect.	00H

Compression Ratio Management Registers

Register Address	Register Name	Function	Default Value
56	PCM_THR1	d7-d0: PCM Threshold 1 (unsigned 0-255).	00H
57	PCM_THR2	d7-d0: PCM Threshold 2 (unsigned 0-255).	00H
58	DIST_THR_I	d7-d0: DIST_THR_I (Distortion. Threshold for Inter).	00H
59	DIST_THR_A	d7-d0: DIST_THR_I (Distortion. Threshold for Intra).	00H
60	MAX_DIST_I	d7-d0: MAX_DIST (Maximum Distortion for Inter).	00H
61	MAX_DIST_A	d7-d0: MAX_DIST (Maximum Distortion for Intra).	00H
62	VID_BUF_LEFT	d7-d0: Space left in ZR36506 SDRAM buffer for compressed video data (given in units of 2KB). **Read-Only Register.**	00H
63	LFP_LSB	d7-d0: bits 10-3 of LAST_FRM_PNTR (SDRAM pointer).	00H

Register Address	Register Name	Function	Default Value
		Read-Only Register.	
64	LFP_MSB	d6-d0: bits 17-11 of LAST_FRM_PNTR (SDRAM pointer). d7: RAM_FULL ('1' if event occurred from last Read). **Read-Only Register.**	00H
65	VID/LPF	d1-d0: VID_BUF_LEFT[9..8]. d3-d2: LPF[19..18]. d7-d4: '0000' reserved. **Read-Only Register.**	00H

5 INTERNAL MICROCONTROLLER HOST REQUEST INTERFACE

In USB mode, the ZR36506 internal 8-bit microcontroller (the V8) waits for a command from the host PC to perform one of the following tasks: Load EEPROM, Upload Flash, cancel Flash Upload and Erase Flash.

In USB mode, the microcontroller does not access the RBCS directly. This is due to the fact that in this mode, the master of the RBCS is the host PC (via USB).

The following register is an interface with the microcontroller:

RBCS Address	Register Name	Function		Value	Default Value
66	V8_CMMND (R/W register)	d0:	LD_EPRM (Download EEPROM to SRAM).	'01'	00H
		d1:	LD_FLSH (Upload Flash to PC).	'02'	
		d0-d1:	CLR_FLSH (Clear Flash memory).	'03'	
		d2:	CNCL_LD (Cancel Flash Upload).	'04'	
		d3-d7:	reserved.		

Once the ZR36506 device is connected to USB, the software driver can perform these operations:

1. Set the LD_EPRM bit (Reg.66, bit d0). This causes the camera to update the V8 software from the external EEPROM, if it exists. Note that before setting the LD_EPRM bit of Reg.66, the SER_MODE Reg. (Reg.7) has to be set to 0xb0. After setting the LD_EPRM bit, the software waits until the LD_EPRM bit returns to '0'.
2. Set the AUTO_BLK bit (Reg.7, bit d7) to enable the V8 to use the Bulk pipe to send data to the host computer. Set the LD_FLSH bit (Reg.66= 0x02, bit d1). This causes the camera to upload all picture and audio data from Flash memory to the host computer using the Bulk pipe (EP #4). The software should wait until the LD_FLSH bit returns to '0'. Note that even if there is no data in the Flash memory (i.e. no pictures were taken), the data transfer starts from address 0 of the Flash memory and ends at the last byte of the Flash (size of the Flash memory is 2 Mbytes). Note that audio data is optional and follows the given picture.
3. If there is a request to cancel the operation of uploading the Flash memory, set the CNCL_LD bit (Reg.66=0x04, bit d2). The software waits until Reg.66 returns to 0x00.
4. Set the CLR_FLSH bits (Reg.66, bit d0-d1, 0x03) upon request from user. This causes the camera to erase Flash memory. The software waits until Reg.66 returns to 0x00.

6 V8 µ-RISC BLOCK

General

The v8 µ-RISC is an 8-bit microcontroller, which is used in a detachable USB standalone mode to control and store captured still images and audio clips in FLASH memory. It initializes the camera and sets the required registers to perform still image capture. In A/V stream standalone mode, the microcontroller transfers data from corresponding data FIFOs to the serial interface.

When connected to a PC, it is possible to download stored images and audio clips.

Memory Resources

The µ-RISC will require the following memory resources:

- External 2 Kbyte EEPROM which contains all parameters for the ZR36506 operation mode, camera setup parameters and tables, Video/Audio Class parameters, and optional direct code for the microcontroller to replace specific functions or add special, new functionality.
- On-chip 5 KByte ROM, which contains the kernel program, service routines, interrupt handling routines and main program.
- On-chip 2 Kbyte SRAM, which is used for Stack, Interrupt Vectors, EEPROM download, and microcontroller work area.

7 POWER MANAGEMENT

To meet USB standard requirements, the ZR36506 must be able to control USB power supply for the entire device implemented around it. Two pins of the ZR36506 were dedicated to this task: PWR_DWN and SUSPND. Both pins are Open-Drain, and active when High-z.

The USB standard requires that once a device is hot-connected, it must consume no more than 100 mA from the USB port. After configuration, the device may consume up to 500 mA. Additionally, the device must not consume more than 0.5 mA in Suspend mode.

The ZR36506 uses its power management pins as follows:

- The PWR_DWN pin was designed to switch the USB 5v source to the video/audio source circuit (CCD, DSP, ADC, µ-Controller, Video-Decoder, audio CODEC, etc.). The only ICs that continue to receive normal power supply in the Power-Down state are the ZR36506, SDRAM, and EEPROM (all ICs operate on 3.3 V).
- The SUSPND pin was designed to enable the designer to shut down any additional element in the ZR36506 application circuit, which may increase the total current consumption to more than the USB standard allows (> 0.5 mA).

Refer to the ZR36506 Application Notes for an example of how the PWR_DWN and SUSPND pins should be used, and for the 3.3 V supply in application design.

The ZR36506 software driver can control part of the power-management process through the following registers on the ZR36506:

Parameter	Register Address	Usage
SSPND_EN	Reg.0/d1 SSPND_EN	Enable Suspend state: 0: Default (after Reset). Responds to USB Suspend condition as required by USB standard. 1: Suspend state is disabled.
PWR_VID	Reg.0/d5 PWR_VID	Apply USB 5 V to Video/Audio Source 0: Default (after Reset). Video/Audio Source is OFF. 1: Video/Audio Source is powered ON.
RES2	Reg.0/d2 RES2	Restart End-Point #2 (Video pipe) in the ZR36506: 0: Default (after Reset). Restart ZR36506 video path. 1: Enable ZR36506 Video Processor and Pipe circuit (after video source is powered on).

After a USB-Reset operation, the ZR36506 is in its Power Down state (PWR_DWN pin is set to High-z). After configuration, the software sets the PWR_VID bit to '1' to turn on the camera circuit (PWR_DWN='0'). Suspend (if SSPND_EN bit is not set by software) occurs if a USB Idle state is detected for as long as 3 milliseconds, and resets the PWR_VID bit.

8 VIDEO INPUT INTERFACE

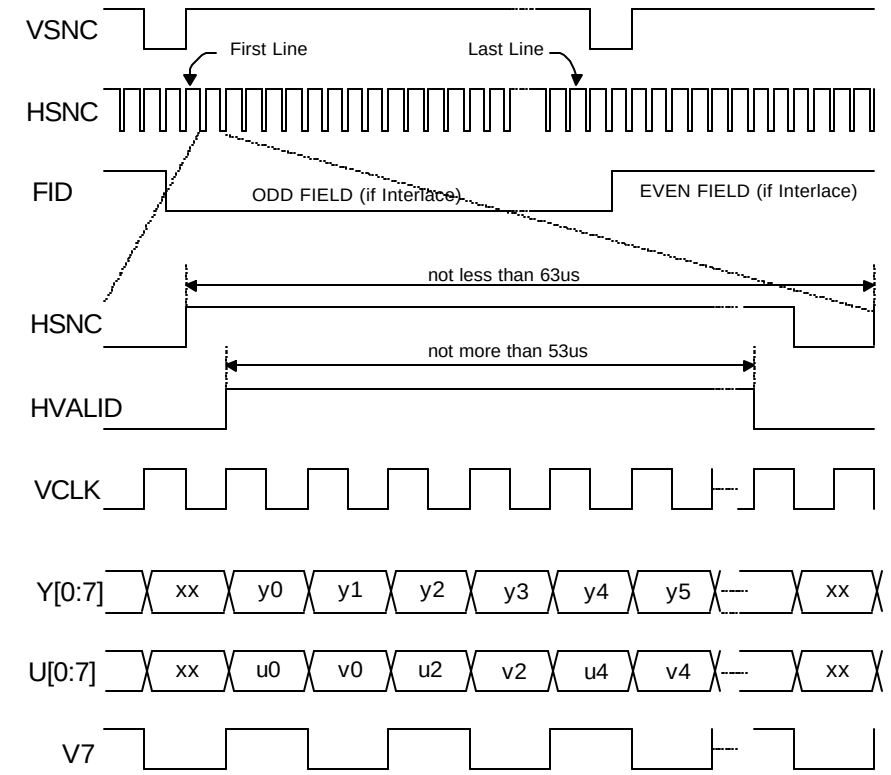
The ZR36506 digital video input is in YUV format. The ZR36506 interface for this format is flexible and supports 4:2:2 (8-bit, or 16-bit), and 4:1:1 timings (12-bit). Horizontal and vertical controls may be physical pulses or coded signals. Additionally, pixel clock and pulse polarity of the control signals may be programmed to either positive or negative.

All the input buffers in the ZR36506 that are supposed to be connected to the digital video source are 5-volt tolerant. This means that a camera with 5-volt CMOS outputs will not cause any damage to the ZR36506, even though the ZR36506 operating voltage is 3.3 Volts.

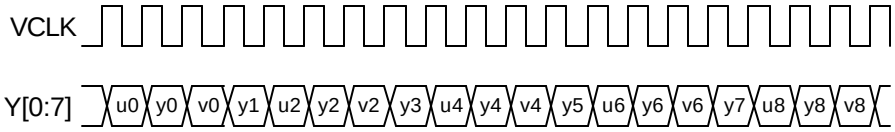
The ZR36506 digital video input consists of the following signals:

- **Y0-Y7**
  In the 4:2:2 16-bit, and 4:1:1 (12-bit) modes, this is the Luminance input bus. In the 4:2:2 8-bit mode, this bus is used for mux YUV data. This bus is sampled by the VCLK input clock for the unsigned binary value (0-255) of the Y component (or U and V as well in the 8-bit mode).
- **U0-U7**
  This is the Color (U or U/V) input bus. In the 4:2:2 16-bit and 4:1:1 (12-bit) formats, this bus is sampled by the even cycles of VCLK input clock for the binary value (0-255) of the U component, and by the odd cycles of VCLK input clock for the binary value (0-255) of the V component.
- **VSYNC**
  This is the Vertical Synchronization pulse, which indicates the start of a new video field (in Interlaced mode) or the start of a new video frame (in Non-Interlaced mode). This pulse is normally negative.
- **HSYNC**
  This is the Horizontal Synchronization pulse, which indicates the start of a new video line. This pulse is normally negative.
- **FID**
  This signal is used in Interlaced mode, to indicate whether the current field is even or odd. In Non-Interlaced mode, this input is ignored by the ZR36506.
- **VCLK**
  This signal is the video pixel clock. It is used by the ZR36506 to sample all other inputs in the digital video interface.
- **HVALID**
  This input is the pixel valid qualifier. When inactive, the ZR36506 refers to the samples that come from the Y, U, and V buses as blank pixels (which are not considered a part of the digital image). The ZR36506 may be programmed to ignore the HVALID input.

The digital video camera timing signal expected by the ZR36506:

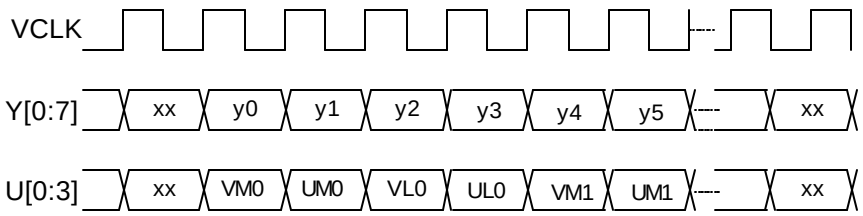


YUV-4:2:2 mode - 16-bit. Note that the order of U/V is set by Reg.49/d0.



YUV-4:2:2 mode 8-bit. Note that the order of Y/U/V is set by Reg.49/d2-d0

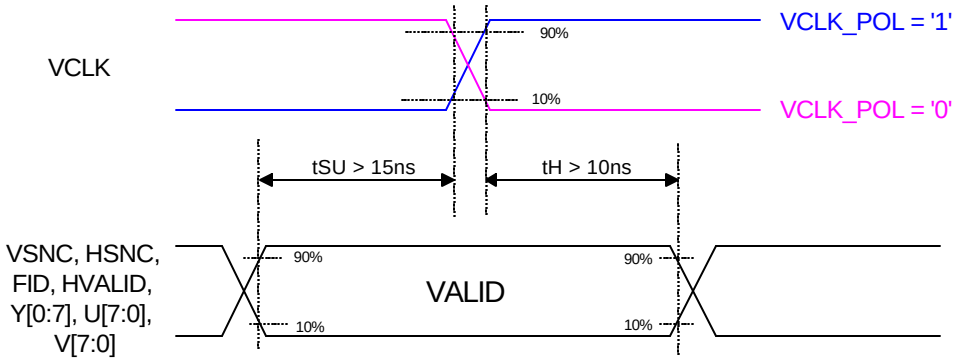
In YUV 8-bit mode, the VCLK frequency is twice the pixel rate.



VM0 = v0[7..4], VL0 = v0[3..0] UM0 = u0[7..4], UL0 = u0[3..0]

YUV-4:1:1 mode (12-bit)

Video Interface Timing Parameters



Input Video Parameters

The ZR36506 was designed to interface to most available YUV formats. To make this possible, most video parameters are programmable via specific registers from the ZR36506 Register Bank.

The following table specifies all parameters that may be set by the host computer to fit a specific video source (digital camera, video decoder, etc.):

Parameter	Register Address	Usage

Parameter	Register Address	Usage
VIN_MODE[2..0]	Reg.27/d2-d0 VIN_REG1	Video input mode: 000: 8-bit 4:2:2 mode, using synchronization pulses. 001: 8-bit 4:2:2 mode, using CCIR 656 sync. codes. 010: 16-bit 4:2:2 mode, using synchronization pulses. 011: 16-bit 4:2:2 mode, using CCIR 656 sync. codes. 110: 12-bit 4:1:1 mode, using synchronization pulses. 101, 111: spare.
VSNC_POL	Reg.27/d3 VIN_REG1	Polarity of VSNC pulse: 0: Synchronize on up-going edge. 1: Synchronize on down-going edge.
HSNC_POL	Reg.27/d4 VIN_REG1	Polarity of HSNC pulse: 0: Synchronize on up-going edge. 1: Synchronize on down-going edge.
FID_POL	Reg.27/d5 VIN_REG1	Polarity of FID (Field Identifier in Interlace mode) : 0: FID='0' during first (odd) field. 1: FID='0' during second (even) field.
HVALID_POL	Reg.27/d6 VIN_REG1	Polarity of HVALID signal: 0: input signal HVALID='1' for active pixels. 1: input signal HVALID='0' for active pixels.
VCLK_POL	Reg.27/d7 VIN_REG1	Polarity of VCLK (pixel clock): 0: Camera data valid at VCLK falling edge. 1: Camera data valid at VCLK rising edge.
AUTO_FID	Reg.28/d0 VIN_REG2	0: Use external FID signal. 1: Generate internal toggling FID. Ignore FID pin.

Parameter	Register Address	Usage
NON_INTERLACE	Reg.28/d1 VIN_REG2	0: Interlace mode. Only even fields are transferred. 1: Non-interlace mode. All frames are transferred.
NO_HVALID	Reg.28/d2 VIN_REG2	0: Normal operation. 1: Ignore the HVALID input (assume constant '1').
UV_ID	Reg.28/d3 VIN_REG2	0: Normal operation. 1: Use V7 input as a U/V identifier ('1'=U, '0'=V).
FIX_2C	Reg.28/d4 VIN_REG2	Fix 2's Compliment U/V values 0: Normal operation. 1: Invert U[7] and V[7] to fix to Unsigned Binary.
XSIZE_IN[9..0]	Regs.29-30 LXSIZE_IN MXSIZE_IN	Number of pixels in active line of video source.
YSIZE_IN[9..0]	Regs.31-32 LYSIZE_IN MYSIZE_IN	Number of active lines in frame (/field) of video source.
X_OFFST[9..0]	Regs.33-34 LX_OFFST MX_OFFST	Horizontal offset (number of pixels to be skipped after start of line).
Y_OFFST[9..0]	Regs.35-36 LY_OFFST MY_OFFST	Vertical offset (number of lines to be skipped after start of frame).
DVI_YUV[2..0]	Reg.49/d2-d0 DVI_YUV	Order of Ya/U/V/Yb components of a pixel-pair in 8-bit modes (d0 affects 16-bit mode also): d0: '0': U comes before V. '1': U comes after V. d1: '0': Ya comes before U/V. '1': Ya comes after U/V. d2: '0': Yb comes before U/V. '1': Yb comes after U/V.

Parameter	Register Address	Usage
SLOW_CLK12 SLOW_CLK16	Reg.49/d7-d6 DVI_YUV	Use these control bits for cameras that have slow VCLK or too short Horizontal Blank time interval: d6: '0': Normal operation. '1': Select 12 MHz clock during Horizontal Blank. d7: '0': Normal operation. '1': Select 16 MHz clock during Horizontal Blank.

Frame-Rate Control

A camera, or any other video source, normally provides a fixed number of frames per second. For example, an NTSC-based camera will always provide a frame rate of 30 frames per sec.

The ZR36506 allows the application software to modify the effective frame rate to fit its needs. This allows some of the frames coming from the camera to be dropped before processing, eliminating the effort that would be wasted on frames dropped by the computer anyway.

The parameter that controls the effective frame rate is called FRM_RATE, and is specified in the following table:

Parameter	Register Address	Usage
Numerator[4..0]	Reg.37/d4-d0 **n**	Frame Drop factor (**n** = 0-31). Effective frame rate is: NTSC: 30*(**n**+1)/**d.** PAL: 25*(**n**+1)/**d.**
Denum.code[1..0]	Reg.37/d6-d5 code for **d**	'00': **d**=32. '01': **d**=30. '10': **d**=25.

The **n** parameter ranges from 0 to **d**-1. The value **n**=**d**-1 instructs the ZR36506 to transfer to the host computer the full frame-rate that is delivered from the video source. Any value **n** that is less than **d**-1 results in dropped frames from time to time, so that the effective frame rate is only (**n**+1)/**d** of the full frame-rate.

Video Scaling

The ZR36506 has two independent down scalers: one for frame width and one for frame height. It is the responsibility of the software application to select scale factors that result in a reasonable aspect ratio.

In order to set the scaling factor, the host computer must simply specify the desired size of the output frame (assuming XSIZE_IN and YSIZE_IN are initially set). Scaling is performed automatically by the ZR36506, regarding the output frame size versus the input frame size.

The following table specifies the parameters that are used to set the output frame size:

Parameter	Register Address	Usage
XSIZE_O [9..0]	Regs.38-39 LXSIZE_O MXSIZE_O	Number of pixels in line of scaled output video frame.
YSIZE_O [9..0]	Regs.40-41 LYSIZE_O MYSIZE_O	Number of lines in scaled output video frame/field.

Note that if the host computer specifies the same values for input frame size and output frame size, no scaling occurs (scaling factor is 1:1).

The ZR36506 performs no Up-Scaling (to produce CIF size from 240-line video fields, a special interpolation process is applied by the software driver). This means that XSIZE_O should never be greater than XSIZE_IN, and YSIZE_O should never be greater than YSIZE_IN.

Video Filters

The ZR36506 uses internal programmable anti-aliasing filters for the scaling process. There are two filters that are used: one for horizontal scaling, and the other for vertical scaling. The filters are programmed independently of each other, and independently of the scaling factors.

Both horizontal and vertical filters use a combination of FIR structure and interpolation to eliminate pixel jitter in the output frame. The interpolation process effectively improves the resolution of the input frame by a factor of 4, both horizontally and vertically.

The following table specifies the register that is used to set filter parameters:

Parameter	Register Address	Usage
XFILT_CONT [2..0]	Reg.42/d2-d0 FILT_CONT	Select one of 5 possible horizontal filters.
YFILT_CONT [1..0]	Reg.42/d4-d3 FILT_CONT	Select one of 3 possible horizontal filters.

The following table specifies the horizontal filters:

XFILT_CONT [2..0]	FIR Filter Applied (Horizontally)	Interpolation (Horizontally)
000	FIR = (1.0)	NO
001	FIR = (1.0)	YES
010	FIR = (0.5, 0.5)	YES
011	FIR = (0.25, 0.5, 0.25)	YES
100	FIR = (0.25, 0.25, 0.25, 0.25)	YES

The following table specifies the vertical filters:

YFILT_CONT [1..0]	FIR Filter Applied (Vertically)	Interpolation (Vertically)
00	FIR = (1.0)	NO
01	FIR = (1.0)	YES
10	FIR = (0.5, 0.5)	YES

Video Output Format

The ZR36506 supports 3 different formats for output video data: Compressed data format, YUV 4:2:2 and 4:2:0 Raw data formats.

The following table specifies the register that is used to set output video format:

Parameter	Register Address	Usage
VO_MODE [6..0]	Reg.43/d6-d0 VO_MODE	Select one of 3 video output formats: 0x60 = Compressed data format. 0x03 = YUV 4:2:2 Interleaved format. 0x14 = YUV 4:2:0 Planar format.

It is the responsibility of the ZR36506 software driver to make conversions to provide the application software with several OS standard video data formats, but the data that is transferred via USB must be one of these 3 formats.

Compressed Data Format

The ZR36506 compressor is designed to compress YUV 4:2:0 frames (12 bits/pixel) by a factor of 1:3 to 1:15 (resulting in 4 to 0.8 bits/pixel). The compression algorithm is a proprietary Zoran development, which meets 3 important requirements that were made to guarantee the high performance of the ZR36506:

- Fits the selectable bandwidth of the USB (0.5 - 7.5 Mbits/sec)
- Supports variable compression rates (in very small increments)
- Requires minimum CPU time for decompression (and fits the MMX® concept)

The ZR36506 compressor compresses specific frames using its “Intra” mode and all others using its “Inter” mode. Intra mode does not require any previous frame, while Inter mode is always based on a reconstructed previous frame. “Intra” frames provide the algorithm with relative resistance to error propagation between frames but consume more bits per pixel than “Inter” frames. Error propagation within the frame itself (from higher lines to lower lines) is eliminated by dividing the frame into many horizontal strips.

YUV 4:2:2 Interleaved Format

In this format, the ZR36506 transfers to the host computer 2 bytes for every pixel (16 bits/pixel). The Y-component is available for every pixel, but the U and V components are each available for every second pixel (Y0, U0, Y1, V2, Y2, U2, Y3...).

YUV 4:2:0 Planar Format

In this format, the ZR36506 transfers to the host computer 3 bytes for every 2 pixels (12 bits/pixel). The Y-component is available for every pixel, but the U and V components are only available for every second pixel in even lines.

In this mode, the host computer receives a frame preformatted in the planar mode; this can save CPU time in the host computer in most video conferencing applications. The Y and U/V components are packed by the ZR36506 in 64-byte packets, and have the following structure:

Packet Number	Contents
1	Pixels 0-63 of the Y-Image.
2	Pixels 64-127 of the Y-Image.
3	Pixels 0-63 of the U-Image (or V-Image). The U-Image and V-Image are half-size of the Y-Image in both horizontal and vertical dimensions. The ZR36506 produces a line of U pixels followed by a line of V pixels, and then U pixels again in a toggling manner. These pixels are always packed in this modulo-3 packet. The host computer - knowing the frame-size - can separate between U and V components.
4	Pixels 128-191 of the Y-Image.
5	Pixels 192-255 of the Y-Image.
6	Pixels 64-127 of the U-Image (or V-Image).

Video Buffer Control registers

The ZR36506 uses a pre-defined SDRAM space to store the output video data before being transferred to USB; this buffer is called Video Buffer, and is used as a FIFO which observes data bursts at the video frame rate (up to 30 Hz) and supplies data bursts at the USB frame rate (1000 packets per second).

The size of the video buffer is set by the host computer via the SDRAM registers. Depending on USB bandwidth and output frame size and rate, this buffer may become full in the middle of video streaming. In this case, additional frames will be dropped by the ZR36506 until enough free space is available in the buffer. When operating in Compressed mode, the host computer can alter the compression rate by modifying some threshold registers on the fly. This may prevent most "buffer-full" events and allows for consistent frame-rate (i.e. frames are not dropped). To enable the host computer to monitor the status of the video buffer and control frame-dropping, the ZR36506 provides the following registers:

Parameter	Register Address	Usage
BUF_THR [9..0]	Reg.48/d7-d0 Reg.49/d4-d3	Minimum remaining buffer space to begin frame dropping (in 2 Kbyte units). "Buffer-Full" occurs when remaining buffer space is less than the value in this register. The host computer sets this register according to the maximum space that a video frame may occupy.
VID_BUF_LEFT [9..0]	Reg.62/d7-d0 Reg.65/d1-d0	This is a read-only register that provides the actual remaining buffer space (in 2 Kbyte units). The host computer can prevent "Buffer-Full" occurrence by monitoring this register and changing compression thresholds.
LFP [19..0]	Reg.63/d7-d0 Reg.64/d6-d0 Reg.65/d3-d2	This is a read-only register that provides the SDRAM address for data write in the video buffer at the end of every video frame (in 16 byte units). The host computer can keep track of the current compression rate by monitoring this register from time to time.

Special Video Control bits

The ZR36506 has two special bits in the VIN_REG2 register, which may alter the input video sequence. These bits are normally used during still capture operation and are specified in the following table:

Parameter	Register address	Usage
SEND_FID	Reg.28/d5 VIN_REG2	Send FID information in frame header data. The FID information is used for reconstructing a 2-field frame from an Interlaced camera. 0: Default value. 1: FID bit overrides bit 0 of Frame_Phase[4..0].
KEEP_BLANK	Reg.28/d7 VIN_REG2	Force a "blank" position on the input video frame source, and drop new frames. Software driver must switch this bit from '0' to '1' during a true blank position. 0: Default value. 1: Keep existing blank longer by forcing "blank".

USB Pipe Video Data Format

Data Packets

Video data is received by the host computer as a stream of bytes via the End-Point #2 Isochronous pipe. There is an incoming data packet every 1 millisecond (every USB-Frame) and its size is limited by the maximum bandwidth that was initially set for End-Point #2. The maximum byte-count for each packet is one of the following numbers: 959 (for 7.5Mb/sec), 895, 831, 767, 703, 639, 575, 511, 447, 383, 319, 255, 191, 127, or 63 (for 0.5Mb/sec). Regarding the data on the USB - the data of a new video frame always starts in a new data packet, so in most cases the last packet of a video frame is shorter than a normal packet. The ZR36506 sends one or more empty packets between every two video frames.

Video Frame Synchronization

In all modes of operation (Compressed or Raw video), two concurrent video frames will be separated by at least one empty data packet. The ZR36506 software driver uses this to detect a Start-Of-Video-Frame. Additionally, the first two bytes of the video frame header contain a Start-Of-Video-Frame-Pattern (=0xAA55), which is used by the software driver as a qualifier to verify that the data represents an uncorrupted video frame.

Video Frame Header

A header precedes every video frame. The header data is organized in Little-Endian format, i.e. the LSB of a 2-byte parameter precedes the MSB (LSB occupies the lower address). The same header format is used in all modes of operation. The following table specifies the parameters of this header:

Offset	Parameter Name	No. of Bytes	Description & Specification
0	Vid_Frm_Patt	2	0xAA55 = Start of Video-Frame Pattern.
2	Header_Length	1	Number of bytes in this header = 12.
3	Frame_Numb	1	D4-D0: Unsigned integer. Incremented (mod 32) on every frame that is delivered to host computer. D7: Capture_Pressed (active if '1'). D6: Resumed ('1': first frame after Suspend). D5: spare
4	Frame_Phase	1	D4-D0: Unsigned integer. Incremented mod 30 on every frame that is acquired from camera. D7-D5: spare.
5	Frame_Latency	1	Unsigned integer. Number of milliseconds elapsed from the moment that the camera began delivery of this frame to ZR36506, to the moment that the ZR36506 began delivery of frame-header to USB.
6	Data_Format	1	D7: '0'=Vendor Specific (like ZR36506) (‘1’=Class Specific). D6: '0'=Raw Data. '1'=Compressed Data. D5-D0: Vid_Format_Code: 0x03 = YUV-4:2:2. 0x14 = YUV-4:2:0 Planar. 0x06-0x12, 0x15-0x1F = spare. 0x20 = Zoran's Compression.

Offset	Parameter Name	No. of Bytes	Description & Specification
7	Format_Param	1	D7: Intra_Frame ('1' = Intra, '0' = Inter + Intra). This bit should be ignored in raw data frames. D6: spare. D4-D0: Pix_Depth (number of bits per pixel). These bits should be ignored in compressed data frames.
8	Frame_Width	2	Unsigned Word integer - number of pixels per line.
10	Frame_Height	2	Unsigned Word integer - number of lines in frame.

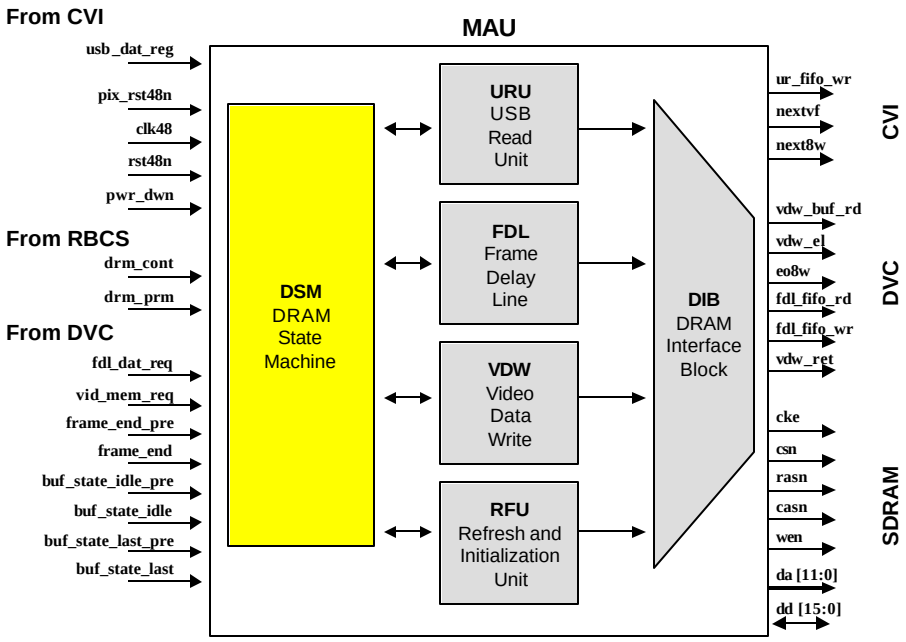
9 SDRAM CONTROL AND INTERFACE

MAU (Memory Access unit)

The MAU is responsible for all data transfers between the internal units and external SDRAM. The SDRAM in use is organized as two Banks of 524,288-Word X 16 Bit and is accessible via a 16 Bit data bus. The design is based on 3.3 V powered SDRAMs manufactured by Micron (MT48LC1M16A1) and Fujitsu (MB81F161622C). The SDRAM operation modes employed by the MAU are:

- Full-Page-Mode-Read
- Full-Page-Mode-Write
- Burst-of-8-Read
- Auto Precharge Mode
- Manual two Bank Precharge
- CAS Latency = 2 to support SDRAMS that do not have CAS Latency = 1(also sufficient for operating frequency of 48 MHz). Both 8.2 ms and 16 ms refresh rates are supported.

Refer to the following MAU main block diagram:



The MAU performs the following tasks:

- **Read data from SDRAM to USB Fifo**
  The Universal Serial Bus can transfer 12 Mbits/sec – while this is considered the USB peak-rate, the maximum average rate that can be used for video data is approximately 8 Mbits/sec (Iso 1023 bytes every 1ms). The MAU performs an 8-word Read operation to fill the USB Fifo. This lasts about 340 ns, and is expected to be performed every 10.6 us on average (assuming continuous 12 Mbit/sec demand).
- **Read & Write data from/to SDRAM to obtain one video-frame delay**
  The video source for this operation is the reconstructed image from the Digital Video Compressor (DVC), and its timing is derived from the Digital Video Scaler (DVS) output. There are two FIFOs for this task in the DVC - one for Write to SDRAM operations and one for Read from SDRAM operations. The data that is written to SDRAM from the Write Fifo is read back from SDRAM to the Read Fifo after a delay of approximately one video frame. This task is active only in Compressed Video mode, and its video format is always 4:2:0 (12 bits/pxl). The pixel rate is 12.2727 MHz for NTSC and 14.75 MHz for PAL (or 9.545454 MHz and 14.31818 MHz in Sanyo cameras), so the maximum rate in 16-bit words is approximately 11.0625 Mw/sec for PAL when full frame-size is used. In all these systems, the active line lasts within 53 us, followed by a 10-11 us blank with no activity. The MAU uses 32-word Page-Read and 32-word Page-Write operations to perform the transfer. This lasts approximately 1600 ns, and is expected to be performed every 2893 ns in worst cases (at rates of 11.0625 Mw/sec).
- **Write output video-data to SDRAM**
  This is the same data that is later on read back into the USB Fifo. The source for this data is the Video Data Buffer which is located in the DVC (Digital Video Compressor). When operating in Compressed Video mode, the Video Data Buffer is first filled with compressed data of at least one video frame line (one line for full-frame size, and additional lines for small frame sizes). This takes place during the active-line time interval, so that the Video Data Buffer is ready to be transferred to SDRAM when the video blank time interval begins. The blank time-interval lasts approximately 10 us, and during this time the MAU writes up to 384 words to SDRAM, using Page-Write mode. The MAU uses a Page-Write operation, which lasts approximately 8400 ns (if N=384 in worst cases, where the MAU encounters end of 256-word SDRAM line twice during the burst). When operating in Raw Video mode, the Video Data Buffer is split into two 192-word buffers. At the same time that one buffer is being filled with Raw video data (this time arriving from the DVS), the other buffer is being transferred to SDRAM. This process is carried out during the active-line time, as well as during the blank time - whenever there is data ready to be written to SDRAM. Residual data is transferred at the end of the video frame.
- **SDRAM Refresh**
  A refresh operation lasts 60 ns and uses Auto Refresh. The ASIC supports both 8.2 ms and 16 ms refresh SDRAMs (32 ms, 2048-cycle refresh or 64 ms, 2048-cycle refresh). 8 ms rate produces a 32 mS x 2048 cycle refresh (15.625 uS between refresh tasks), while 16 ms rate produces a 64 mS x 2048 cycle refresh (31.25 uS between refresh tasks).

- **SDRAM Initialization**
  SDRAM requires initialization after Reset, Suspend and power down. Users should write 1 to register 18 (DRM_CONT) bit 1 of RBCS after these events, allowing the SDRAM at least 100 microseconds to stabilize intemal circuitry. The MAU then automatically performs an SDRAM initialization sequence and allows other memory tasks to be performed. This task lasts approximately 600 nS.

- **In the beginning of every task, the MAU programs the Mode Register, utilizing the address bus.**
- **CAS Latency is always set to 2, Burst type is always sequential, and Burst length is set to 8 for USB Fifo read tasks and to Full-Page for all other tasks. Only the USB Fifo read task employs Auto Precharge. All other tasks (Read and Write) perform a PALL command during task command sequence.**

The following table specifies the registers that are used to support SDRAM:

SDRAM and Memory Buffer Setup Registers

Register Address	Register Name	Function	Default Value
18	DRM_CONT	d0: REF '0' = 8.2 ms refresh rate. '1' = 16 ms refresh rate. d1: SDRAM_EN. d2: RES_UR Restart video out buffer read logic. d3: RES_FDL Restart video-frame-delay logic. d4: RES_VDW Restart video out buffer write logic. d5-d7: reserved.	00H
19	DRM_PRM1	d0-d3: Bits 16 to 19 of FDL_LAST_WORD. d4-d7: Reserved.	00H
20	DRM_PRM2	d0-d3: Bits 8 to 11 of FDL_1ST_LINE. d4-d7: Reserved.	00H
21	DRM_PRM3	d0-d3: Bits 8 to 11 of VDW_1ST_LINE. d4-d7: Bits 8 to 11 of VDW_LAST_LINE.	00H

Register Address	Register Name	Function	Default Value
22	DRM_PRM4	d0-d7: Bits 0 to 7 of FDL_1ST_LINE.	00H
23	DRM_PRM5	d0-d7: Bits 0 to 7of FDL_LAST_WORD.	00H
24	DRM_PRM6	d0-d7: Bits 8 to 15 of FDL_LAST_WORD.	00H
25	DRM_PRM7	d0-d7: Bits 0 to 7 of VDW_1ST_LINE.	00H
26	DRM_PRM8	d0-d7: Bits 0 to 7 of VDW_LAST_LINE.	00H

Video Setup and Control Registers

Register Address	Register Name	Function	Default Value
48	BUF_THR	d7-d0: Threshold for buffer space Frame-Drop decision (given in units of 2 KBytes).	00H
49	DVI_YUV	d2-d0: Code for YUV re-order processor. d4-d3: BUF_THR[9..8] Extension for 16 Mbit SDRAM. d6: SLOW_CLK12 '1' Select 12 MHz for Horizontal blank. d7: SLOW_CLK16 '1' Select 16 MHz for Horizontal blank. d5: '0' reserved.	00H

CLK48 Output

Register Address	Register Name	Function	Default Value
0	PWR_REG	d0: WD_EN: '1' Enables USB Watch-Dog timer. d1: SSP ND_EN: '0' Enables Suspend-Resume logic. d2: RES2 '0' Restarts End-Point #2 logic. '1' Releases. d3: CLK48_EN - '1' Enables 48 MHz at CLK48 output pin. d4: EP234_EN - '1'Enables SPO output in USB Mode. d5: PWR_VID - '1' Video-logic Power-On. d6: reserved. d7: E2_EN - '1' Enables EEPROM R/W.	00H

10 CAMERA CONTROL SERIAL PORT

The ZR36506 has a dedicated Programmable Serial Port intended to be used for camera control. This port has several modes of operation, where the ZR36506 is always the bus-master (one of the more useful modes is IICC). The programmable serial port is controlled by the host computer via the following registers of the ZR36506 register bank: SER_MODE, SER_ADRS, SER_CONT, SER_DAT1, SER_DAT2, SER_DAT3, and SER_DAT4.

Camera control uses 3 dedicated pins on the ZR36506:

- IICCK is an Open Drain output pin, used to drive the serial port clock signal. It is supposed to be connected to an external 3.3-10KΩ Pull-Up resistor to 3.3.
- IICDT is an Open-Drain bi-directional pin, used to send and receive the serial port data. It is supposed to be connected to an external 3.3-10KΩ Pull-Up resistor to 3.3.
- SENS is an Open Drain output pin, used as a serial control strobe signal in some modes of operation. It is supposed to be connected to an external 3.3-10KΩ Pull-Up resistor to 3.3.

There are 6 modes of operation available to the camera control port. These are listed in the following table, and described in more detail in the following paragraphs:

Mode Number	Mode Name	Description
0	Soft	Bit-level Software controlled mode.
1	SIO	Serial clocked I/O.
2	IIC LRACK	IICC with Last Byte Read Acknowledged.
3	IIC LRNACK	IICC with Last Byte Read Not Acknowledged.
4	CAM1	Camera 1 - refer to timing diagram.
5	CAM2	Camera 2 - refer to timing diagram.

Modes number 1-5 are referred to as automatic modes: in these modes, the host computer only needs to write the data bytes (and, in some of them, the device address byte) in certain registers (SER_DAT1 to SER_DAT4, and SER_ADRS), and initiate a transfer request. Similarly, the host computer can read received data from the same registers.

The SER_MODE register has some specific bits that can turn the automatic modes into more flexible serial data formats. These register bits are:

- **CLK_RATE**
  Writing '0' to this bit will select a 93.75 KHz clock at the IICCK output. Writing '1' to this bit will select a 1.5 MHz clock at the IICCK output.
- **CLK_POL**
  Writing '0' to this bit will select the normal polarity at the IICCK output. Writing '1' to this bit will select an inverted polarity at the IICCK output.
- **VSYNC**
  Writing '0' to this bit will select an immediate transfer. Writing '1' to this bit will delay start-of-transfer to camera blank period.

Another register that is used by the automatic modes is the SER_CONT register. This register is used by the host computer to control the serial port machine. The SER_CONT register consists of the following control bits:

- **SER_LEN**
  This field contains a 3-bit binary integer that specifies the number of data bytes that the host wishes to transfer in the serial transaction (the address byte is not counted). The range of this parameter is 0 to 4.
- **SER_DIR**
  Writing '0' to this bit selects a write operation (host to camera). Writing '1' to this bit selects a read operation (camera to host).
- **SER_GO / SER_BUSY**
  This is used as both a command and a status bit. Writing '1' to this bit will initiate a serial transfer request. The serial transfer will either start immediately or wait until the vertical blank time interval is detected at the camera video signal (depends on the VSYNC bit). The SER_GO / SER_BUSY bit will remain '1' until the end of the transaction, to indicate to the host computer when a new transaction may be initiated.
- **NACK_RCV**
  This is a read-only bit and is used in modes 2 and 3 only (IICC modes). The ZR36506, after completing a serial transfer in this mode, reports to the host computer via this bit whether or not all transmitted bytes were acknowledged by the camera (this includes the address byte and all data bytes that were sent from the host to the camera). A '0' in this bit indicates all ACK, and a '1' indicates a NACK for one or more bytes.
- **NO_STOP**
  This bit is used in modes 2 and 3 only (IICC modes) and enables multiple transactions inside a single START / STOP frame. When set to '1', it informs the serial machine to omit the STOP pattern at the end of the following transaction. Combined with the CONTINUE bit, this enables the software driver to perform long transactions (i.e. for downloading the Gamma-Correction table into camera DSP).

- **CONTINUE**
  This bit is used in modes 2 and 3 only (IICC modes), and enables multiple transactions inside a single START / STOP frame. When set to '1', it informs the serial machine to prepare for multiple transaction mode. It will never affect the following transaction, but the one coming after it, which will not contain a START pattern.

The following pages specify all 6 modes of operation for the camera-control serial port.

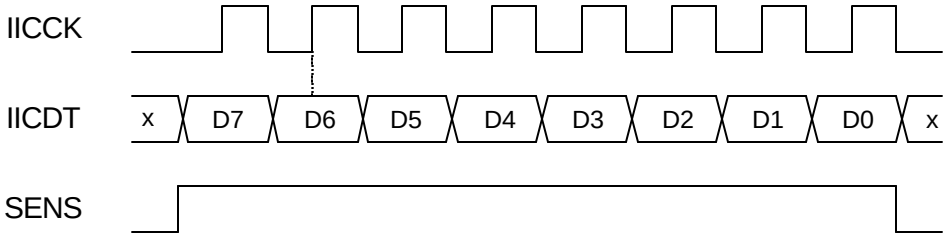
Soft Mode: (MODE=0)

This mode is selected when the MODE field (d7-d4) of the SER_MODE register is set to 0. In this mode the host computer may access the serial port pins directly in order to enable control of cameras that are not supported by the other automatic modes.

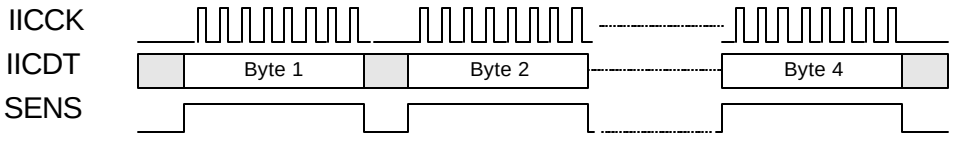
In Soft mode, the value of the CLK_OUT bit (d0) is reflected in the IICCK output pin. A write operation to the DAT_IO bit (d1) sets the value of the IICDT pin. A read operation from the same DAT_IO bit reads the actual voltage level at the IICDT pin. The value of the SENS_OUT bit (d2) is reflected in the SENS output pin.

SIO Mode: (MODE=1)

This is the Serial Clocked I/O automatic mode, and is selected when the MODE field (d7-d4) of the SER_MODE register is set to 1. The following waveform describe the SIO mode:



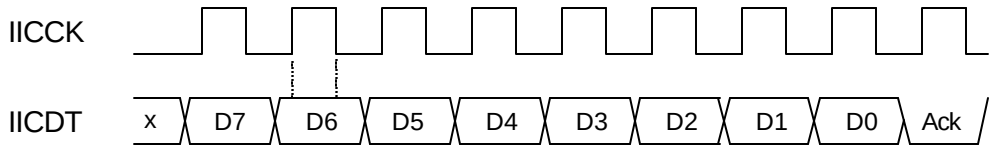
NOTE: In both Read and Write sequence, data is sampled in the up-going edge of the clock IICCK.



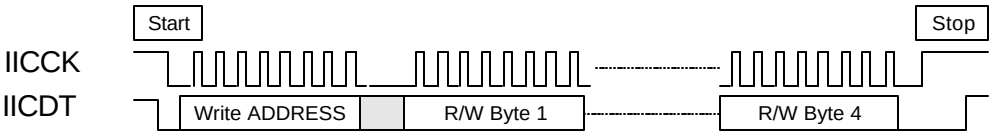
NOTE: In the SIO mode 1 to 4 bytes are written or read.

IIC LRACK Mode: (MODE=2)

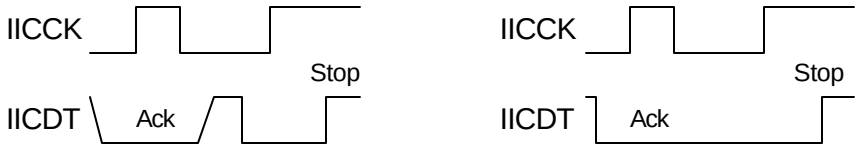
This is the IIC LRACK (Last Read Acknowledged) automatic mode, and is selected when the MODE field (d7-d4) of the SER_MODE register is set to 2. In this mode, the IICCK frequency is set to 93.75 KHz.



NOTE: In both Read and Write sequence, data should be stable during the '1' state of the clock IICCK. D7-D0 are sent by transmitter, Ack is sent by receiver.



NOTE: Start is defined when the IICDT turns from '1' to '0' while the IICCK is '1'. Stop is defined when the IICDT turns from '0' to '1' while the IICCK is '1'. The Address byte is written like any other byte.



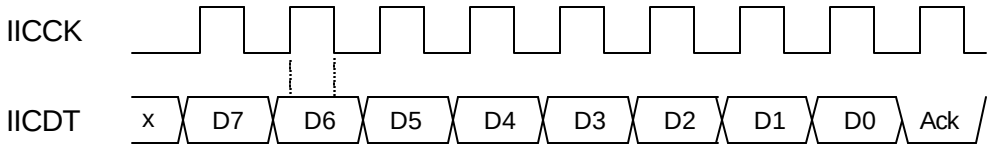
In this mode, the host defines the camera address byte and the data bytes to be written to the camera in the appropriate registers. The ZR36506 then sends these bytes automatically. Similarly, the ZR36506 may read data bytes from the camera. The ZR36506 acknowledges the last byte read like all other bytes.

By using the NO_STOP and CONTINUE bits, a concatenation of multiple IICC transactions is possible, in order to send or receive more than 4 bytes in a single START / STOP frame. Additionally, by using these control bits, write/read operations may be combined with a single STOP pattern at the end. Note that the SER_LEN parameter may be set to 0 to further support the concatenation operation mode.

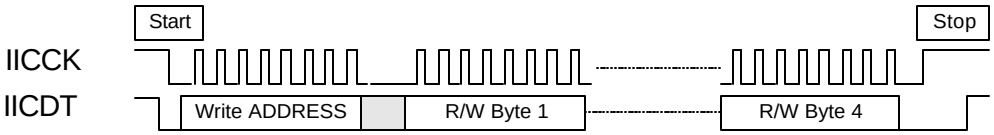
IIC LRNACK Mode: (MODE=3)

This is the IIC LRNACK (Last Read Not Acknowledged) automatic mode, and is selected when the MODE field (d7-d4) of the SER_MODE register is set to 3. In this mode, the IICCK frequency is set to 93.75 KHz.

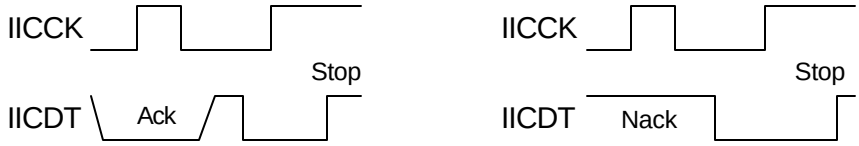
In this mode, the host defines the camera address byte and the data bytes to be written to the camera in the appropriate registers. The ZR36506 then sends these bytes automatically. Similarly, the ZR36506 may read data bytes from the camera. The ZR36506 does not acknowledge the last byte read from camera. This is done as a signaling to the camera that no more bytes are needed. The waveforms for this mode of operation are specified be low.



NOTE: In both Read and Write sequence, data should be stable during the '1' state of the clock IICCK. D7-D0 are sent by transmitter, Ack is sent by receiver.



NOTE: Start is defined when the IICDT turns from '1' to '0' while the IICCK is '1'. Stop is defined when the IICDT turns from '0' to '1' while the IICCK is '1'. The Address byte is written like any other byte.



End of Write sequence

End of Read sequence

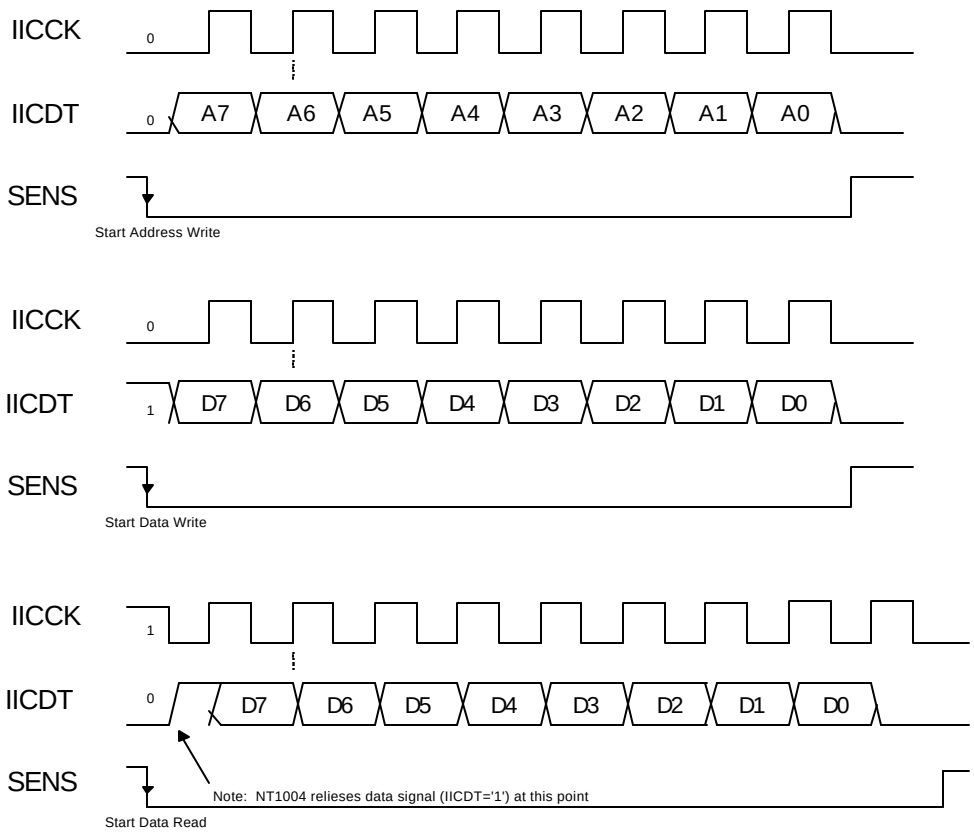
In this mode, the host defines the camera address byte and the data bytes to be written to the camera in the appropriate registers. The ZR36506 then sends these bytes automatically. The ZR36506 may also read data bytes from the camera. The ZR36506 does not acknowledge the last byte read (NACK).

By using the NO_STOP and CONTINUE bits, concatenation of multiple IICC transactions is possible, in order to send or receive more than 4 bytes in a single START / STOP frame. Additionally, by using these control bits, write/read operations may be combined with a single STOP pattern at the end. Note that the SER_LEN parameter may be set to 0 to further support the concatenation operation mode.

CAM1 Mode: (MODE=4)

This mode is selected when the MODE field (d7-d4) of the SER_MODE register is set to 4. In this mode, the IICCK frequency must not exceed 10 MHz.

Three signals are used: IICCK, IICDT and SENS. The host defines the desired camera register address byte and a single data byte to be written to that register in the appropriate ZR36506 registers. The ZR36506 first sends the address and then the data automatically. Similarly, the ZR36506 may read a data byte from any given camera register. The waveforms for the CAM1 mode are specified in the following diagram. Note that every byte transfer has its own start condition, which indicates one of 3 possibilities: Address Write, Data Write, or Data Read.



Register Write operation:	Address Write	Data Write
Register Read operation:	Address Write	Data Read

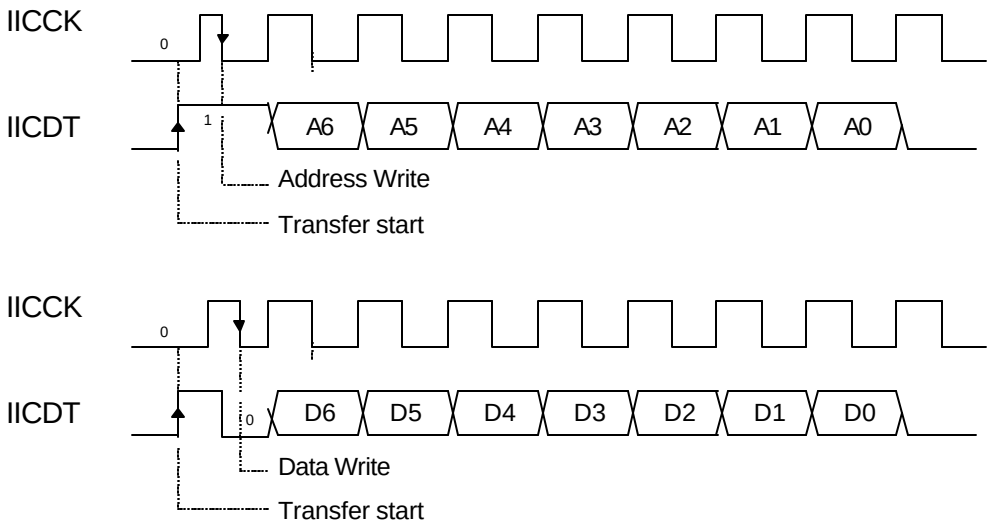
NOTE: A transaction consists of Address Write, followed by Data Write or Data Read.

CAM2 Mode: (MODE=5)

This mode is selected when the MODE field (d7-d4) of the SER_MODE register is set to 5. In this mode, the IICCK frequency must not exceed 10 MHz.

Only two signals are used: IICCK and IICDT. The host defines the desired camera register address byte and a single data byte to be written to that register in the appropriate ZR36506 registers. The ZR36506 first sends the address and then the data automatically. Note that in this mode, both address and data consist of 7 bits only. There is no way to read data from the camera.

The waveforms for the CAM2 mode are specified in the following diagram. Note that every byte transfer has its own transfer start signaling (which is identical for both address and data), followed by an Address Write condition or a Data Write condition.



Register Write operation:	Address Write	Data Write

NOTE: Data is sampled on the down-going edge of the clock IICCK. A transaction consists of Address Write, followed by Data Write.

11 EXTERNAL EEPROM

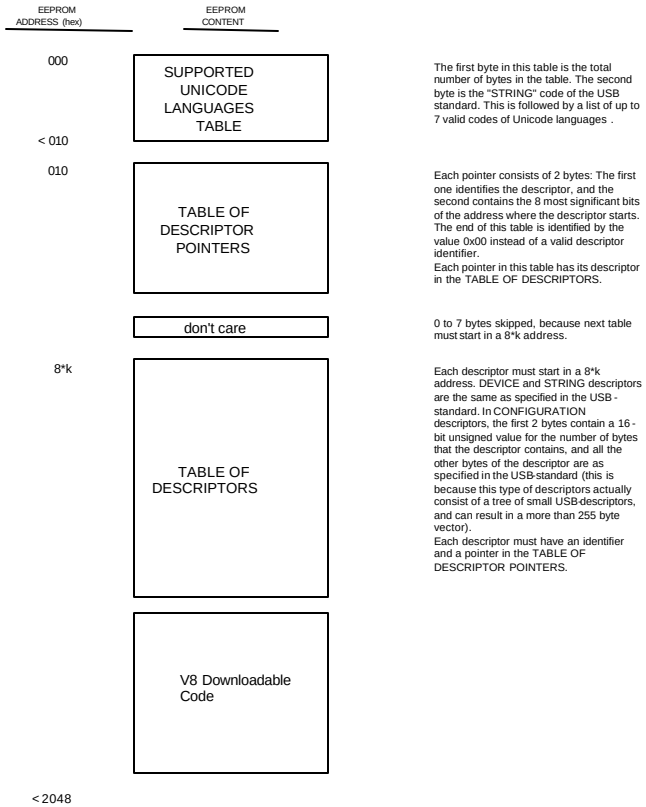
The ZR36506 provides a full USB compliant solution without the need for an external EEPROM (USB Vendor ID is pin programmable). When Unicode names are required, the ZR36506 may use an external 3.3 V 2 Kbyte Serial EEPROM as an optional source for USB descriptors. There are several vendors that produce these 8-pin EEPROM chips, which are pin-to-pin compatible.

Normally, the external EEPROM will only be read in a working device (soon after USB insertion). The ZR36506 supports on-board EEPROM programming, which can be used to alter some USB descriptors - especially the product serial number. The ZR36506 register bank includes special registers to perform a byte Read or Write operation to a given address of the EEPROM.

In addition to the USB Descriptors data, the external EEPROM may contain some assembler code segments for the V8. These code segments are used as modification patches to override the original internal V8 software.

EEPROM Data Structure

The EEPROM contains the device descriptor, up to 4 configuration descriptors, and up to 15 string descriptors in up to 7 different languages. The following diagram specifies the block structure of the EEPROM data:

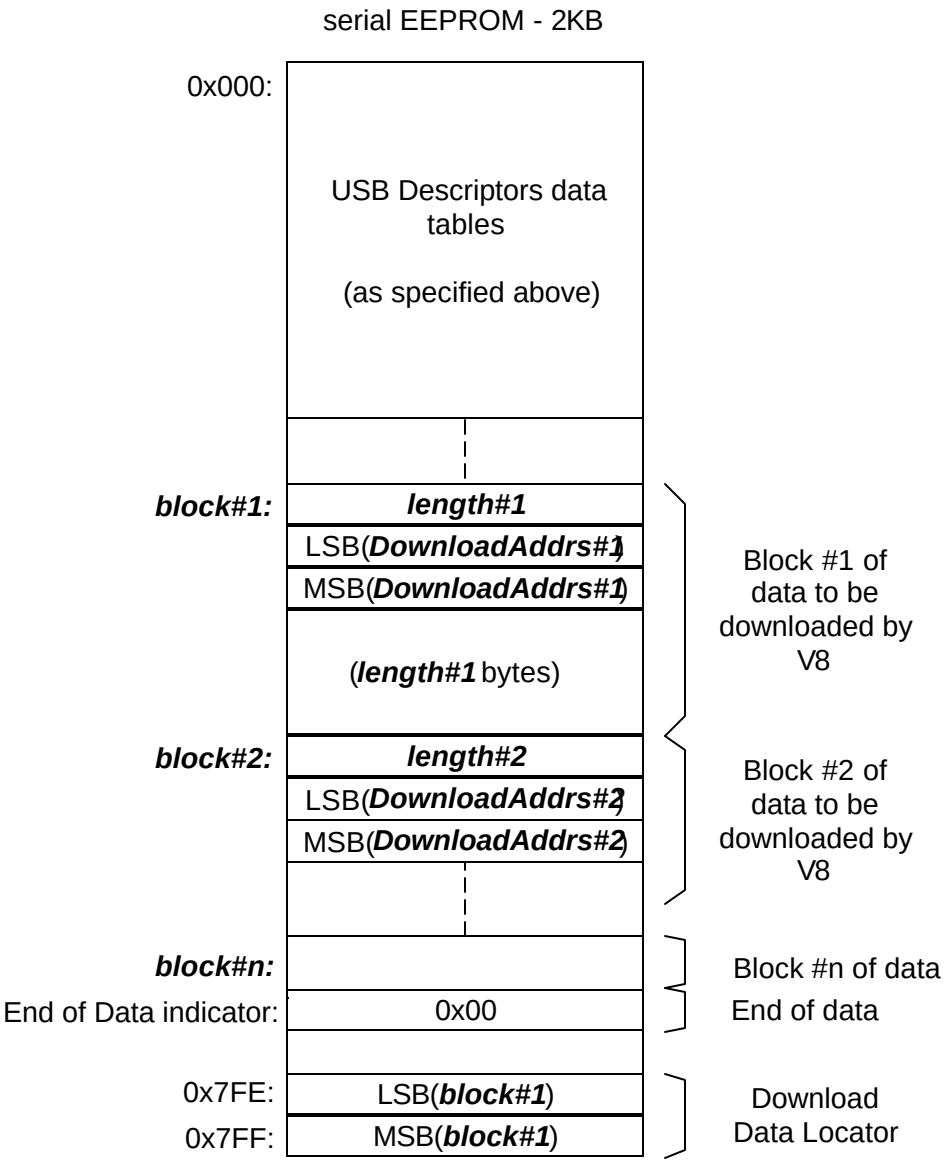


V8 Downloadable Code

The serial EEPROM in the ZR36506 application contains two files of data:

- USB descriptor data.
- Standalone mode application parameters and V8 downloadable data code.

Refer to the following diagram for EEPROM general data structure:



In order to download all data blocks from EEPROM, the V8 Software will perform the following steps:

1. Load two bytes from EEPROM to temporary space in SRAM, starting from EEPROM address 0x7FE. This 16-bit value – denoted by ***block#1*** - will be the Data Locator pointer.
2. Use the Data Locator pointer ***block#1*** to define the start address of the first data block to be downloaded. Read 3 bytes from this EEPROM address into a temporary space in SRAM. The first byte defines the total number of bytes in block#1 that should be downloaded, and is denoted by ***length#1.*** The other two bytes define a 16-bit start address in the V8 address space for the whole block to be downloaded to. This parameter is denoted by ***DownloadAddrs#1*** and normally points to some byte address in the internal SRAM.
3. Download ***length#1*** bytes from EEPROM address ***block#1*** +3 to given address ***DownloadAddrs#1*** in SRAM (or to any other destination in this address).
4. Repeat steps 2 and 3 to download all the other blocks from EEPROM to destination addresses. The address of the beginning of the new block always follows the end of the last block. End the download process if the first byte of the "new" block is 0x00 – which denotes End of Data.

Supported UNICODE Language Table:

This table is used as the "string" of index 0, which is defined in the USB-Standard. This "string" is actually a list of all the LANGIDs that are supported by the device. The first two bytes in this table are needed for the standard format of USB String descriptors.

EEPROM Address (Hex)	EEPROM Data (Hex)	Description
000	blength	Number of bytes in this table (4-16). This is needed for the standard format of USB String descriptors.
001	STRING descriptor type (=03)	Code of STRING descriptor type (=03). This is needed for the standard format of USB String descriptors.
002	LANGID#1 (LSB)	Bits 7-0 of Language-Identifier of language #1. This language must be supported, and it is also used as the default language if the host specifies a language that is not included in this list.
003	LANGID#1 (MSB)	Bits 15-8 of Language-Identifier of language #1.
004	LANGID#2 (LSB)	**Optional**. Bits 7-0 of Language-Identifier of language #2. Must contain FF if not used.

EEPROM Address (Hex)	EEPROM Data (Hex)	Description
005	LANGID#2 (MSB)	**Optional**.Bits 15-8 of Language-Identifier of language #2. Must contain FF if not used.
006	LANGID#3 (LSB)	**Optional**. Bits 7-0 of Language-Identifier of language #3. Must contain FF if not used.
007	LANGID#3 (MSB)	**Optional**.Bits 15-8 of Language-Identifier of language #3. Must contain FF if not used.
008	LANGID#4 (LSB)	**Optional**. Bits 7-0 of Language-Identifier of language #4. Must contain FF if not used.
009	LANGID#4 (MSB)	**Optional**.Bits 15-8 of Language-Identifier of language #4. Must contain FF if not used.
00A	LANGID#5 (LSB)	**Optional**. Bits 7-0 of Language-Identifier of language #5. Must contain FF if not used.
00B	LANGID#5 (MSB)	**Optional**.Bits 15-8 of Language-Identifier of language #5. Must contain FF if not used.
00C	LANGID#6 (LSB)	**Optional**. Bits 7-0 of Language-Identifier of language #6. Must contain FF if not used.
00D	LANGID#6 (MSB)	**Optional**.Bits 15-8 of Language-Identifier of language #6. Must contain FF if not used.
00E	LANGID#7 (LSB)	**Optional**. Bits 7-0 of Language-Identifier of language #7. Must contain FF if not used.
00F	LANGID#7 (MSB)	**Optional**.Bits 15-8 of Language-Identifier of language #7. Must contain FF if not used.

Table of Descriptor Pointers

This table is used by the ZR36506 to locate the start address of a given descriptor. Each item in this table consists of a Descriptor Identifier byte (first byte), and EEPROM address (second byte - contains only 8 most significant bits of address. The other 3 bits always equal '000').

EEPROM Address (Hex)	EEPROM Data (Hex)	Description
010	DDI (=40)	Device-Descriptor Identifier code (=40). This descriptor must exist in EEPROM.
011	DD address	Device-Descriptor address in this EEPROM (in this table, units are in 8-byte steps for address pointers).
012	CDI#0 (=20)	Configuration-Descriptor Identifier # 0 code (=20). This descriptor must exist in EEPROM. bits 7-2: '001000' (code of Configuration-Descriptor). bits 1-0: '00' (Configuration Index).
013	CD#0 address	Configuration-Descriptor #0 address.
	CDI#1 (=21)	**Optional**. Configuration-Descriptor Identifier # 1 code.
	CD#1 address	**Optional**. Configuration-Descriptor #1 address.
	CDI#2 (=22)	**Optional**. Configuration-Descriptor Identifier # 2 code.
	CD#2 address	**Optional**. Configuration-Descriptor #2 address.
	CDI#3 (=23)	**Optional**. Configuration-Descriptor Identifier # 3 code.
	CD#3 address	**Optional**. Configuration-Descriptor #3 address.
	SDI#1,0 (=90)	String-Descriptor Identifier Lang#1 Indx#0 (=90). This descriptor is actually the first table in EEPROM. bit 7: '1'. bits 6-4: '001' (Language number in language-table). bits 3-0: '0000' (String Index).

EEPROM Address (Hex)	EEPROM Data (Hex)	Description
	SDI#1,0 address (=00)	String-Descriptor #1,0 address (=00).
	SDI#2,0 (=A0)	String-Descriptor Identifier Lang#2 Indx#0 (=A0). This descriptor is actually the first table in EEPROM.
	SDI#2,0 address (=00)	String-Descriptor #1,0 address (=00).
	SDI#3,0 (=B0)	String-Descriptor Identifier Lang#3 Indx#0 (=B0). This descriptor is actually the first table in EEPROM.
	SDI#3,0 address (=00)	String-Descriptor #3,0 address (=00).
	SDI#4,0 (=C0)	String-Descriptor Identifier Lang#4 Indx#0 (=C0). This descriptor is actually the first table in EEPROM.
	SDI#4,0 address (=00)	String-Descriptor #4,0 address (=00).
	SDI#5,0 (=D0)	String-Descriptor Identifier Lang#5 Indx#0 (=D0). This descriptor is actually the first table in EEPROM.
	SDI#5,0 address (=00)	String-Descriptor #5,0 address (=00).
	SDI#6,0 (=E0)	String-Descriptor Identifier Lang#6 Indx#0 (=E0). This descriptor is actually the first table in EEPROM.
	SDI#6,0 address (=00)	String-Descriptor #6,0 address (=00).
	SDI#7,0 (=F0)	String-Descriptor Identifier Lang#7 Indx#0 (=F0). This descriptor is actually the first table in EEPROM.
	SDI#7,0 address (=00)	String-Descriptor #7,0 address (=00).

EEPROM Address (Hex)	EEPROM Data (Hex)	Description
	SDI#n1,m1	**Optional**. String-Descriptor Identifier Lang#n1 Indx#m1. bit 7: '1.' bits 6-4: n1 (Language number in language-table). bits 3-0: m1 (String Index).
	SDI#n1,m1 address	**Optional**. String-Descriptor #n1,m1 address.
	SDI#n2,m2	**Optional**. String-Descriptor Identifier Lang#n2 Indx#m2.
	SDI#n2,m2 address	**Optional**. String-Descriptor #n1,m1 address.
	SDI#nk,mk	**Optional**. String-Descriptor Identifier Lang#nk Indx#mk.
	SDI#nk,mk address	**Optional**. String-Descriptor #nk,mk address.
	EOT (=00)	End-Of-Table code (=00).

Table of Descriptors

This table contains the DEVICE descriptor, all CONFIGURATION descriptors, and all STRING descriptors. DEVICE and STRING descriptors are organized exactly as specified in the USB standard. CONFIGURATION descriptors start with a word (= 2 bytes - LSB first, then MSB) that specifies the number of total bytes in the descriptor (excluding the first 2 bytes), followed by the descriptor's body, which is organized exactly as specified in the USB standard.

- **The Supported Unicode Languages Table is also used as STRING descriptor #0 for all languages.**
- **There is one and only one DEVICE descriptor, which is always 18 bytes long.**
- **A descriptor always starts at an 8*k address of the EEPROM (the 3 least significant bits of the address are '000'). This means that there can be up to 7 unused bytes between any two descriptors in the table.**

EEPROM Access Registers

EEPROM access via the ZR36506 registers is enabled when the E2_EN bit in the PWR_REG register is set. The following registers are used for EEPROM access:

Parameter	Register Address	Usage
E2_EN	Reg.0/d7 E2_EN	Enable EEPROM access. 0: Default after Reset. EEPROM access disabled. 1: Enable EEPROM Read and Write(1) .
EE_DATA [7..0]	Reg.14 EE_DATA	Data Byte to be written to EEPROM. Also, last Data Byte that was read from EEPROM.
EE_LSBAD [7..0]	Reg.15 EE_LSBAD	8 Least Significant bits of byte address in EEPROM to be accessed.
EE_MSBAD [10..8]	Reg.16/d2-d0	3 Most Significant bits of byte address in EEPROM to be accessed.
EE_DIR	Reg.16/d3 EE_DIR	Select EEPROM access direction: 0: Select Write operation to EEPROM. 1: Select Read operation from EEPROM.
EE_GO/EE_BUSY	Reg.16/d4 EE_GO/ EE_BUSY	This is used as both a command and a status bit. Writing '1' to this bit will initiate a byte Read or Write. The EE_GO/EE_BUSY bit will remain '1' till the end of operation, to indicate to the host computer when a EEPROM access can begin.

- **A Write operation to the EEPROM requires the EEPROM WP pin to be grounded.**
- **A Write operation requires additional 10 milliseconds in the EEPROM internal circuits.**

EEPROM Control Signals

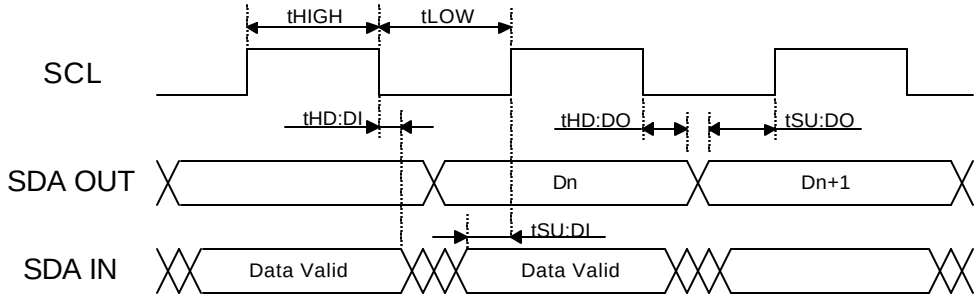
The SCL/PWR0 and SDA pins of the ZR36506 are the EEPROM control signals. The SCL/PWR0 is used as the clock output, and the SDA signal is used as the data I/O.

If an external EEPROM does not exist (EEPROM = '0'), the ZR36506 automatically uses its internal ROM for USB descriptors. In this case, the ZR36506 relates to hard-coding of the pins SCL/PWR0 and PWR1 to determine the current-consumption parameter for the configuration descriptor. The following table summarizes these two modes of operation:

Internal ROM Mode	External EEPROM Mode
EEPROM pin connected to GND. SCL/PWR0 and PWR1 pins are hard-coded to determine device current consumption for Configuration-Descriptor: PWR1 SCL/PWR0 Current 0 0 200mA 0 1 300mA 1 0 400mA 1 1 500mA	EEPROM pin connected to 10 Kbyte Pull-Up resistor (3.3 V to 5.0 V). External Serial 2 K * 8 EEPROM is connected: SDA/EEPROM connected to Serial-Data (SDA). SCL/PWR0 connected to Serial-Clock (SCL).

The following timing diagrams and table specify the EEPROM control waveforms that the ZR36506 generates:

Start/Stop Timings



Data Timings

Symbol	Parameter	Min	Max	Unit
$t_{SU:STA}$	START condition setup time	5300	-	ns
$t_{HD:STA}$	START condition hold time	5300	-	ns
$t_{SU:STO}$	STOP condition setup time	5300	-	ns
t_{HIGH}	Clock high time	5300	-	ns
t_{LOW}	Clock low time	5300	-	ns
$t_{SU:DO}$	Data output setup time	2500	2670	ns
$t_{HD:DO}$	Data output hold time	2500	2670	ns
$t_{SU:DI}$	Data input setup time	20	-	ns
$t_{HD:DI}$	Data input hold time	0	-	ns

12 ZR36506 USB AND STATUS REGISTERS

The ZR36506 has some registers that allow the software driver to directly read and affect some USB device parameters. These are specified in the following table:

Parameter	Register Address	Usage
CONFIG_REG	Reg.1 CONFIG_ REG	Read Only register. Contains the Device Configuration number.
ADRS_REG	Reg.2/d6-d0 ADRS_REG	Read Only register. Contains the Device Address.
ALTER_REG	Reg.3/d3-d0 ALTER_REG	Read Only register. Contains the Alternate setting for End-Point #2 (video bandwidth). Regarding this value as a binary number in the range [1,15], the number of bytes sent in the Isochronous pipe of EP2 in every millisecond is: N = (16-ALTER_REG)*64 - 1 USB Bandwidth = (16-ALTER_REG)*0.5 Mbit/sec
NEW_ALT	Reg.4/d3-d0 FORCE_ALTE R_REG	New Alternate setting for End-Point #2, (video bandwidth), to replace the original setting. This can be used to lower the actual used bandwidth temporarily, without notifying the Operating System.
FORCE_ALT	Reg.4/d7 FORCE_ALTE R_REG	Force New Alternate. 0: Use original setting. 1: Select NEW_ALT value.
VFRM_BLNK	Reg.5/d0 STATUS_REG	Read Only register. 0: Valid region of input video frame. 1: Blank or unused region of input video frame. .

Parameter	Register Address	Usage
EE_CLK_FORCE [2..0]	Reg.16/d7-d5 EE_CONT	Read Only register. These 3 bits reflect the logical level of the following pins of the ZR36506: EE_CLK_FORCE [0] = SCL/PWR0 pin. EE_CLK_FORCE [1] = PWR1 pin. EE_CLK_FORCE [2] = SDA pin.
WD_EN & WD_COUNT[7..0]	Reg.0/d0 Reg.53/d7-d0	Some USB host controllers may start an Isochronous IN transaction too long after the SOF (Start of USB Frame point). This means that long IN transactions may exceed the 1 mS time interval of the USB frame, and cause the USB host controller to disconnect the device. The ZR36506 uses an internal Watch Dog timer to eliminate such problems. The Watch Dog operates if the WD_EN control bit is set to '1'. It then starts to count 686 uS after the SOF pattern, and terminates any Isochronous transaction automatically when reaching the value of the WD_COUNT register. Every one count is equivalent to 1.33 uS. Note that the value of WD_COUNT should be no more than 0xE9 in order to take any effect.

13 PROGRAMMABLE I/O PINS AND 48 MHZ OUTPUT PIN

The ZR36506 has two programmable I/O pins for general purpose usage. These are IO-1 and IO-2 pins, which are Open-Drain.

Each of these pins - if used - must be connected to an external Pull-Up resistor to 3.3-5.0 V (if not used, it can be tied to GND). The external Pull-Up resistor should be in the range of 1-10 KΩ.

To use these pins as inputs, the host computer should write '1' to the appropriate bit in the IOPIN_REG register (in the ZR36506 register bank) - these are the IO_1 and IO_2 bits, respectively. In this condition, the voltage level presented on the IO-1 or IO-2 pin may be read by the host computer via the appropriate bit ('0' represents <0.8 V, '1' represents > 2.0 V).

To use these pins as outputs, the host computer should write the output value to the appropriate bit in the IOPIN_REG register; In this condition, and assuming that no external device forces the voltage level presented on the IO-1 or IO-2 pin, the written value will be reflected ('0' will generate 0 V, '1' will generate 3.3-5.0 V).

Upon a Power On Reset or a USB-Reset operation, the IO-1 and IO-2 pins are cleared to '0'. In Suspend mode, these pins are temporarily set to High-z.

The ZR36506 provides a 48 MHz clock output for SDRAM interface and general purpose usage. The pin CLK48 is dedicated to this, and is enabled when the CLK48_EN bit is set to '1' (Reg.0/d3). When disabled, the output level in this pin is constant '0'.

The 48 MHz output is 50% duty cycle with 1 nS jitter, and is derived from the external 12 MHz crystal (an internal analog PLL is used).

14 AUDIO CHANNEL

The audio channel in the ZR36506 is based on a serial 64 – 512 Kbit/s data stream from the ZR36506 to the host computer (USB Isochronous mode is used for this stream). The 64 – 512 Kbit/s stream comes from an 8,000 / 16,000 S/sec 16 / 8-bit audio sample at the external audio Codec(s). Two external Codecs should be used for Stereo mode recordings. The 8 / 16 KHz sampling clock is derived from the 12 MHz external crystal.

The ZR36506 pins for the external Codec interface are BCLK, FS_L, FS_R, and DAT_IN.

The following table specifies the AUDIO_CONT register (Register address = 50):

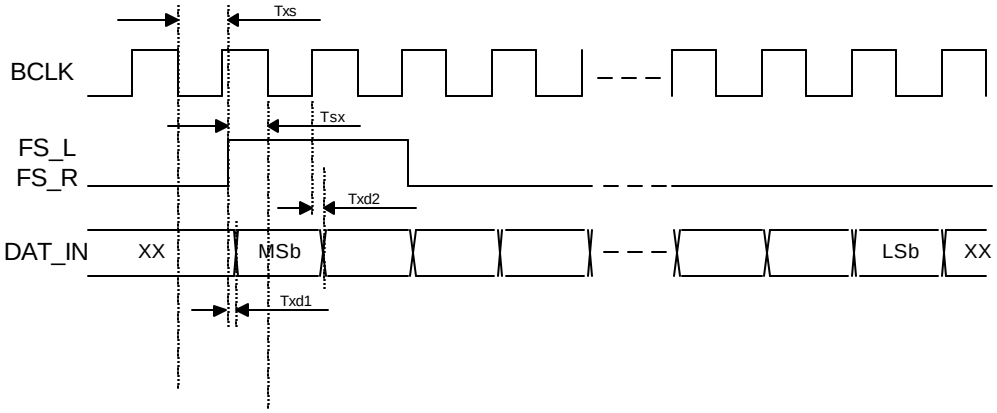
Bit #	Name	Description	
0	E_A	'0':	Disables Audio channel. Set FS_L and FS_R outputs to constant '0'. If E_B is also '0', BCLK is set to constant '0'.
		'1':	Enable Audio channel.
1	E_B	'0':	Disable Bulk Data input. Set BLK_FULL output to constant '0'. If E_A is also '0', BCLK is set to constant '0'.
		'1':	Enable Bulk Data input.
3-2	BPS	'00':	8-bit per sample.
		'01':	12-bit per sample (Occupies 2 bytes. Bits d3-d0 of second byte are set to '0000').
		'10':	14-bit per sample (Occupies 2 bytes. Bits d1-d0 of second byte are set to '00').
		'11':	16-bit per sample.
4	S/M	'0':	Selects Mono mode. FS_L output is active, FS_R output is constant '0'.
		'1':	Selects Stereo mode. Both FS_L and FS_R outputs are active.
5	FS	'0':	Set sampling rate to 8,000 Samp/Sec.
		'1':	Set sampling rate to 16,000 Samp/Sec.
7-6	BK	'00':	BCLK frequency is not defined.
		'01':	Select BCLK frequency = 64 KHz.
		'10':	Select BCLK frequency = 1.544 MHz.
		'11':	Select BCLK frequency = 2.048 MHz.

In addition to the AUDIO_CONT register, there is the AUD_PK_LEN register (Register address = 51), to select the maximum packet size to be sent via the audio Isochronous pipe. This number is limited to 128, which is the maximum number of bytes that the ZR36506 audio FIFO can contain. The software driver should set this register to a value that fits the USB descriptor for the EP#3 maximum packet length (which is 66, if not using an external EEPROM).

Codec Interface

The Codec Interface is Long Frame Sync Timing based. The BCLK frequency may be selected to be – 2048 KHz, 1536 KHz, or 64 KHz, which enables the designer to use almost any family of low cost Codecs available on the market.

In the Long Frame Sync Timing modes, the MSb of the "transmitted" data is always expected soon after the rising edge of the FS_L (or FS_R) signal. The ZR36506 produces a positive pulse of 2 BCLK cycles in these output pins every 125 us (8 KHz) or every 62.5 us (16 KHz), which indicates the start of sample as specified in the following waveform diagram:



The BCLK is derived from the 12 MHz clock on the crystal. This results in a 4.3% jitter at the BCLK signal.

The following table specifies the minimum and maximum time intervals for the Codec Interface waveform diagram:

Parameter	Symbol	Min	Max	Unit
Hold Time from BCLK Low to FS_L / FS_R High	Txs	180	-	ns
Setup Time from FS_L / FS_R High to BCLK Low	Tsx	180	-	ns
Delay Time to valid data from FS_L / FS_R	Txd1	-	200	ns
Delay Time from BCLK High to DAT_IN valid	Txd2	-	200	ns
Jitter at the Bit Clock signal BCLK	Cj	-	4.3	%

15 BULK CHANNEL

The Bulk channel in the ZR36506 is capable of transferring serial data from an external source to the host computer at a bit rate of up to 2 Mbits/sec. It uses a bulk end point (E.P#4), with a maximum packet length that may be specified by a value of 1 - 64 bytes (the USB standard does not allow a bulk packet of more than 64 bytes).

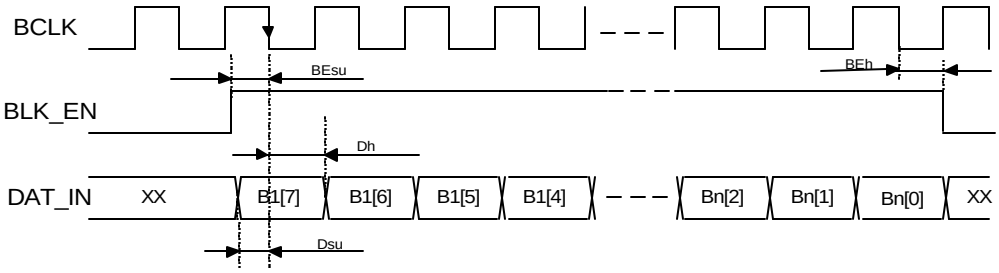
The Bulk channel takes advantage of the existing interface for the audio codec. In order to work simultaneously with the audio channel, the external data source should be able to stop the data transfer from time to time - as specified in the Bulk waveform diagram.

The ZR36506 pins for the Bulk channel interface are BCLK, DAT_IN, BLK_EN, and BLK_FULL. The signals FS_L and FS_R should be monitored by the data source logic, in order to coexist with the audio channel.

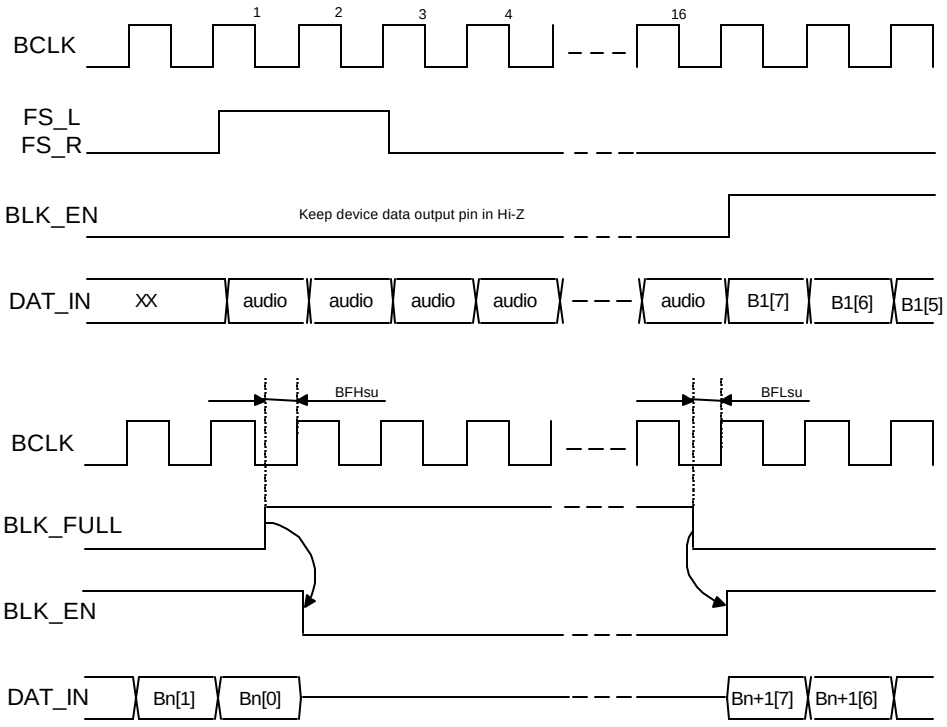
The following table specifies the control registers that are used for controlling the Bulk channel:

Control Name	Description
E_B Reg.50/d1	'0': Disable Bulk Data input. Set BLK_FULL output to constant '0'. If E_A is also '0', BCLK is set to constant '0'. '1': Enable Bulk Data input.
BLK_PK_LEN [6..0] Reg.52/d6-d0	This register specifies the maximum number of bytes to be sent in a single USB Bulk packet. This must be a number between 0 and 64, and should fit the content of the USB descriptor (64 if no external EEPROM used). This register directly affects the bit rate capability of the Bulk channel. The actual bit rate is also limited by the BCLK frequency, which may be 64 KHz, 1544 KHz, or 2048 KHz. A bit rate of 2 Mbits/sec may be reached only on computers that are capable of performing more than one packet in a USB frame (OHCI).

The following waveform diagram specifies the procedure and timings for the ZR36506 Bulk interface. Note that the input data is sampled on the falling edge of the BCLK clock signal. The BLK_EN input is set to '1' by the sending device to indicate the beginning of a byte sequence; it should always turn to '1' before the most significant bit of the first byte, and return to '0' after the least significant bit of the last byte in sequence. When the BLK_FULL output of the ZR36506 turns '1', the sending device should wait (by switching BLK_EN to '0') until the BLK_FULL indication returns to '0'.



If the audio channel is enabled, the sending device should wait at least 16 clock cycles after the FS_L (or FS_R) pulse before beginning to send its own data. During this time it should keep its data out signal in the High-z state, so as not to interfere with the audio data.



Parameter	Symbol	Min	Max	Unit
Setup Time from BLK_EN High to BCLK Low	BEsu	100	-	ns
Hold Time from BCLK Low to BLK_EN Low	BEh	100	-	ns
Setup Time from DAT_IN valid to BCLK Low	Dsu	100	-	ns
Hold Time from BCLK Low to DAT_IN valid	Dh	100	-	ns
Setup Time from BLK_FULL High to BCLK High	BFHsu	80	-	ns
Hold Time from BLK_FULL Low to BCLK High	BFLsu	0	-	ns
Jitter at the Bit Clock signal BCLK	Cj	-	4.3	%

16 SERIAL PIPE OUT INTERFACE

Description

The Serial Pipe Out (SPO) interface is used for compressed video and audio data transfer to external devices. This interface is used in Standalone mode (when not connected to USB)

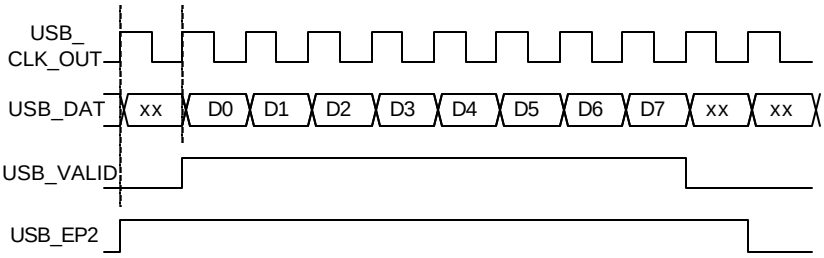
The SPO consists of the following signals:

Pin #	Pin Name	I/O	Description
11	USB_CLK_OUT	O	12 MHz clock for bit sampling.
10	USB_DAT	O	Serial data output. This signal carries both compressed video and PCM audio signals.
9	USB_VALID	O	Data-Valid signal. '1' indicates that data is valid. '0' indicates "ignore data signal". Switch from '0' to '1' indicates beginning of a new byte.
8	USB_EP2	O	Video Data Select signal. '1' indicates video data region.
7	USB_EP3	O	Audio Data Select signal. '1' indicates Audio data region.
29	IO1	I	Video Data Request. '1' means external device is ready to receive more data. '0' means external device cannot receive more data now.

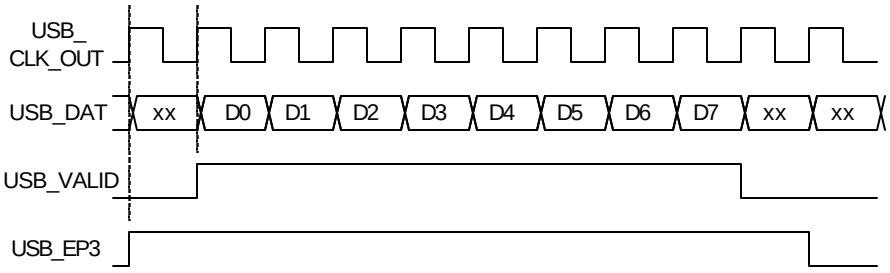
Video and audio data are byte-oriented and always begin with the LSbit. The signal USB_VALID always returns to '0' between every two subsequent bytes, hence it can be used for byte synchronization.

The signals USB_EP2 and USB_EP3 indicate whether the data belong to the video or audio streams respectively. The signal USB_EP2 can also indicate the end of a video frame and the beginning of the next one. Refer to the waveform diagrams for this indication.

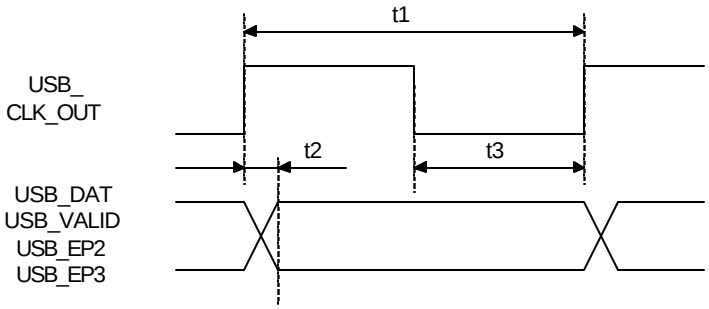
Video Data Output



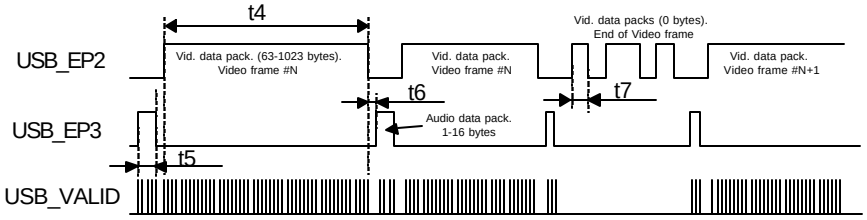
Audio Data Output



General Timing 1

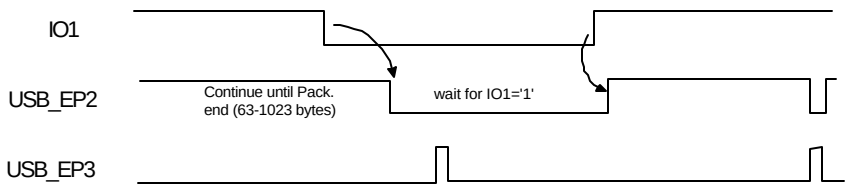


General Timing 2



Note: One or more empty packets of video type must occur after every video frame

General Timing 3



Timing Table

Name	Min	Typical	Max	Unit
t1	78	83	88	[ns]
t2	5	7	10	[ns]
t3	37	42	47	[ns]
t4	10	1000	2000	[us]
t5	1	8	16	[us]
t6	200	800	-	[ns]
t7	200	800	1500	[ns]

17 SOFTWARE PACKAGE

Listed below is a description of the software components provided with the ZR36506.

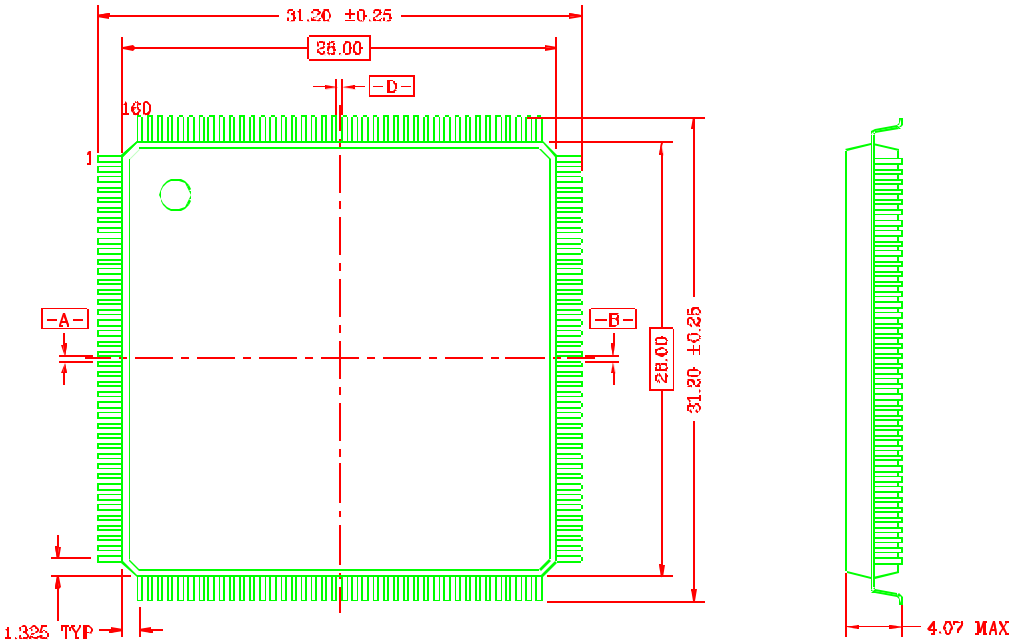
- **WDM Video streaming class MiniDriver**
  - MS® standard connection and streaming in kernel mode (Capture, Still)
  - MS® standard property sets (TV Tuner, Crossbar)
  - MS® standard way of exposing data formats.
  - MS® standard way of controlling stream flow.

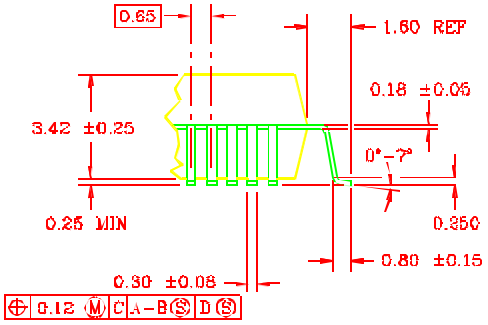
All interfaces are exposed through the DirectShow architecture. VFW interfaces are also available via a WDM to VFW mapper, provided by Microsoft.

- **WDM Audio streaming class MiniDriver**- streams audio data from the ZR36506 chip.
- **TWAIN Compliant Drivers** - The package includes a TWAIN compliant driver for high resolution still image capture. The GUI of the TWAIN driver displays a live video preview. The package also includes a TWAIN compliant driver for Digital Camera support.
- **EEPROM Programming Application** - An application for programming the ZR36506 EEPROM to contain vendor specific USB Descriptors. It allows the setting of the device and manufacturer names as well as the serial number for the device.

The drivers are supplied with an INF file for easy installation. Customization is applied by modifying the name strings in the INF file.

18 MECHANICAL SPECIFICATIONS





DETAIL -A-

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS.
2. LEADFRAME MATERIAL: COPPER.
3. LEAD FINISH: SOLDER PLATE.

160 METRIC QUAD FLAT PACK 1.60 mm
DWG No: 25-90019 REV: *B

19 CONTACT INFORMATION

USA
Zoran Corporation
3112 Scott Boulevard,
Santa Clara, CA 95054-3317

Tel.: +1-408-919-4111
Fax: +1-408-919-4122

CHINA
Zoran China Office
Suite 2507
Electronics Science &
Tech Building
2070 Central Shennan Rd.
Shenzhen, Guangdong,
518031 P.R. China

Tel.: +86-755-378-0319
Fax: +86-755-378-0852

TAIWAN
Zoran Taiwan Office
4F-1, No. 5, Alley 22
Lane 513, Reikuang Rd.
Taipei, Taiwan R.O.C.

Tel.: +886-2-2659-9797
Fax: +886-2-2659-9595

WEB
http://www.zoran.com

ISRAEL
Zoran Microelectronics Ltd.
Advanced Technology Ctr.
P.O. Box 2495
Haifa, 31024 Israel

Tel.: +972-4-8545-777
Fax: +972-4-8551-551

JAPAN
Zoran Japan Office
2-2-8 Roppongi, Minato-ku
Tokyo 106-0032, Japan

Tel.: +81-03-5574-7081
Fax: +81-03-5574-7156

CANADA
Zoran Toronto Lab
2175 Queen St. East,
Suite 302
Toronto, Ontario
M4E 1E5 Canada

Tel.: +1-416-690-3356
Fax: +1-416-690-3363

http://www.nogatech.com