

FEATURES

- 3.3V and 5V power supply options
- 250ps propagation delay
- High bandwidth output transitions
- Internal 75K Ω input pull-down resistors
- Replaces SY10/100EL16
- Improved output waveform characteristics
- ESD protection of 2000V
- Available in 8-pin SOIC and TSSOP package

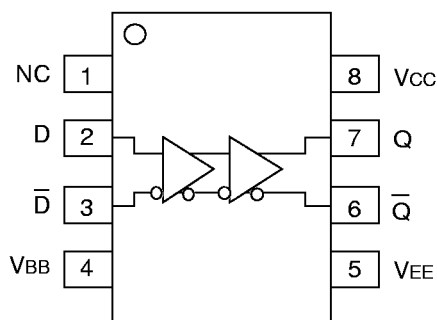
DESCRIPTION

The SY10/100EL16V are differential receivers. The devices are functionally equivalent to the E116 devices, with higher performance capabilities. With output transition times significantly faster than the E116, the EL16V is ideally suited for interfacing with high-frequency sources.

The EL16V provides a VBB output for either single-ended use or as a DC bias for AC coupling to the device. The VBB pin should be used only as a bias for the EL16V as its current sink/source capability is limited. Whenever used, the VBB pin should be bypassed to ground via a 0.01 μ f capacitor.

Under open input conditions (pulled to VEE), internal input clamps will force the Q output LOW.

PIN CONFIGURATION/BLOCK DIAGRAM



(Available in 8-pin SOIC or 8-pin TSSOP)

TOP VIEW

PIN NAMES

Pin	Function
D	Data Inputs
Q	Data Outputs
VBB	Reference Voltage Output

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE} \text{ (Min.) to } V_{EE} \text{ (Max.)}$; $V_{CC} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I _{EE}	Power Supply Current													mA
	10EL	—	18	22	9	18	22	9	18	22	9	18	22	
	100EL	—	18	22	9	18	22	9	18	22	9	21	26	
V _{BB}	Output Reference Voltage													V
	10EL	-1.43	—	-1.30	-1.38	—	-1.27	-1.35	—	-1.25	-1.31	—	-1.19	
	100EL	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.26	
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	μA

NOTE:

- Parametric values specified at: 10/100EL16V Series: -3.0V to -5.5V.

AC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_{EE} = V_{EE} \text{ (Min.) to } V_{EE} \text{ (Max.)}$; $V_{CC} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t _{PLH}	Propagation Delay to Output													ps
t _{PHL}	D (Diff)	125	250	375	175	250	325	175	250	325	205	280	355	
	D (SE)	75	250	425	125	250	375	125	250	375	155	280	405	
t _{skew}	Duty Cycle Skew ⁽²⁾ (Diff)	—	5	—	—	5	20	—	5	20	—	5	20	ps
V _{PP}	Minimum Input Swing ⁽³⁾	150	—	—	150	—	—	150	—	—	150	—	—	mV
V _{CMR}	Common Mode Range ⁽⁴⁾	-1.3	—	-0.4	-1.4	—	-0.4	-1.4	—	-0.4	-1.4	—	-0.4	V
t _r	Output Rise/Fall Times Q	100	225	350	100	225	350	100	225	350	100	225	350	ps
t _f	(20% to 80%)													

NOTES:

- Parametric values specified at: 10/100EL16V Series: -3.0V to -5.5V.
- Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
- Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.
- The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = -3.3V. Note for PECL operation, the V_{CMR} (min) will be fixed at 3.3V - |V_{CMR} (min)|.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	V _{EE} Range (V)
SY10EL16VKCTR	K8-1	Commercial	-3.0 to -5.5
SY100EL16VKCTR	K8-1	Commercial	-3.0 to -5.5
SY10EL16VZC	Z8-1	Commercial	-3.0 to -5.5
SY10EL16VZCTR	Z8-1	Commercial	-3.0 to -5.5
SY100EL16VZC	Z8-1	Commercial	-3.0 to -5.5
SY100EL16VZCTR	Z8-1	Commercial	-3.0 to -5.5

8 LEAD TSSOP (K8-1)

FILE/REV #: PD0052A01

PD/0052/ASCORP

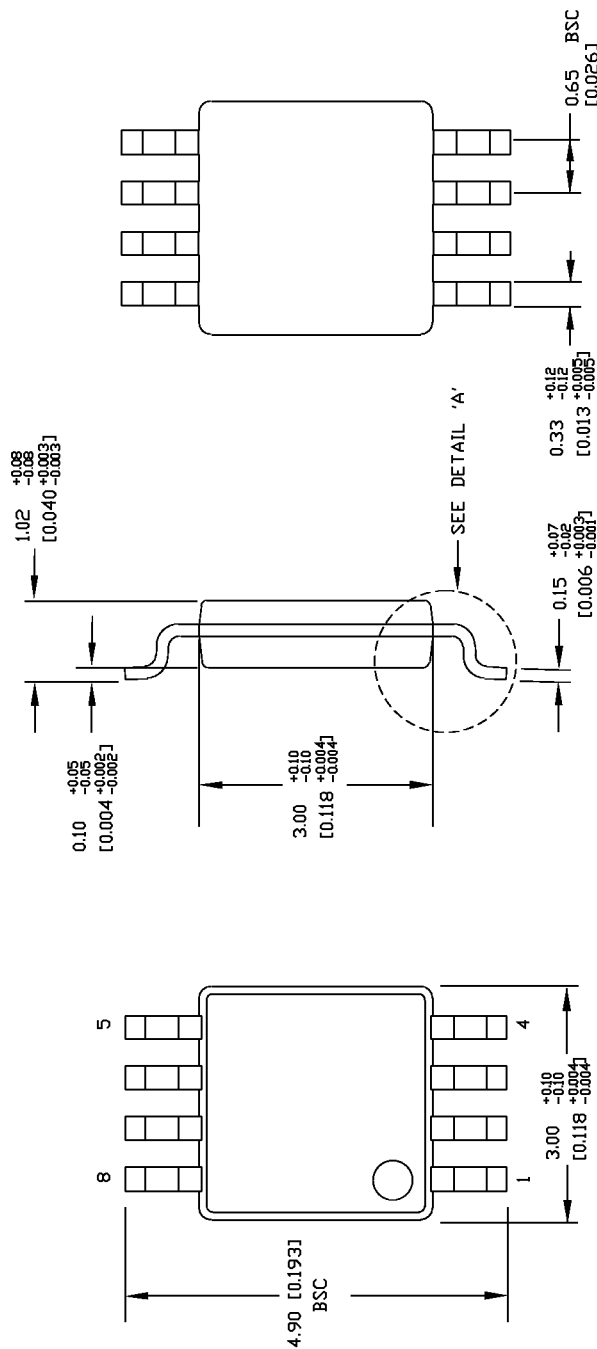
PAGE 1 OF 1

REV	REVISION DESCRIPTION	DATE
00	NEW OUTLINE DRAWING	07/14/97
01	CONVERT DWG. TO AUTOCAD REL. 13 AND ONE PAGE DOCUMENT 02/09/98	

TOP VIEW

END VIEW

BOTTOM VIEW



NOTES:

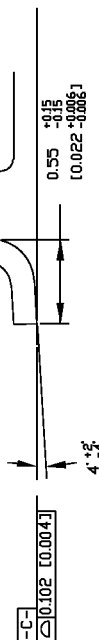
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.



3250 SCOTT BOULEVARD
SANTA CLARA, CA. 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	8 LEAD TSSOP (3MM X 3MM BODY)
ORIGINATOR: FERMIN G. URRUTIA	02/23/88	QUALITY: WILDER		A	PACKAGE OUTLINE
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					
					SCALE N/A
					REVISION 01

DETAIL A



8 LEAD PLASTIC SOIC (Z8-1)

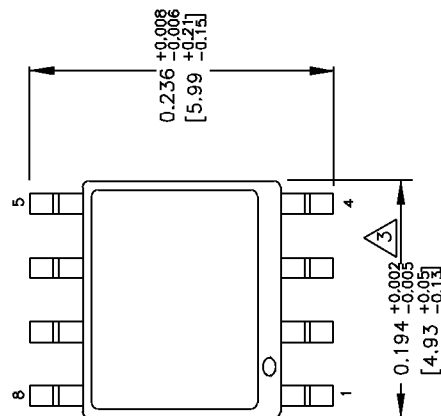
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PD/0032/ASCORP

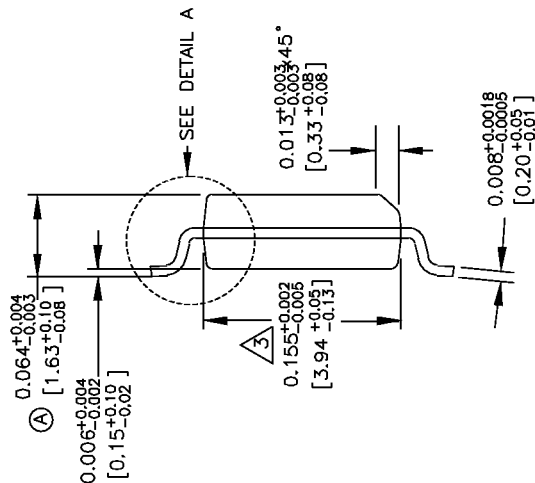
PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
00	NEW OUTLINE DRAWING.	07/20/94
01	CONVERT TO AUTOCAD. REFERENCE AMKOR DWG. NO. 00019 REV.05. MAKE (A) SAME AS JEDEC.	12/14/95
02	ADDED LEAD WIDTH AND PITCH DIMENSIONS. CORRECTED TYPES.	03/12/97
03	CONVERT DWG TO REL13 AND ONE PAGE DOCUMENT.	02/20/98

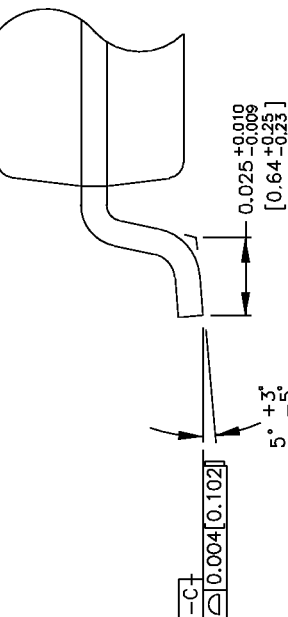
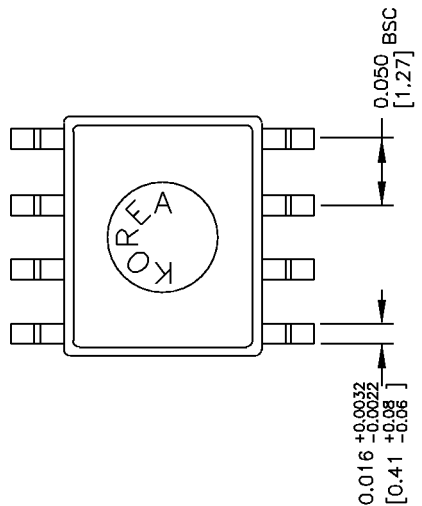
TOP VIEW



END VIEW



BOTTOM VIEW



DETAIL A

NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

SYNERGY
SEMICONDUCTOR

3250 SCOTT BOULEVARD
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APPROVALS	DATE	APPROVALS	DATE	SIZE	8 LEAD PLASTIC SOIC (.150"WIDE)
ORIGINATOR:	02/23/98	QUALITY:		A	PACKAGE OUTLINE
CHK'D:		DOCUMENT CONTROL:			
NON CHANG		BRIAN SANFILIPPO			
RELEASE DATE:					

SCALE	REVISION
N/A	Q3

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