

FEATURES

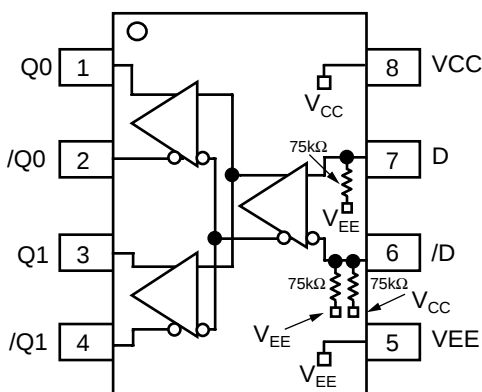
- 2.5V, 3.3V and 5V power supply options
- Guaranteed AC parameters over temperature:
 - $f_{MAX} > 3.0\text{GHz}$
 - $< 20\text{ps}$ output-to-output skew
 - $< 200\text{ps}$ t_r / t_f
 - $< 300\text{ps}$ propagation delay
- Wide temperature range: -40°C to $+85^\circ\text{C}$
- Available in 8-pin (3mm) MSOP and SOIC packages

DESCRIPTION

The SY10/100EP11U is a precision, high-speed 1:2 differential fanout buffer. Having within-device skews and output transition times significantly improved over the EL11V, the EP11U is ideally suited for those applications which require the ultimate in AC performance.

The differential inputs of the EP11U employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open (pulled to V_{EE}), the Q outputs will go LOW.

PIN CONFIGURATION/BLOCK DIAGRAM



8-pin MSOP and SOIC Packages

PIN NAMES

Pin	Function
D	PECL, LVPECL, ECL, LVECL Clock or Data Input: Internal 75kΩ pulldown resistor. If left floating, pin defaults LOW, Q_{OUT} goes LOW.
/D	PECL, LVPECL, ECL, LVECL complementary Clock or Data Input: Internal 75kΩ pull-up and down resistors. If left open, default is $V_{CC}/2$. When the input is not used, it can be left open.
Q0, /Q0 Q1, /Q1	PECL, LVPECL, ECL, LVECL Outputs: Terminates to $V_{CC} - 2V$.
V_{CC}	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors.
V_{EE}	Negative Power Supply: For PECL operation, connect to GND.

CROSS REFERENCE TABLE

Micrel Semiconductor	ON Semiconductor
SY10EP11UZI/KI	MC10EP11D/DT
SY10EP11UZI/KI	MC10LVEP11D/DT
SY100EP11UZI/KI	MC100EP11D/DT
SY100EP11UZI/KI	MC100LVEP11D/DT

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
$V_{CC} - V_{EE}$	Power Supply Voltage	6V	V
V_{IN}	Input Voltage ($V_{CC} = 0V$, V_{IN} not more negative than V_{EE}) Input Voltage ($V_{EE} = 0V$, V_{IN} not more positive than V_{CC})	-6.0 to 0 +6.0 to 0	V V
I_{OUT}	Output Current -Continuous -Surge	50 100	mA
T_A	Operating Temperature Range	-40 to +85	°C
T_{store}	Storage Temperature Range	-65 to +150	°C
θ_{JA}	Package Thermal Resistance (Junction-to-Ambient) -Still-Air (SOIC) -500lfpm (SOIC) -Still-Air (MSOP) -500lfpm (MSOP)	160 109 206 155	°C/W °C/W
θ_{JC}	Package Thermal Resistance (Junction-to-Case) (SOIC) (MSOP)	39 39	°C/W

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Power Supply Voltage (PECL) (LVPECL) (ECL) (LVECL)	4.5 2.37 -5.5 -3.8	5.0 — -5.0 -3.3	5.5 3.8 -4.5 -2.37	4.5 2.37 -5.5 -3.8	5.0 — -5.0 -3.3	5.5 3.8 -4.5 -2.37	4.5 2.37 -5.5 -3.8	5.0 — -5.0 -3.3	5.5 3.8 -4.5 -2.37	V	
I_{EE}	Power Supply Current SY10EP11U SY100EP11U	— —	— —	37 44	— —	25 30	39 44	— —	— —	40 44	mA mA	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	$V_{IN} = V_{IH}$
I_{IL}	Input LOW Current D /D	0.5 -150	— —	— —	0.5 -150	— —	— —	0.5 -150	— —	— —	μA μA	$V_{IN} = V_{IL}$ $V_{IN} = V_{IL}$
C_{IN}	Input Capacitance (MSOP) (SOIC)	— —	— —	— —	— —	0.75 1.1	— —	— —	— —	— —	pF pF	

NOTES:

1. 10/100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

(10KEP) LVPECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾ $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{OL}	Output LOW Voltage	565	690	815	630	755	880	690	815	940	mV	50Ω to $V_{CC}-2V$
V_{OH}	Output HIGH Voltage	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV	50Ω to $V_{CC}-2V$
V_{IHCMR}	Input HIGH Voltage ⁽²⁾ Common Mode Range	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	

NOTES:

- 10KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at $V_{CC} = 2.5V$. They vary 1:1 with V_{CC} .
- The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single-ended input CLK pin operation is limited to $V_{CC} \geq 3.0V$ in PECL mode.

(10KEP) LVPECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾ $V_{CC} = 3.3V \pm 10\%$, $V_{EE} = 0V$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	1365	—	1690	1430	—	1755	1490	—	1815	mV	
V_{IH}	Input HIGH Voltage (Single-Ended)	2090	—	2415	2155	—	2480	2215	—	2540	mV	
V_{OL}	Output LOW Voltage	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV	50Ω to $V_{CC}-2V$
V_{OH}	Output HIGH Voltage	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV	50Ω to $V_{CC}-2V$
V_{IHCMR}	Input HIGH Voltage ⁽²⁾ Common Mode Range	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	

NOTES:

- 10KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at $V_{CC} = 3.3V$. They vary 1:1 with V_{CC} .
- The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single-ended input CLK pin operation is limited to $V_{CC} \geq 3.0V$ in PECL mode.

(10KEP) PECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾ $V_{CC} = 5.0V \pm 10\%$, $V_{EE} = 0V$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	3065	—	3390	3130	—	3455	3190	—	3515	mV	
V_{IH}	Input HIGH Voltage (Single-Ended)	3790	—	4115	3855	—	4180	3915	—	4240	mV	
V_{OL}	Output LOW Voltage	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV	50Ω to $V_{CC}-2V$
V_{OH}	Output HIGH Voltage	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV	50Ω to $V_{CC}-2V$
V_{IHCMR}	Input HIGH Voltage ⁽²⁾ Common Mode Range	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	

NOTES:

- 10KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at $V_{CC} = 5.0V$. They vary 1:1 with V_{CC} .
- The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single-ended input CLK pin operation is limited to $V_{CC} \geq 3.0V$ in PECL mode.

(10KEP) ECL/LVECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾ $V_{CC} = 0V$, $V_{EE} = -5.5V$ to $-2.375V$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	-1935	—	-1610	-1870	—	-1545	-1810	—	-1485	mV	
V_{IH}	Input HIGH Voltage (Single-Ended)	-1210	—	-885	-1145	—	-820	-1085	—	-760	mV	
V_{OL}	Output LOW Voltage	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV	50Ω to $V_{CC}-2V$
V_{OH}	Output HIGH Voltage	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV	50Ω to $V_{CC}-2V$
V_{IHCMR}	Input HIGH Voltage ⁽²⁾ Common Mode Range	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	V	

NOTES:

- 10KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
- The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single-ended input CLK pin operation is limited to $V_{EE} \leq -3.0V$ in ECL/LVECL mode.

(100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾ $V_{CC} = 2.5V \pm 5\%$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{OL}	Output LOW Voltage	555	680	805	555	680	805	555	680	805	mV	50Ω to $V_{CC}-2V$
V_{OH}	Output HIGH Voltage	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV	50Ω to $V_{CC}-2V$
V_{IHCMR}	Input HIGH Voltage ⁽²⁾ Common Mode Range	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	

NOTES:

- 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at $V_{CC} = 2.5V$. They vary 1:1 with V_{CC} .
- The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single-ended input CLK pin operation is limited to $V_{CC} \geq 3.0V$ in PECL mode.

(100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾ $V_{CC} = 3.3V \pm 10\%$, $V_{EE} = 0V$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	1355	—	1675	1355	—	1675	1355	—	1675	mV	
V_{IH}	Input HIGH Voltage (Single-Ended)	2075	—	2420	2075	—	2420	2075	—	2420	mV	
V_{OL}	Output LOW Voltage	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV	50Ω to $V_{CC}-2V$
V_{OH}	Output HIGH Voltage	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV	50Ω to $V_{CC}-2V$
V_{IHCMR}	Input HIGH Voltage ⁽²⁾ Common Mode Range	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	

NOTES:

- 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at $V_{CC} = 3.3V$. They vary 1:1 with V_{CC} .
- The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single-ended input CLK pin operation is limited to $V_{CC} \geq 3.0V$ in PECL mode.

(100KEP) PECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾ $V_{CC} = 5.0V \pm 10\%$, $V_{EE} = 0V$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	3055	—	3375	3055	—	3375	3055	—	3375	mV	
V_{IH}	Input HIGH Voltage (Single-Ended)	3775	—	4120	3775	—	4120	3775	—	4120	mV	
V_{OL}	Output LOW Voltage	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV	50Ω to $V_{CC}-2V$
V_{OH}	Output HIGH Voltage	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV	50Ω to $V_{CC}-2V$
V_{IHCMR}	Input HIGH Voltage ⁽²⁾ Common Mode Range	2.0	—	V_{CC}	2.0	—	V_{CC}	2.0	—	V_{CC}	V	

NOTES:

- 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at $V_{CC} = 5.0V$. They vary 1:1 with V_{CC} .
- The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single-ended input CLK pin operation is limited to $V_{CC} \geq 3.0V$ in PECL mode.

(100KEP) ECL/LVECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾ $V_{CC} = 0V$, $V_{EE} = -5.5V$ to $-2.375V$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV	
V_{IH}	Input HIGH Voltage	-1225	—	-880	-1225	—	-880	-1225	—	-880	mV	
V_{OL}	Output LOW Voltage	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV	50Ω to $V_{CC}-2V$
V_{OH}	Output HIGH Voltage	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV	50Ω to $V_{CC}-2V$
V_{IHCMR}	Input HIGH Voltage ⁽²⁾ Common Mode Range	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	V	

NOTES:

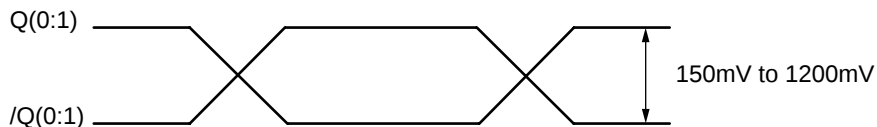
- 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
- The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single-ended input CLK pin operation is limited to $V_{EE} \leq 3.0V$ in ECL/LVECL mode.

AC ELECTRICAL CHARACTERISTICS
 $V_{CC} = 0V$; $V_{EE} = -5.5V$ to $-2.375V$ or $V_{CC} = 2.375V$ to $5.5V$, $V_{EE} = 0V$

Symbol	Parameter	$T_A = -40^{\circ}C$			$T_A = +25^{\circ}C$			$T_A = +85^{\circ}C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Toggle Frequency ⁽¹⁾	3	—	—	3	—	—	3	—	—	GHz	
t_{PLH} t_{PHL}	Propagation Delay (Differential) D to Q, /Q D to Q, /Q	140 170	200 230	250 300	160 180	220 240	270 310	180 210	240 270	300 360	ps ps	$V_{CC} = 3.3V/5V$ $V_{CC} = 2.5V$
t_{SKEW}	Within-Device Skew ⁽²⁾ Q, /Q	—	5	20	—	5	20	—	5	20	ps	
	Part-to-Part Skew ⁽²⁾	— —	— —	130 110	— —	— —	130 110	— —	— —	150 120	ps ps	$V_{CC} = 3.3V/5V$ $V_{CC} = 2.5V$
t_{JITTER}	Cycle-to-Cycle Jitter (rms)	—	0.2	< 1	—	0.2	< 1	—	0.2	< 1	ps _{rms}	
V_{PP}	Minimum Input Swing ⁽³⁾	150	800	1200	150	800	1200	150	800	1200	mV	
t_r, t_f	Output Rise/Fall Time (20% to 80%)	70	110	170	80	120	180	100	140	200	ps	

NOTES:

1. Measured with 750mV input signal, 50% duty cycle. All loading with a 50Ω to $V_{CC} - 2.0V$.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
3. See "Timing Waveform."

TIMING WAVEFORM

TERMINATION RECOMMENDATIONS

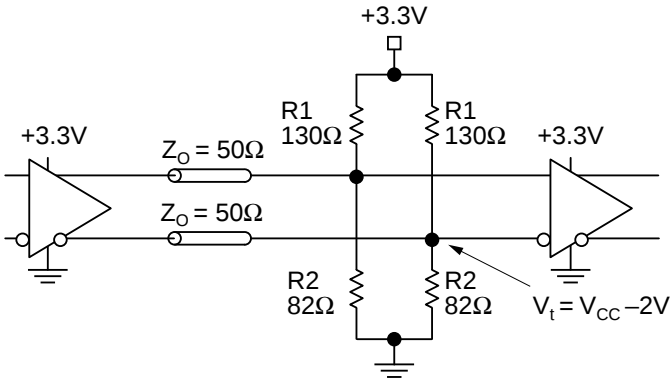


Figure 1. Parallel Termination-Thevenin Equivalent

Notes:

- 1. For +2.5V systems:
R1 = 250Ω
R2 = 62.5Ω
- 2. For +5.0V systems:
R1 = 82Ω
R2 = 130Ω

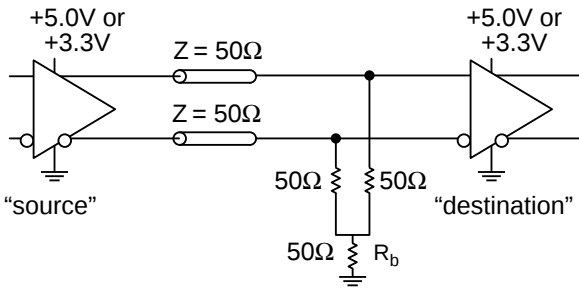


Figure 2. Three-Resistor "Y-Termination"

Notes:

- 1. Power-saving alternative to Thevenin termination.
- 2. Place termination resistors as close to destination inputs as possible.
- 3. R_b resistor sets the DC bias voltage equal to V_t. For +3.3V systems R_b = 46Ω to 50Ω. For +5V systems, R_b = 110Ω.

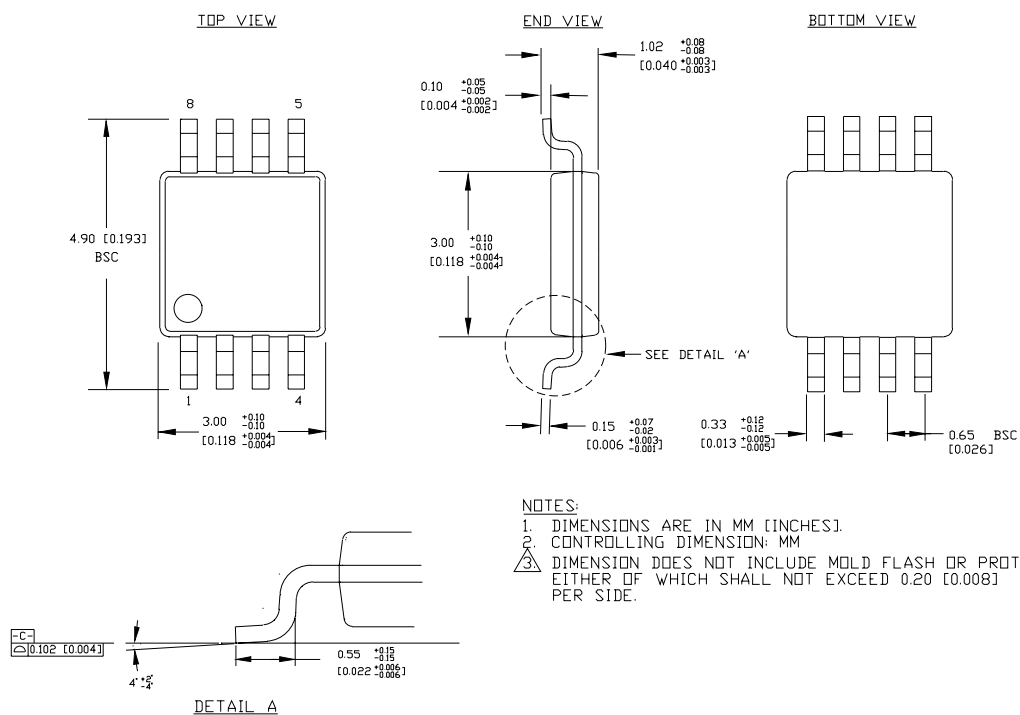
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	Package Marking
SY10EP11UKI	K8-1	Industrial	HP11
SY10EP11UKITR*	K8-1	Industrial	HP11
SY10EP11UZI	Z8-1	Industrial	HEP11U
SY10EP11UZITR*	Z8-1	Industrial	HEP11U

Ordering Code	Package Type	Operating Range	Package Marking
SY100EP11UKI	K8-1	Industrial	XP11
SY100EP11UKITR*	K8-1	Industrial	XP11
SY100EP11UZI	Z8-1	Industrial	XEP11U
SY100EP11UZITR*	Z8-1	Industrial	XEP11U

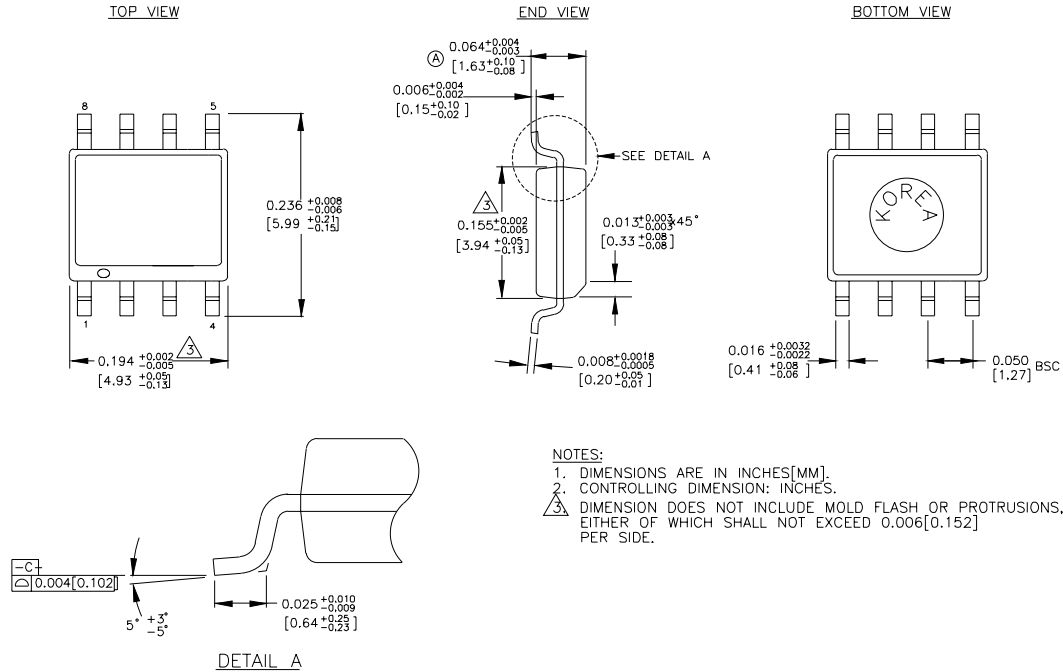
*Tape and Reel

8 LEAD MSOP (K8-1)



Rev. 01

8 LEAD SOIC .150" WIDE (Z8-1)



Rev. 03

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