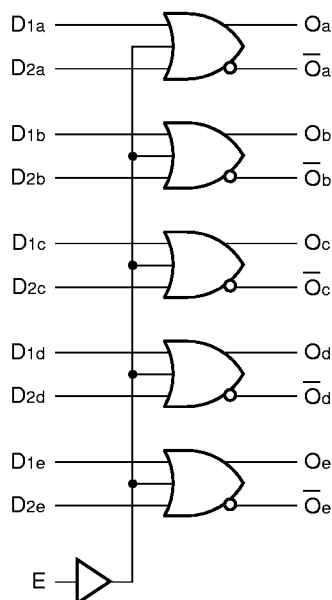


FEATURES

- Max. propagation delay of 700ps
- IEE min. of -45mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 50% faster than National 300K
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin Cerdip, 24-pin CERPACK and 28-pin PLCC packages

BLOCK DIAGRAM



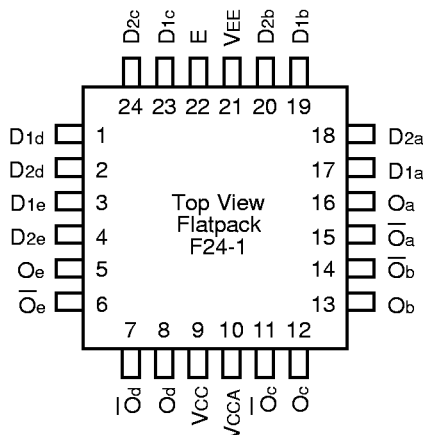
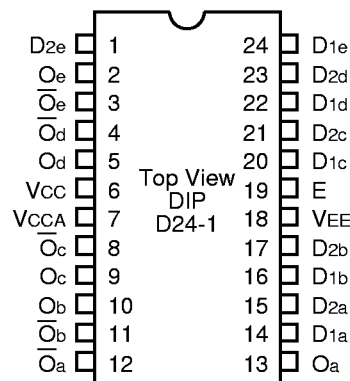
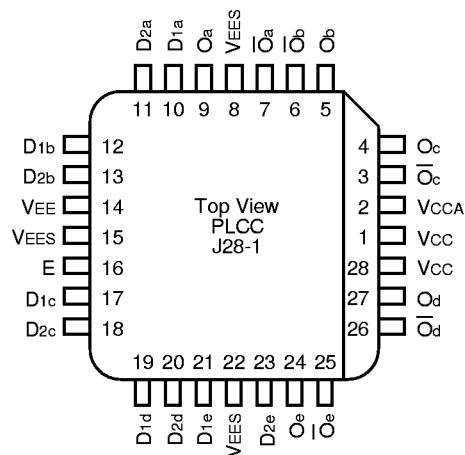
PIN NAMES

Pin	Function
D _{na} – D _{ne}	Data Inputs (n-1...5)
E	Enable Input
O _a – O _e	Data Outputs
$\overline{O}_a$ – $\overline{O}_e$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

DESCRIPTION

The SY100S302 offers five 2-input OR/NOR gates designed for use in high-performance ECL systems. The five gates are controlled by a common Enable signal. All inputs have 75KΩ pull-down resistors and all outputs are buffered.

PIN CONFIGURATIONS



TRUTH TABLE⁽¹⁾

D1X	D2X	E	OX	$\overline{OX}$
L	L	L	L	H
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

NOTE:

1. H = High Voltage Level
L = Low Voltage Level

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	μA	$V_{IN} = V_{IH} (Max.)$
I_{EE}	Power Supply Current	-45	-28	-21	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	800	300	800	300	800	ps	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	300	1100	300	1100	300	1100	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	300	750	300	750	300	750	ps	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	250	950	250	950	250	950	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

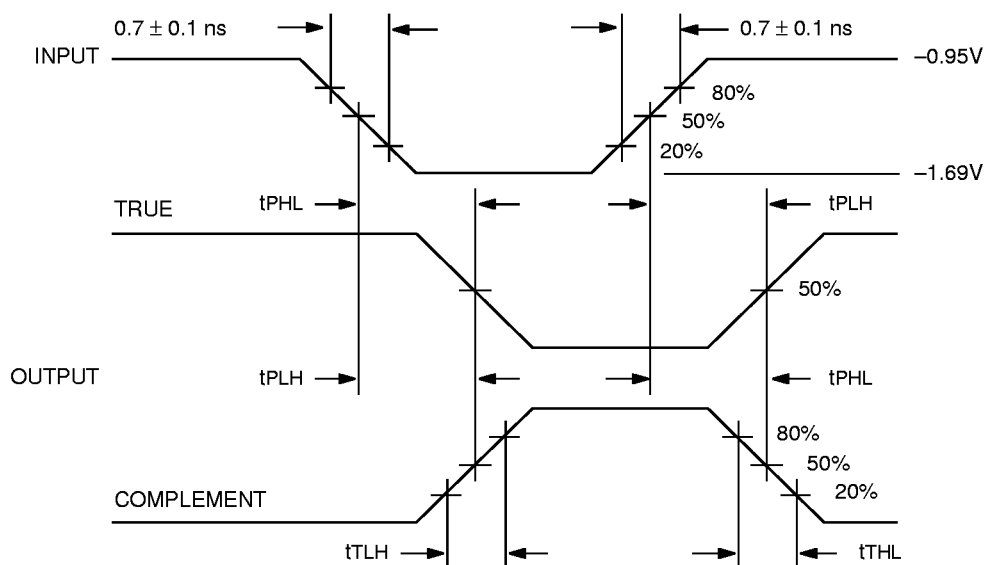
AC ELECTRICAL CHARACTERISTICS (CONT'D.)

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	250	700	250	700	250	700	ps	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	250	900	250	900	250	900	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



Propagation Delay and Transition Times

NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

PRODUCT ORDERING CODE

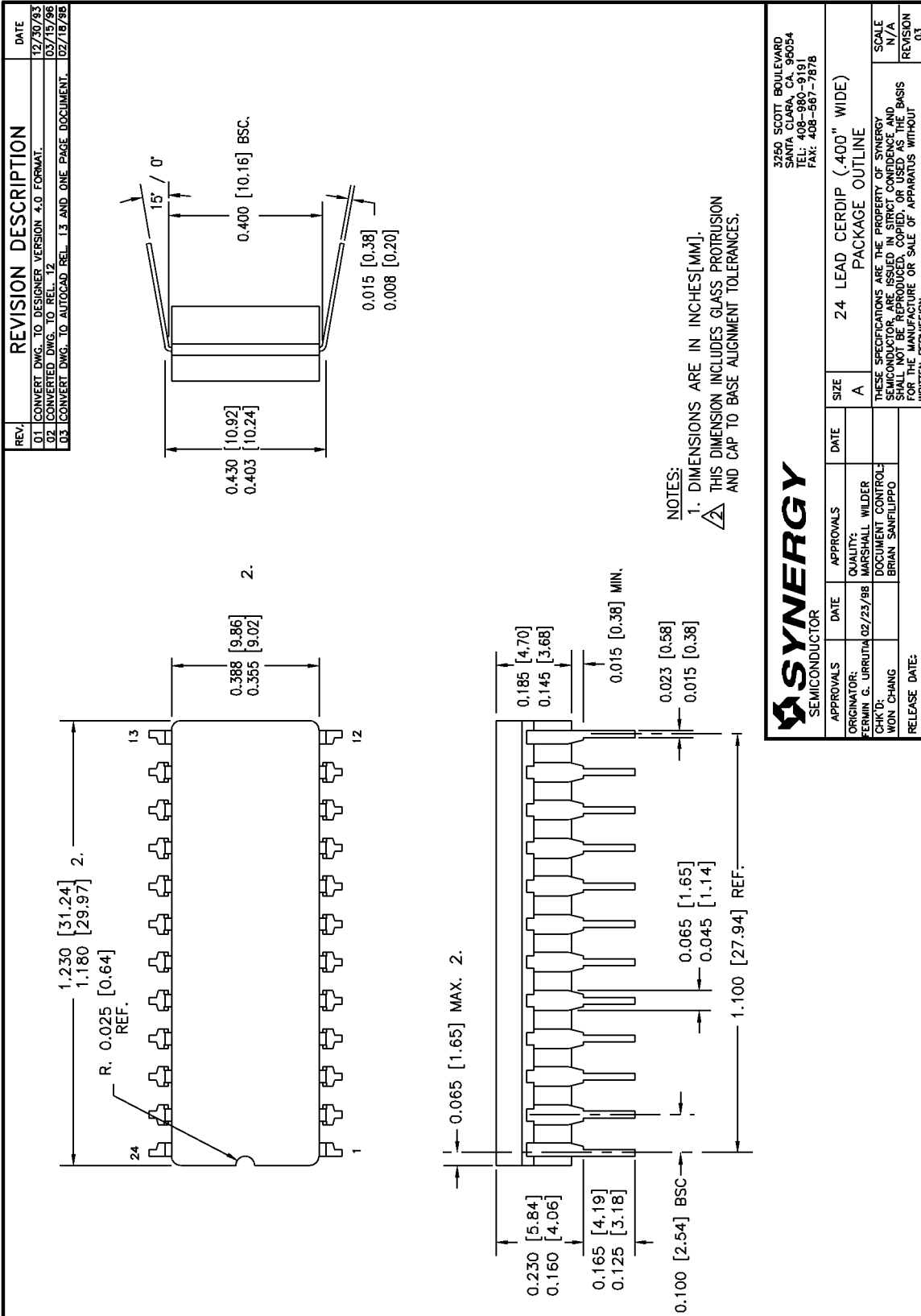
Ordering Code	Package Type	Operating Range
SY100S302DC	D24-1	Commercial
SY100S302FC	F24-1	Commercial
SY100S302JC	J28-1	Commercial
SY100S302JCTR	J28-1	Commercial

24 LEAD CERPDP (D24-1)

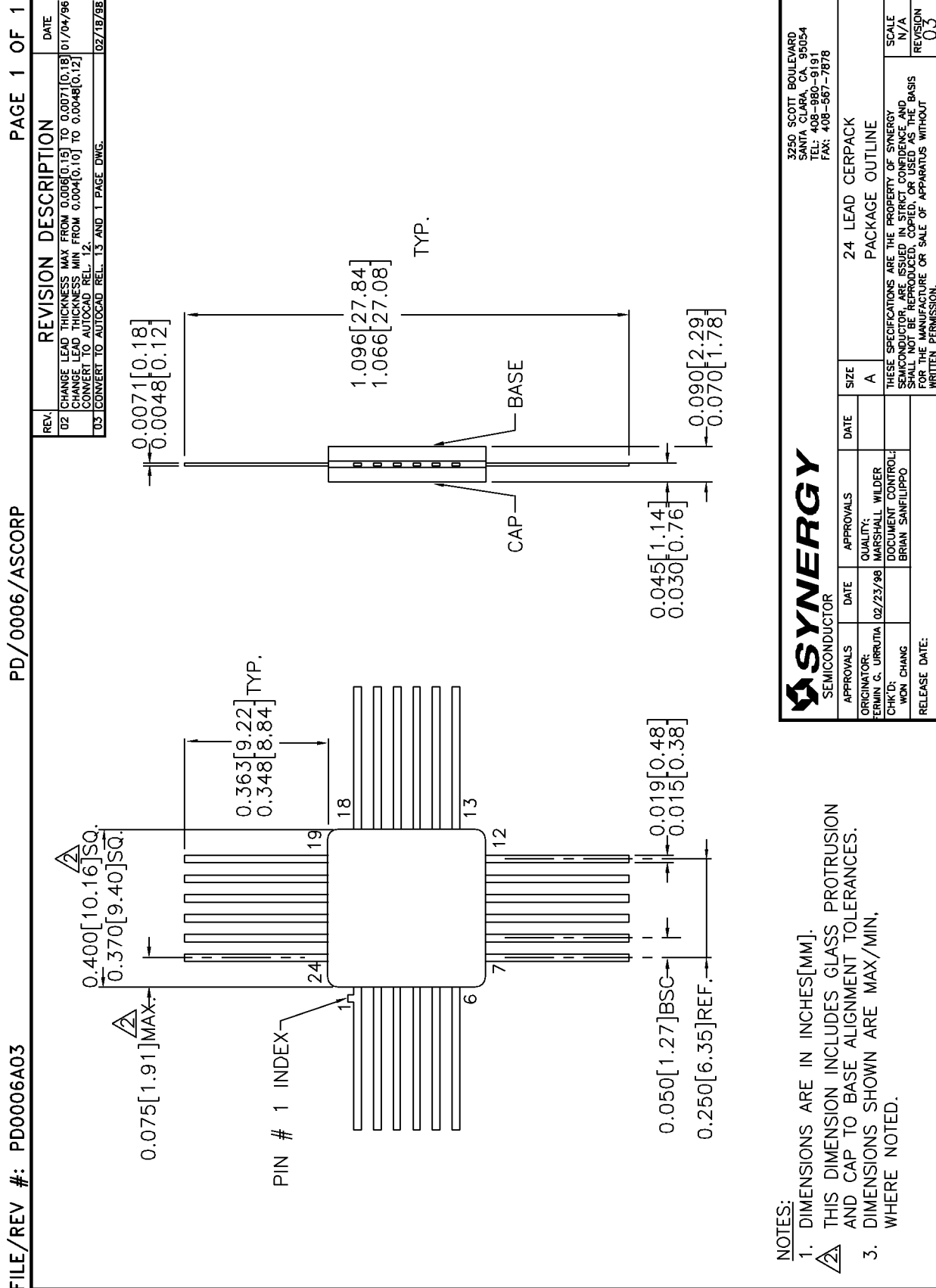
FILE/REV #: PD0003A03

PD/0003/ASCORP

PAGE 1 OF 1



24 LEAD CERPACK (F24-1)



28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

FILE/REV #: PD0008A03

PD/0008/ASCORP

PAGE 1 OF 1

