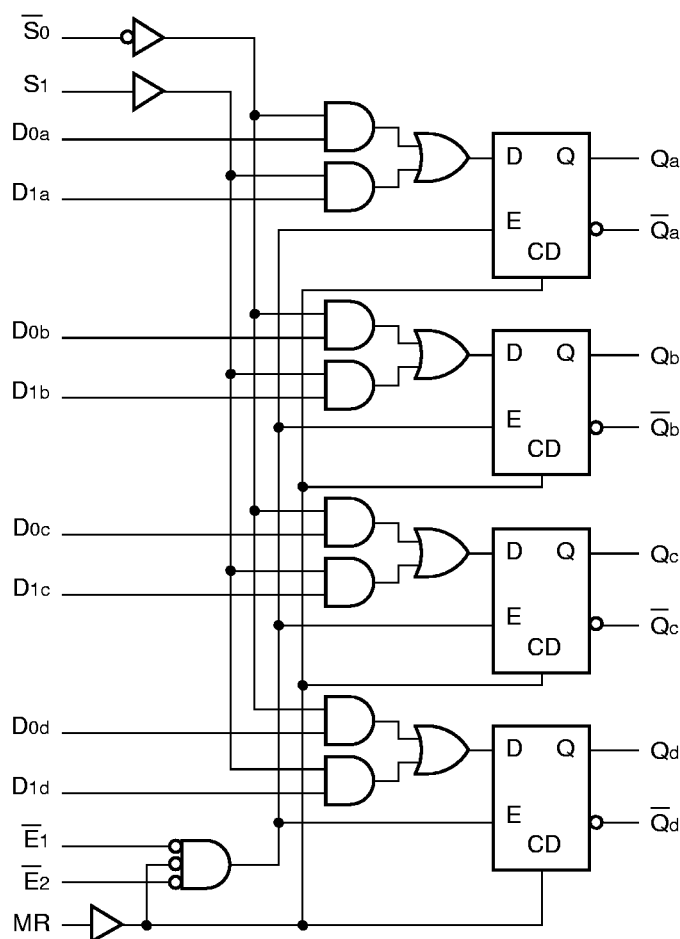


FEATURES

- Max. propagation delay of 1100ps
- Max. enable to output delay of 1400ps
- IEE min. of -80mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75K Ω input pull-down resistors
- 50% faster than National or Signetics
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin CERPDP, 24-pin CERPAC and 28-pin PLCC packages

BLOCK DIAGRAM

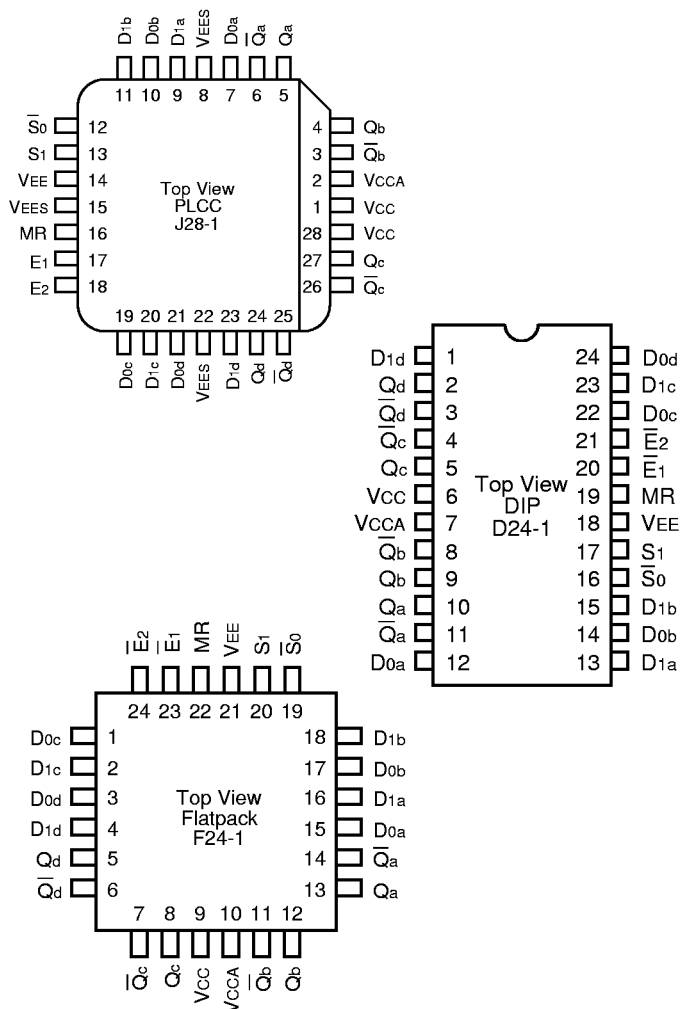


DESCRIPTION

The SY100S355 offers four transparent latches with differential outputs and is designed for use in high-performance ECL systems. The Select inputs ($\bar{S}_0$, S_1) select one of the two sources of input data (D_0 or D_1) to the latch. The Select inputs can also force the outputs to a logic LOW when the latch is in the transparent mode. The latches are in the transparent mode when both Enables ($\bar{E}_1$, $\bar{E}_2$) are at a logic LOW state. In the transparent mode, the Select inputs can pass an input logic HIGH from D_0 or D_1 to the output.

If the Select inputs are tied together, then input data from either D_0 or D_1 is always passed through. A rising edge on either Enable input will latch the outputs with the most recent data at the latch inputs being stored. The Master Reset (MR) input overrides all other inputs and takes the Q outputs to a logic LOW. The inputs on this device have 75K Ω pull-down resistors.

PIN CONFIGURATIONS



PIN NAMES

Pin	Function
$\bar{E}_1 - \bar{E}_2$	Enable Inputs (Active LOW)
$\bar{S}_0, S_1$	Select Inputs
MR	Master Reset
$D_{na} - D_{nd}$	Data Inputs
$Q_a - Q_d$	Data Outputs
$\bar{Q}_a - \bar{Q}_d$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

TRUTH TABLE⁽¹⁾

Inputs							Outputs	
MR	$\bar{E}_1$	$\bar{E}_2$	S_1	$\bar{S}_0$	D_{1x}	D_{0x}	$\bar{Q}_x$	Q_x
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched	
L	X	H	X	X	X	X	Latched	

NOTE:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care

DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
IIH	Input HIGH Current				μA	$V_{IN} = V_{IH} \text{ (Max.)}$
	$\bar{S}_0, S_1$	—	—	220		
	$\bar{E}_1, \bar{E}_2$	—	—	350		
	D_{na}, D_{nd}	—	—	340		
	MR	—	—	430		
IEE	Power Supply Current	-80	-57	-40	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay Dna – Dnd to Output (Transparent Mode)	400	1300	400	1300	400	1300	ps	
tPLH tPHL	Propagation Delay S0, S1 to Output (Transparent Mode)	400	1600	400	1600	400	1600	ps	
tPLH tPHL	Propagation Delay E1, E2 to Output	300	1200	300	1200	300	1200	ps	
tPLH tPHL	Propagation Delay MR to Output	300	1600	300	1600	300	1600	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
ts	Set-up Time Dna – Dnd S0, S1 MR (Release Time)	700 1200 1000	— — —	700 1200 1000	— — —	700 1200 1000	— — —	ps	
th	Hold Time Dna – Dnd S0, S1	400 400	— —	400 400	— —	400 400	— —	ps	
tpw (L)	Pulse Width LOW, E1, E2	1000	—	1000	—	1000	—	ps	
tpw (H)	Pulse Width HIGH, MR	1000	—	1000	—	1000	—	ps	

CERPACK

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay Dna – Dnd to Output (Transparent Mode)	300	1200	300	1200	300	1200	ps	
tPLH tPHL	Propagation Delay S0, S1 to Output (Transparent Mode)	300	1500	300	1500	300	1500	ps	
tPLH tPHL	Propagation Delay E1, E2 to Output	300	1500	300	1500	300	1500	ps	
tPLH tPHL	Propagation Delay MR to Output	300	1200	300	1200	300	1200	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
ts	Set-up Time Dna – Dnd S0, S1 MR (Release Time)	700 1200 1000	— — —	700 1200 1000	— — —	700 1200 1000	— — —	ps	
th	Hold Time Dna – Dnd S0, S1	400 400	— —	400 400	— —	400 400	— —	ps	
tpw (L)	Pulse Width LOW, E1, E2	1000	—	1000	—	1000	—	ps	
tpw (H)	Pulse Width HIGH, MR	1000	—	1000	—	1000	—	ps	

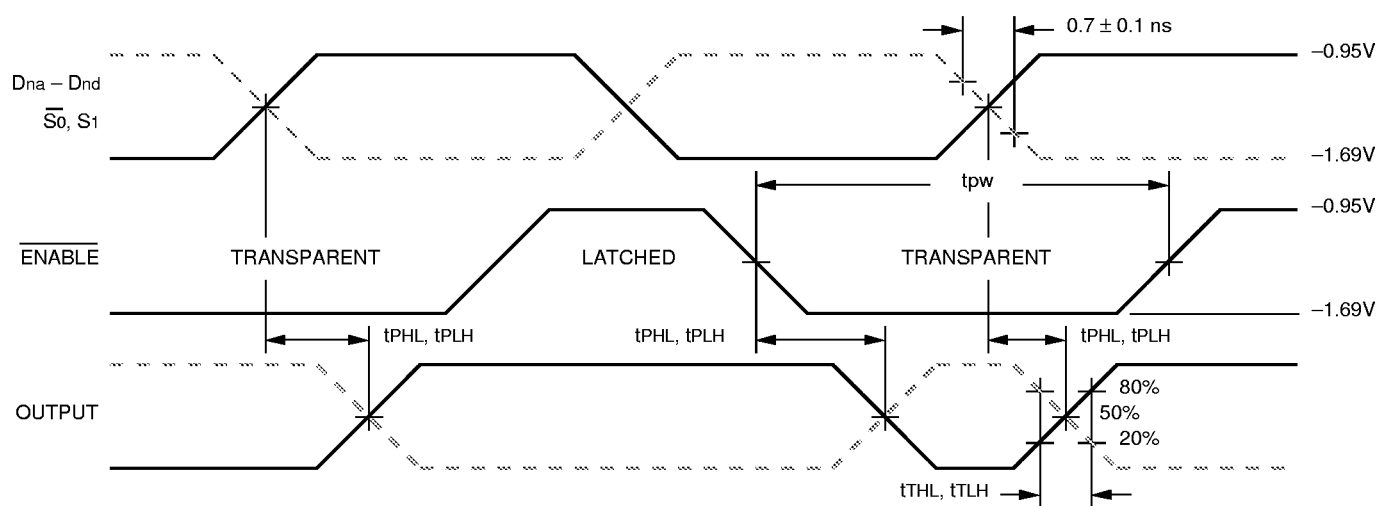
AC ELECTRICAL CHARACTERISTICS (Continued)

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

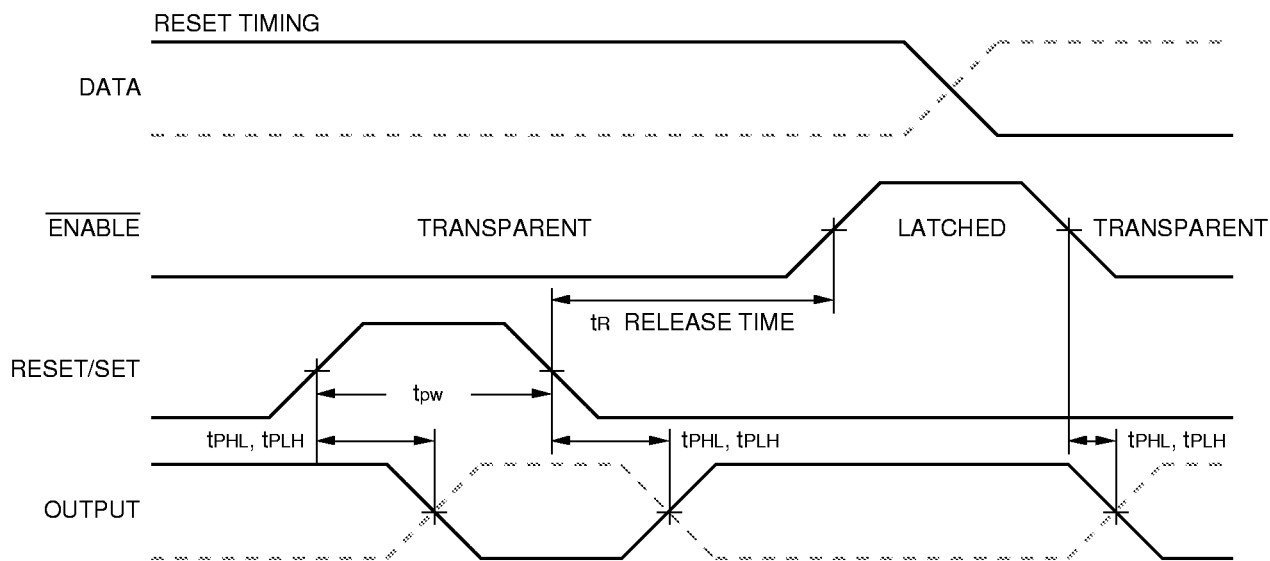
Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay $D_{na} - D_{nd}$ to Output (Transparent Mode)	300	1100	300	1100	300	1100	ps	
tPLH tPHL	Propagation Delay $\bar{S}_0, S_1$ to Output (Transparent Mode)	300	1400	300	1400	300	1400	ps	
tPLH tPHL	Propagation Delay $\bar{E}_1, \bar{E}_2$ to Output	300	1400	300	1400	300	1400	ps	
tPLH tPHL	Propagation Delay MR to Output	300	1100	300	1100	300	1100	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
ts	Set-up Time $D_{na} - D_{nd}$	700	—	700	—	700	—	ps	
	$\bar{S}_0, S_1$	1200	—	1200	—	1200	—		
	MR (Release Time)	1000	—	1000	—	1000	—		
th	Hold Time $D_{na} - D_{nd}$	300	—	300	—	300	—	ps	
	$\bar{S}_0, S_1$	300	—	300	—	300	—		
tpw (L)	Pulse Width LOW, $\bar{E}_1, \bar{E}_2$	1000	—	1000	—	1000	—	ps	
tpw (H)	Pulse Width HIGH, MR	1000	—	1000	—	1000	—	ps	

TIMING DIAGRAMS

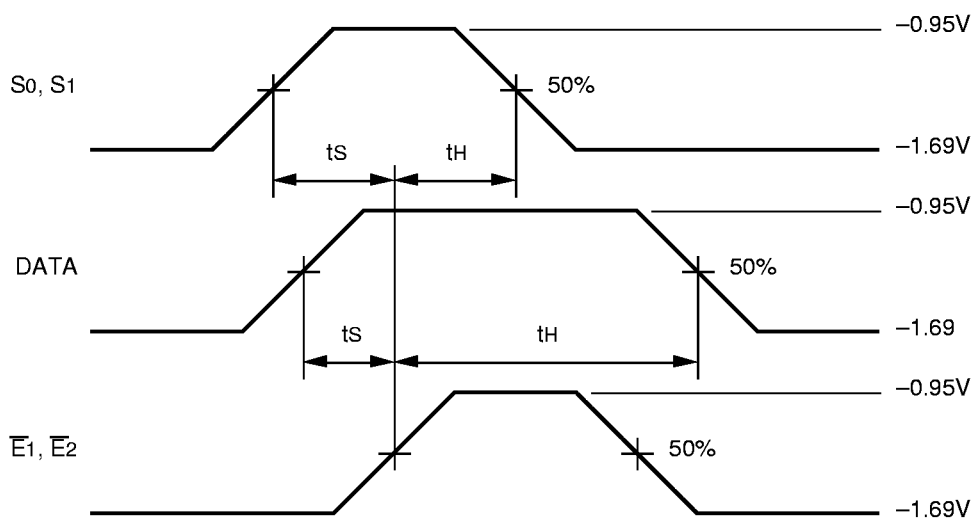


Enable Timing

TIMING DIAGRAMS (Continued)



Reset Timing



Data Set-up and Hold Times

NOTES:

1. $V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$
2. t_s is the minimum time before the transition of the clock that information must be present at the data input.
3. t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

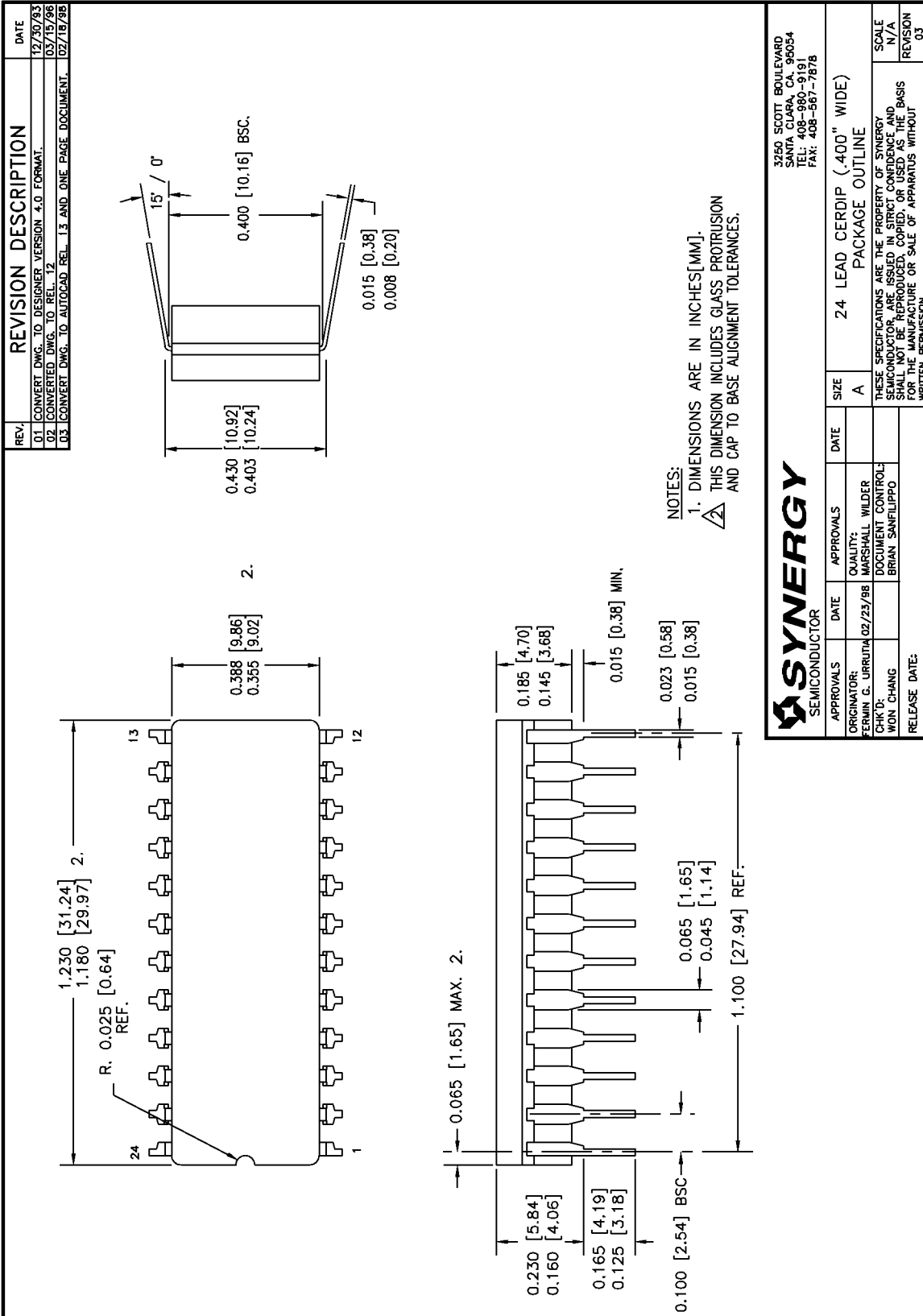
Ordering Code	Package Type	Operating Range
SY100S355DC	D24-1	Commercial
SY100S355FC	F24-1	Commercial
SY100S355JC	J28-1	Commercial
SY100S355JCTR	J28-1	Commercial

24 LEAD CERDIP (D24-1)

FILE/REV #: PD0003A03

PD/0003/ASCORP

PAGE 1 OF 1

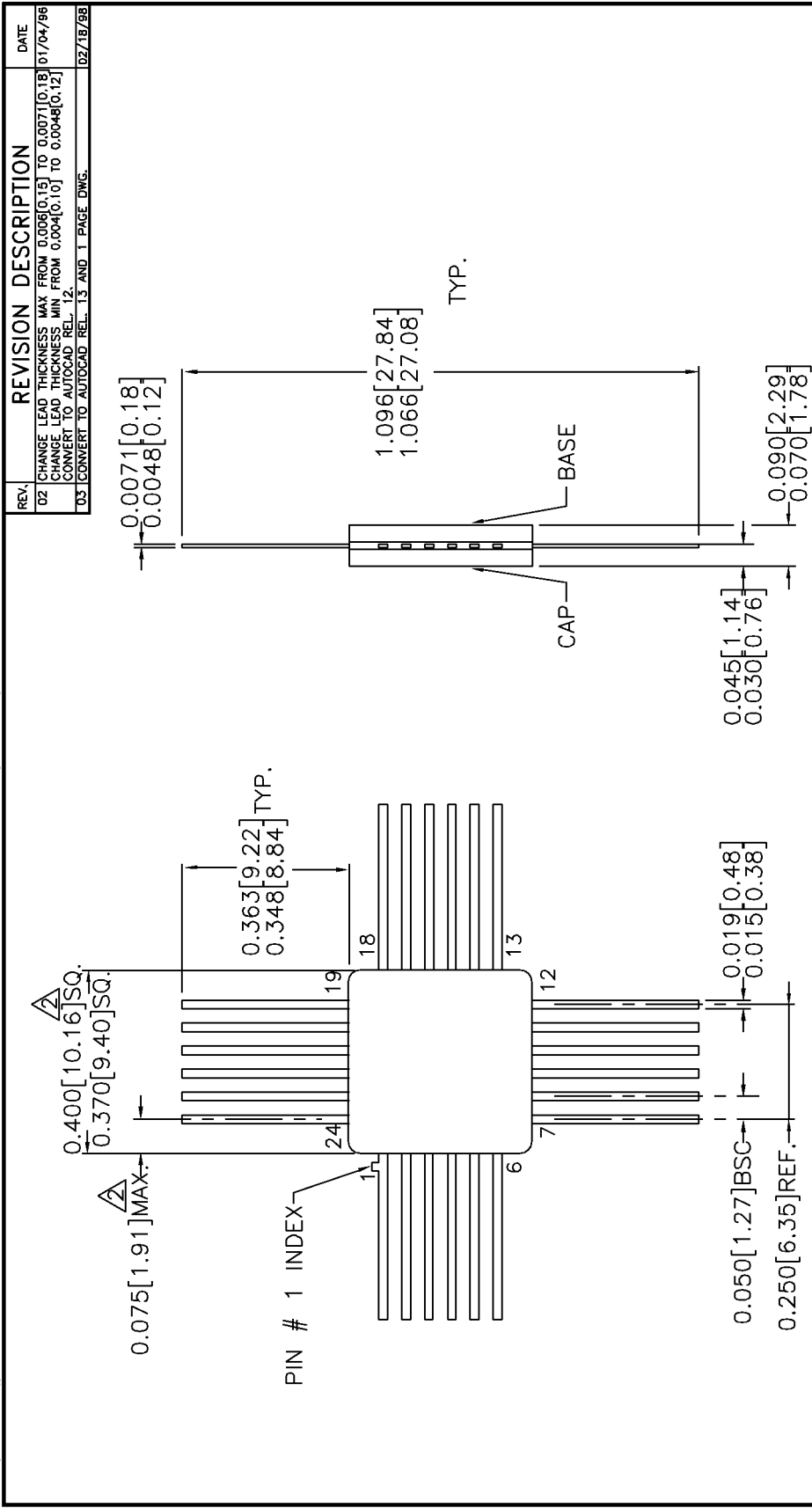


24 LEAD CERPACK (F24-1)

FILE/REV #: PD0006A03

PD/0006/ASCORP

PAGE 1 OF 1



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.



3250 SCOTT BOULEVARD
SANTA CLARA, CA 95054
TEL: 408-980-9191
FAX: 408-587-7878

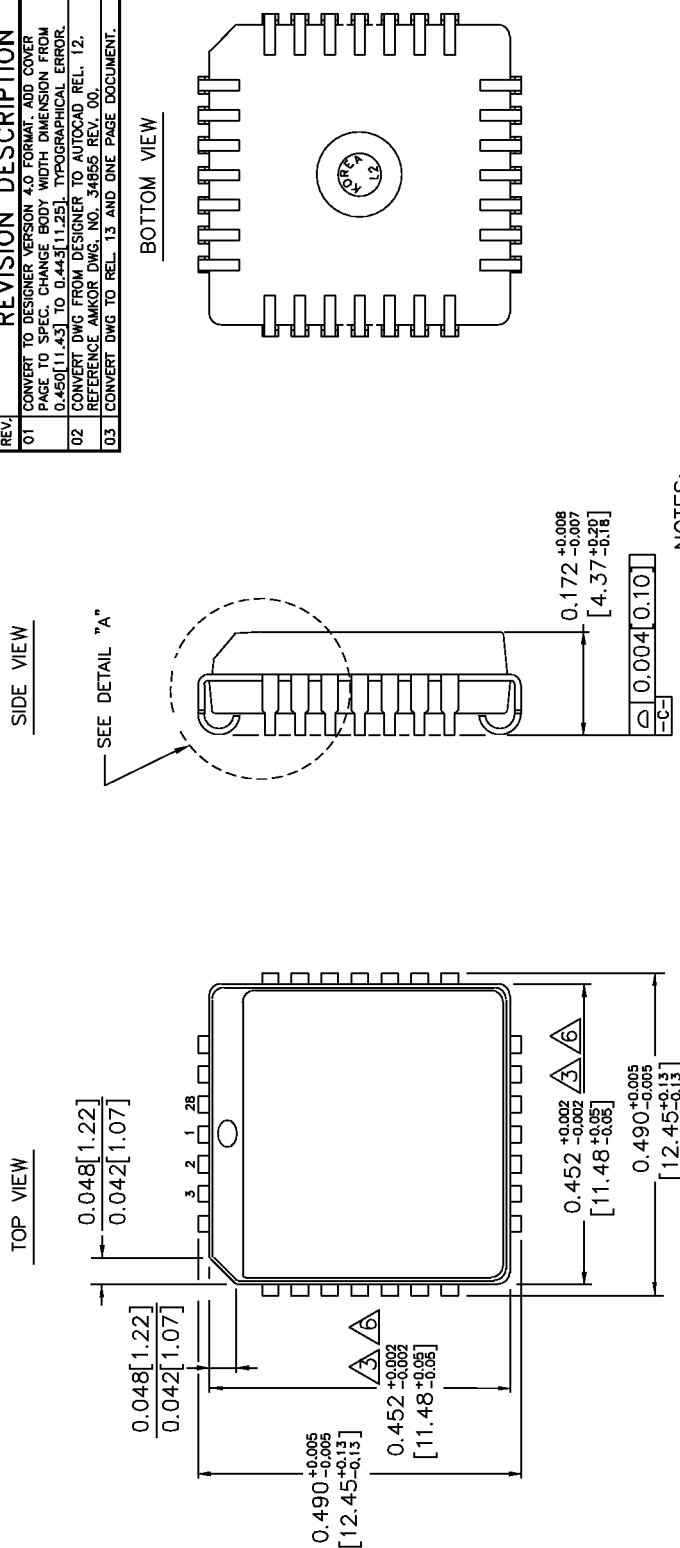
APPROVALS	DATE	APPROVALS	DATE	SIZE	24 LEAD CERPACK
ORIGINATOR: FERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					
					THESE SPECIFICATIONS ARE THE PROPERTY OF SYNERGY SEMICONDUCTOR, ARE ISSUED IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, OR USED AS THE BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS WITHOUT WRITTEN PERMISSION.
					SCALE N/A
					REVISION 03

FILE/REV #: PD0008A03

PD/0008/ASCORP

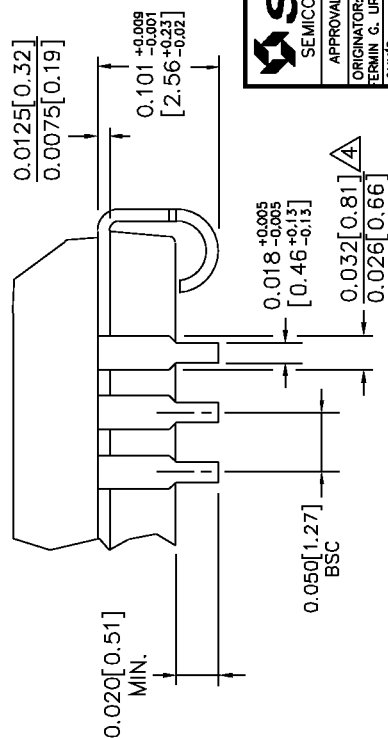
PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER BODY 4.0 FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH WITH DIMENSION FROM 0.450(11.43) TO 0.443(11.25). TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AKMOR DWG. NO. 34855 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



DETAIL "A"

SYNERGY
SEMICONDUCTOR

3250 SCOTT BOULEVARD
SANTA CLARA, CA, 95054
TEL: 408-980-9191
FAX: 408-567-7878

SEMI-CONDUCTOR	APPROVALS	DATE	APPROVALS	DATE	SIZE	28 LEAD PLCC	PLCC
	ORIGINATOR:	02/23/98	QUALITY:		A	PACKAGE OUTLINE	
	CHK'D:		DOCUMENT CONTROL:				
	WON CHANG		BRIAN SANFILIPPO				
	RELEASE DATE:					THESE SPECIFICATIONS ARE THE PROPERTY OF SYNERGY SEMICONDUCTOR, ARE ISSUED IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, OR USED AS THE BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS WITHOUT	SCALE N/A
							REVISION 03