FEATURES

- **Max. propagation delay of 1500ps**
- **I_{EE} min. of –120mA**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option: V_{EE} = –4.2V to –5.5V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **120% faster than National or Signetics**
- **Approximately 40% lower power than National or Signetics**
- **Function and pinout compatible with National and Signetics F100K**
- **ESD protection of 2000V**
- **Available in 24-pin CERDIP, 24-pin CERPACK and 28-pin PLCC packages**

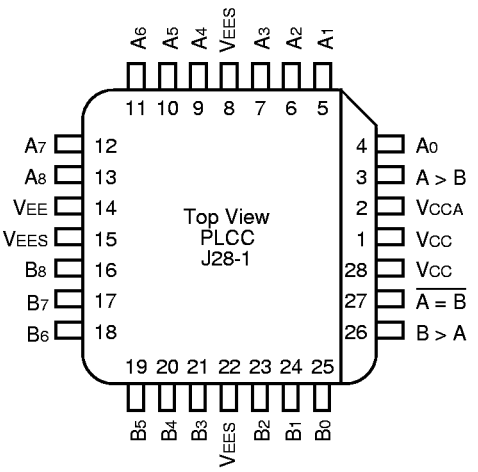
PIN NAMES

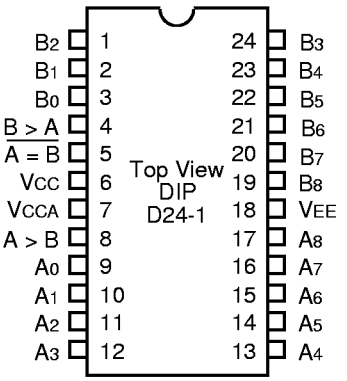
Pin	Function
A_0 – A_8	A Data Inputs
B_0 – B_8	B Data Inputs
A > B	A Greater Than B Output
B > A	B Greater Than A Output
$\overline{A = B}$	Complement A Equal to B Output (Active LOW)
V_{EES}	V_{EE} Substrate
V_{CCA}	V_{CCO} for ECL Outputs

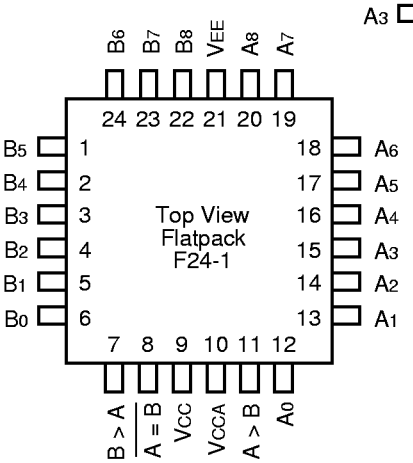
DESCRIPTION

The SY100S366 is an ultra-fast 9-bit magnitude comparator designed for use in high-performance ECL systems. The device compares the arithmetic value of two 9-bit words and indicates whether one word is greater than or equal to the other. The inputs on the device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS

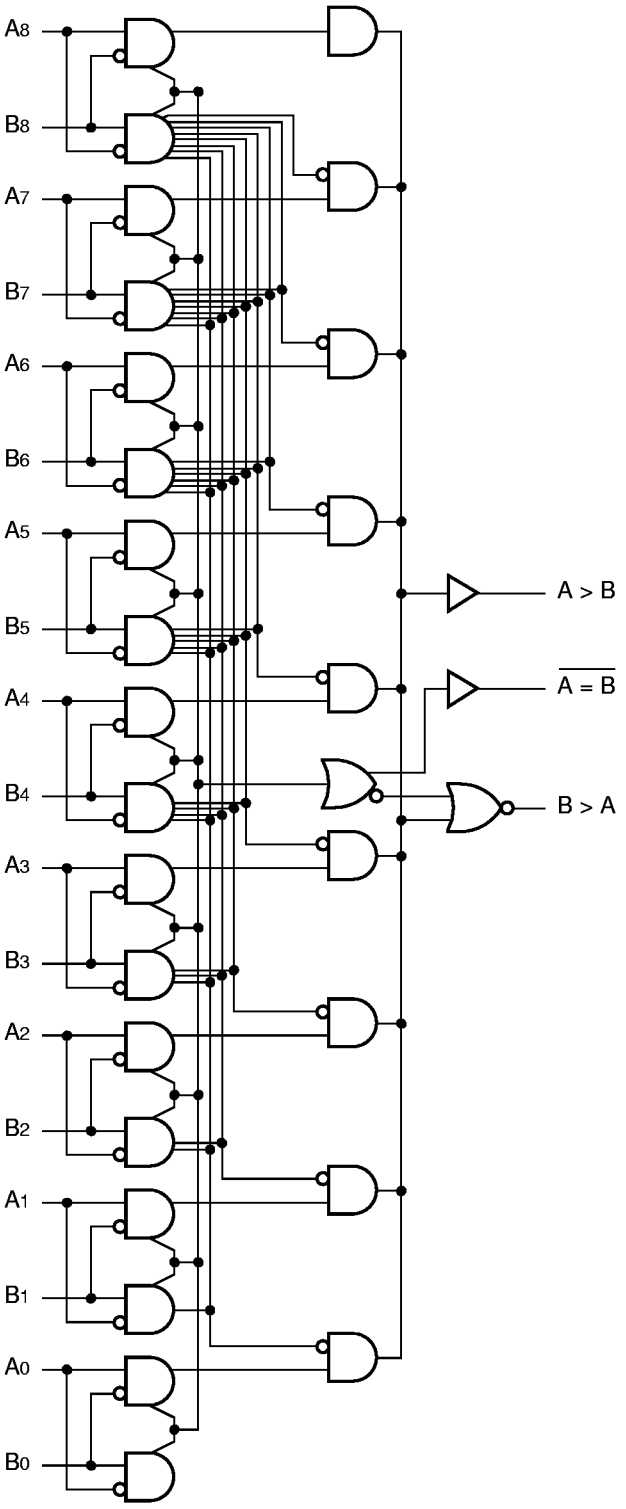






Rev.: F Amendment: /0
Issue Date: October, 1998

BLOCK DIAGRAM



TRUTH TABLE[1]

Inputs									Outputs		
A_8B_8	A_7B_7	A_6B_6	A_5B_5	A_4B_4	A_3B_3	A_2B_2	A_1B_1	A_0B_0	A > B	B > A	$\overline{A = B}$
H L									H	L	H
L H									L	H	H
$A_8 = B_8$	H L								H	L	H
$A_8 = B_8$	L H								L	H	H
$A_8 = B_8$	$A_7 = B_7$	H L							H	L	H
$A_8 = B_8$	$A_7 = B_7$	L H							L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	H L						H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	L H						L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	H L					H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	L H					L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	H L				H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	L H				L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	H L			H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	L H			L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	H L		H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	L H		L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	H L	H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	L H	L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	H

NOTE:

1. H = HIGH Voltage Level, L = LOW Voltage Level, Blank = X = Don't Care

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–120	–86	–60	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	400	1700	400	1700	400	1700	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

AC ELECTRICAL CHARACTERISTICS (Continued)

CERPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

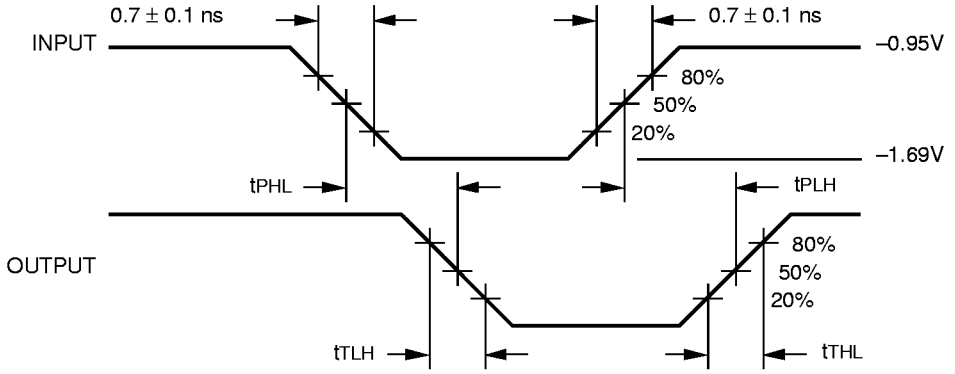
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	400	1600	400	1600	400	1600	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	400	1500	400	1500	400	1500	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



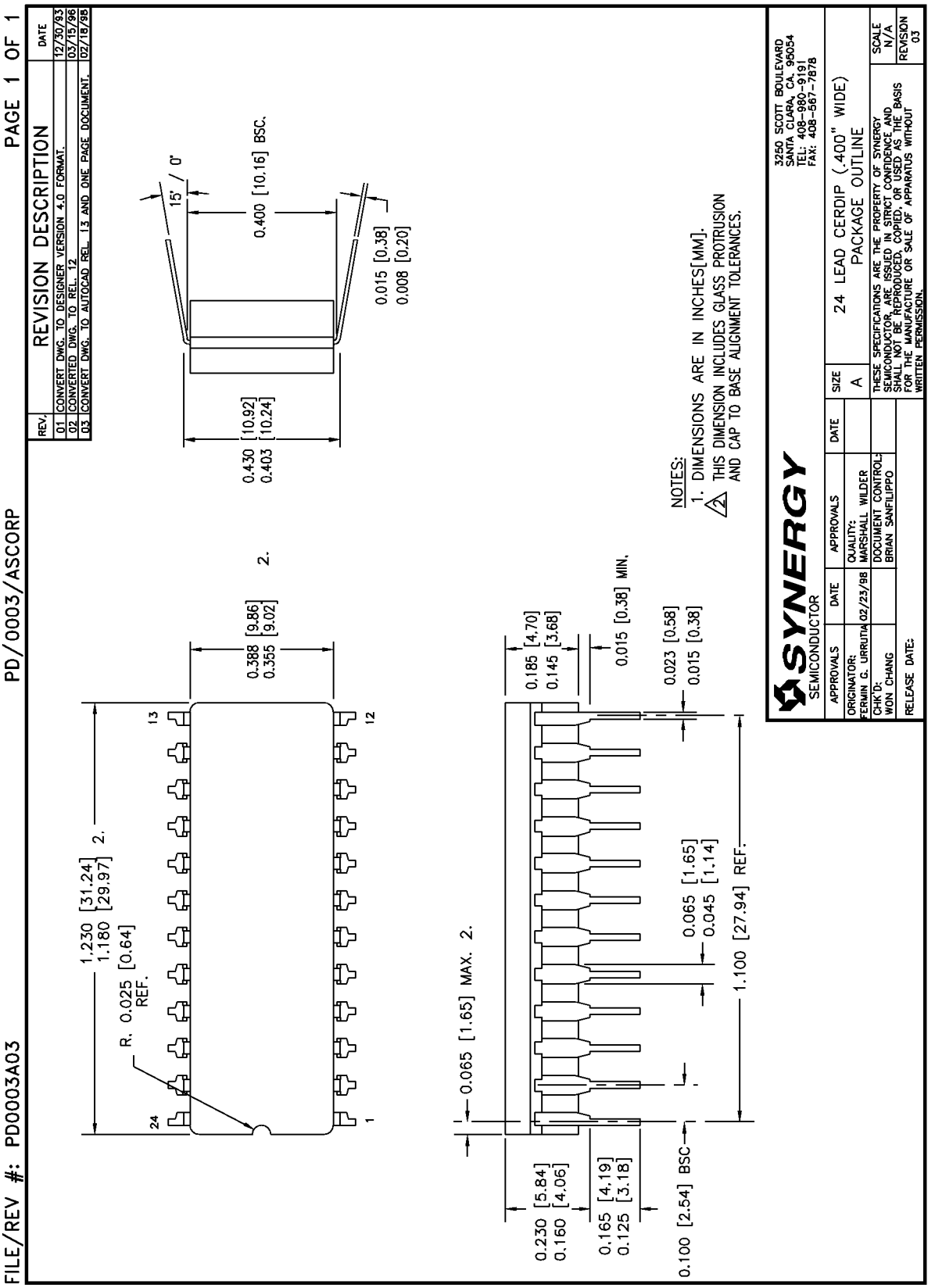
Propagation Delay and Transition Times

NOTE:
V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

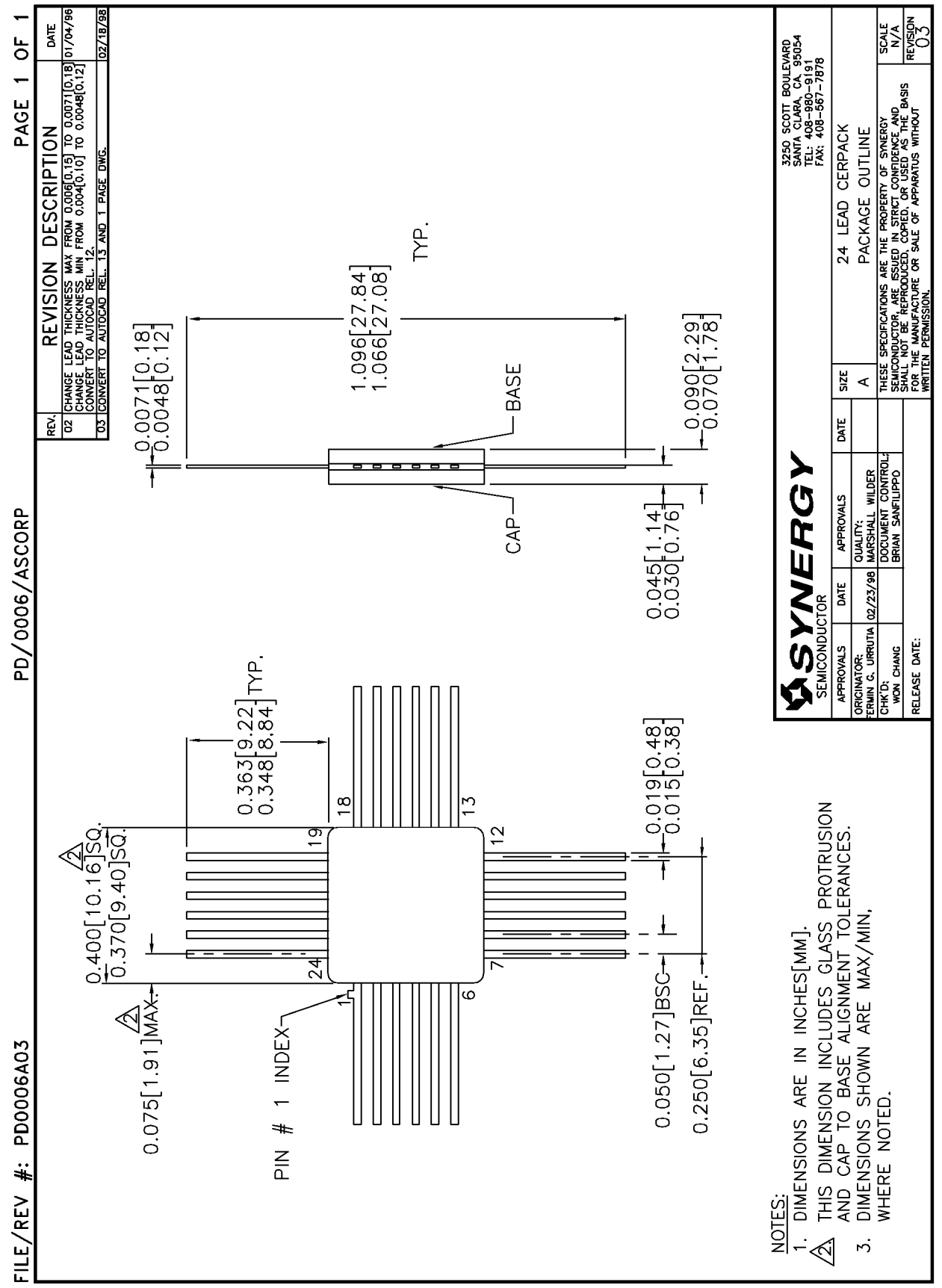
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S366DC	D24-1	Commercial
SY100S366FC	F24-1	Commercial
SY100S366JC	J28-1	Commercial
SY100S366JCTR	J28-1	Commercial

24 LEAD CERDIP (D24-1)



24 LEAD CERPACK (F24-1)



28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)