

FEATURES

- Max. propagation delay of 1500ps
- IEE min. of -120mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 120% faster than National or Signetics
- Approximately 40% lower power than National or Signetics
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin CERDIP, 24-pin CERPAC and 28-pin PLCC packages

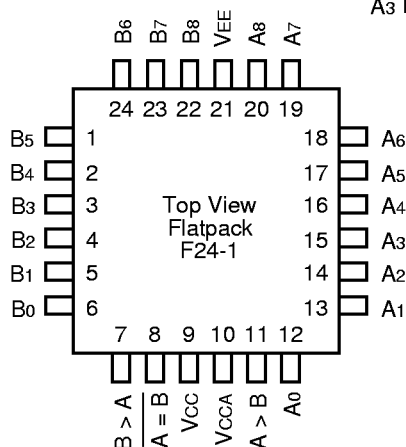
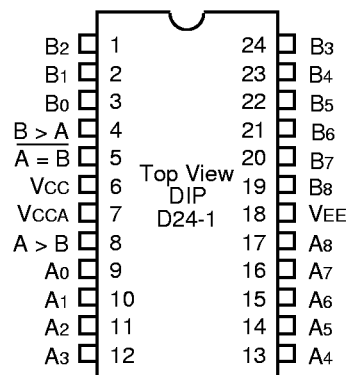
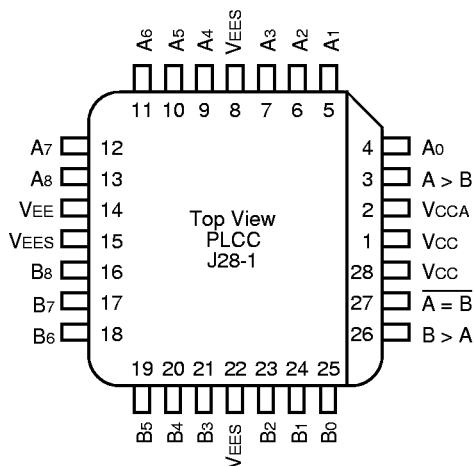
PIN NAMES

Pin	Function
A0 – A8	A Data Inputs
B0 – B8	B Data Inputs
A > B	A Greater Than B Output
B > A	B Greater Than A Output
A = B	Complement A Equal to B Output (Active LOW)
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

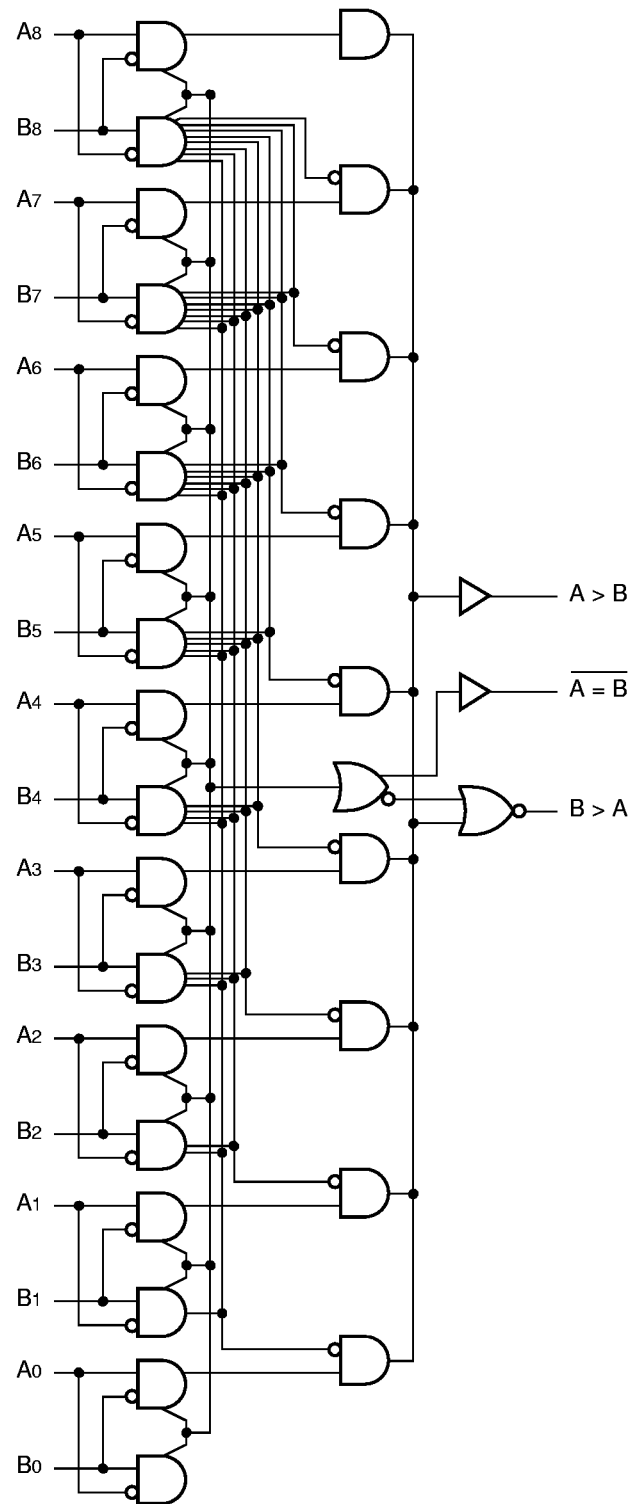
DESCRIPTION

The SY100S366 is an ultra-fast 9-bit magnitude comparator designed for use in high-performance ECL systems. The device compares the arithmetic value of two 9-bit words and indicates whether one word is greater than or equal to the other. The inputs on the device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS



BLOCK DIAGRAM



TRUTH TABLE⁽¹⁾

Inputs									Outputs		
A8B8	A7B7	A6B6	A5B5	A4B4	A3B3	A2B2	A1B1	A0B0	A > B	B > A	A = B
H L L H A8 = B8 A8 = B8	H L L H								H L H L	L H L H	H H H H
A8 = B8 A8 = B8 A8 = B8 A8 = B8	A7 = B7 A7 = B7 A7 = B7 A7 = B7	H L L H A6 = B6 A6 = B6	H L L H						H L H L	L H L H	H H H H
A8 = B8 A8 = B8 A8 = B8 A8 = B8	A7 = B7 A7 = B7 A7 = B7 A7 = B7	A6 = B6 A6 = B6 A6 = B6 A6 = B6	A5 = B5 A5 = B5 A5 = B5 A5 = B5	H L L H A4 = B4 A4 = B4	H L L H				H L H L	L H L H	H H H H
A8 = B8 A8 = B8 A8 = B8 A8 = B8	A7 = B7 A7 = B7 A7 = B7 A7 = B7	A6 = B6 A6 = B6 A6 = B6 A6 = B6	A5 = B5 A5 = B5 A5 = B5 A5 = B5	A4 = B4 A4 = B4 A4 = B4 A4 = B4	A3 = B3 A3 = B3 A3 = B3 A3 = B3	H L L H A2 = B2 A2 = B2	H L L H		H L H L	L H L H	H H H H
A8 = B8 A8 = B8 A8 = B8 A8 = B8	A7 = B7 A7 = B7 A7 = B7 A7 = B7	A6 = B6 A6 = B6 A6 = B6 A6 = B6	A5 = B5 A5 = B5 A5 = B5 A5 = B5	A4 = B4 A4 = B4 A4 = B4 A4 = B4	A3 = B3 A3 = B3 A3 = B3 A3 = B3	A2 = B2 A2 = B2 A2 = B2 A2 = B2	A1 = B1 A1 = B1 A1 = B1 A1 = B1	H L L H A0 = B0 A0 = B0	H L L L	L H H H	H H H H

NOTE:

1. H = HIGH Voltage Level, L = LOW Voltage Level, Blank = X = Don't Care

DC ELECTRICAL CHARACTERISTICS

V_{EE} = -4.2V to -5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current, All Inputs	—	—	200	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	-120	-86	-60	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

V_{EE} = -4.2V to -5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	400	1700	400	1700	400	1700	ps	
t _{TTLH} t _{TTHL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

AC ELECTRICAL CHARACTERISTICS (Continued)

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

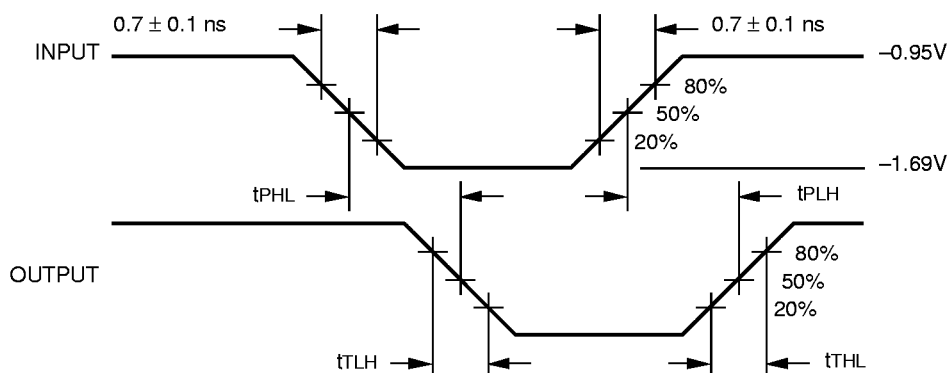
Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay Data to Output	400	1600	400	1600	400	1600	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay Data to Output	400	1500	400	1500	400	1500	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



Propagation Delay and Transition Times

NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

PRODUCT ORDERING CODE

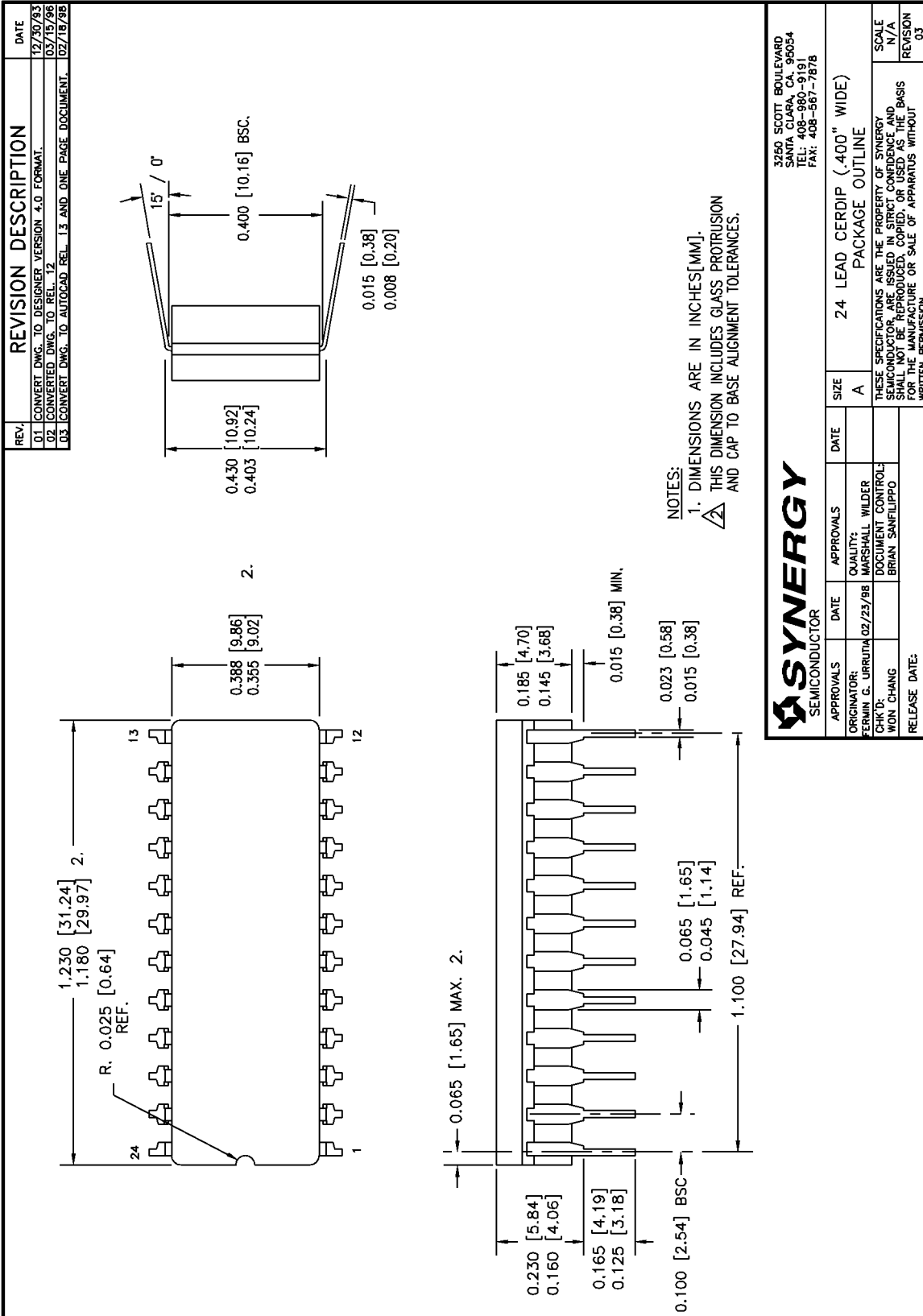
Ordering Code	Package Type	Operating Range
SY100S366DC	D24-1	Commercial
SY100S366FC	F24-1	Commercial
SY100S366JC	J28-1	Commercial
SY100S366JCTR	J28-1	Commercial

24 LEAD Cerdip (D24-1)

FILE/REV #: PD0003A03

PD/0003/ASCORP

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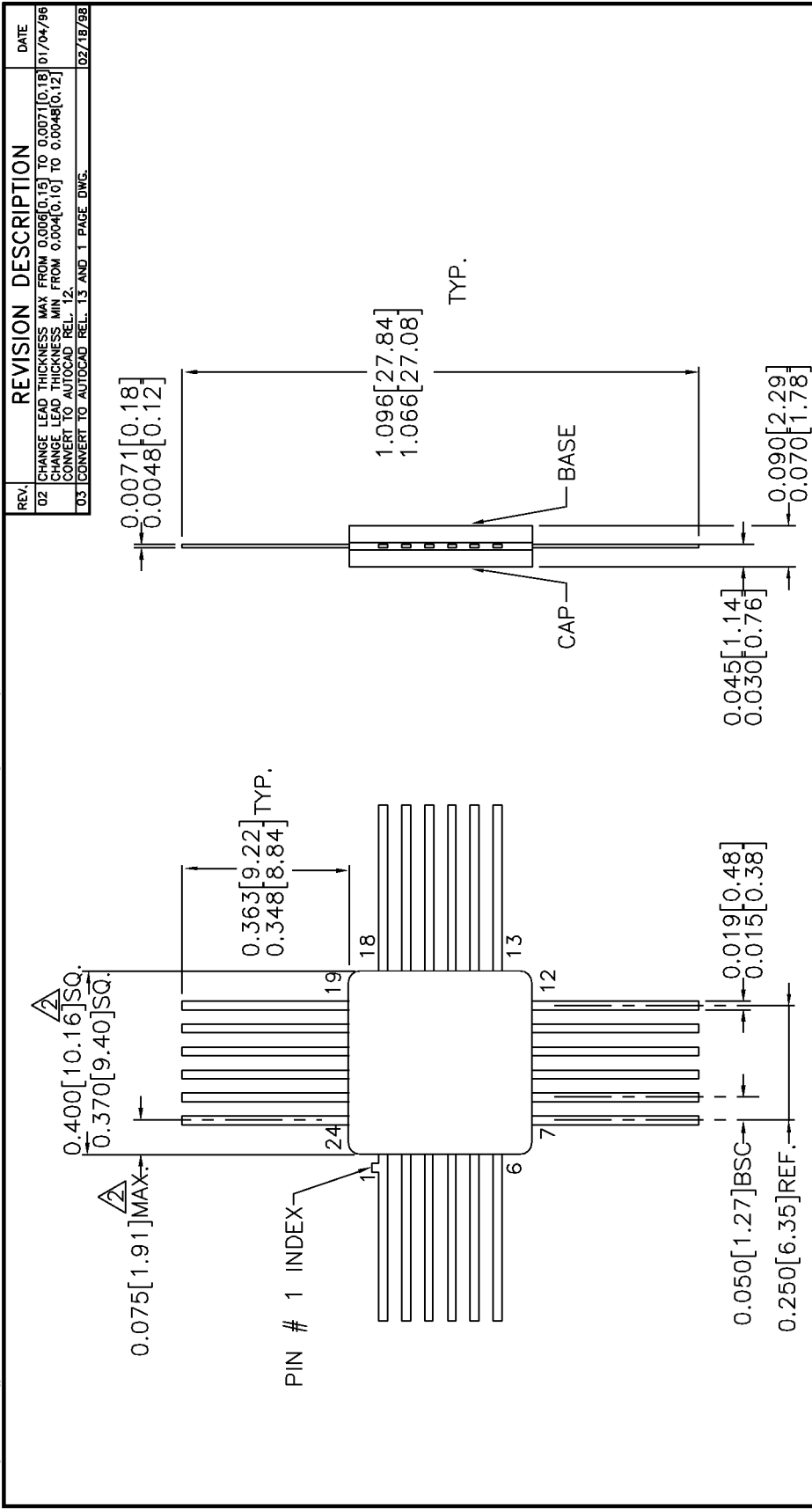


24 LEAD CERPACK (F24-1)

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NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.



3250 SCOTT BOULEVARD
SANTA CLARA, CA 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	24 LEAD CERPACK
ORIGINATOR: FERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					
					THESE SPECIFICATIONS ARE THE PROPERTY OF SYNERGY SEMICONDUCTOR, ARE ISSUED IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, OR USED AS THE BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS WITHOUT WRITTEN PERMISSION.
					SCALE N/A
					REVISION 03

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

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