N-channel enhancement mode vertical D-MOS transistor

BSP110

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use in telephone ringer circuits and for application in relay, high-speed and line transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	325	mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	1.5	W
Drain-source ON-resistance $I_D = 200$ mA; $V_{GS} = 10$ V	$R_{DS(on)}$	typ. max.	4.5 7	Ω Ω
Transfer admittance $I_D = 200$ mA; $V_{DS} = 15$ V	$\lvert Y_{fs} \rvert$	min. typ.	75 150	mS mS

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

MARKING CODE

BSP110

PIN CONFIGURATION

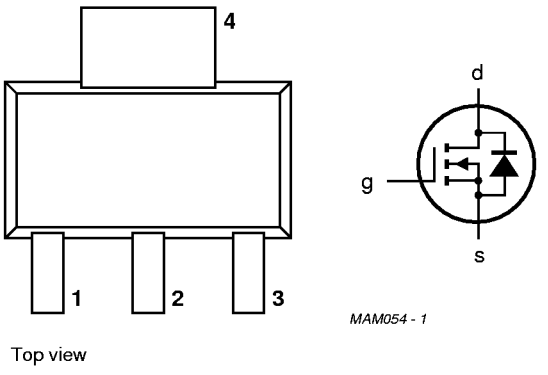

Fig.1 Simplfied outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	325	mA
Drain current (peak)	I_{DM}	max.	650	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)\ DSS}$	min.	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$I_{GS(th)}$	min. max.	0.8 2.8	V V
Drain-source ON-resistance (see Fig.4) I_D = 150 mA; V_{GS} = 5 V	$R_{DS(on)}$	typ. max.	7 10	Ω Ω
I_D = 200 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	4.5 7	Ω Ω
Transfer admittance I_D = 200 mA; V_{DS} = 5 V	$\lvert Y_{fs} \rvert$	min. typ.	75 150	mS mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	15 30	pF pF

Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	13 pF
		max.	20 pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	3 pF
		max.	6 pF
Switching times (see Figs 2 and 3)			
I_D = 200 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	2 ns
		max.	5 ns
	t_{off}	typ.	5 ns
		max.	10 ns

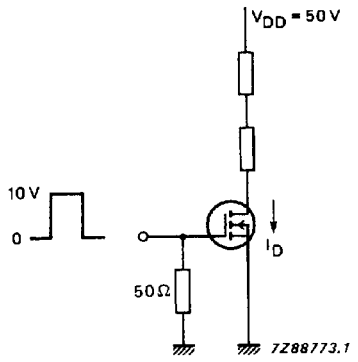


Fig.2 Switching time test circuit.

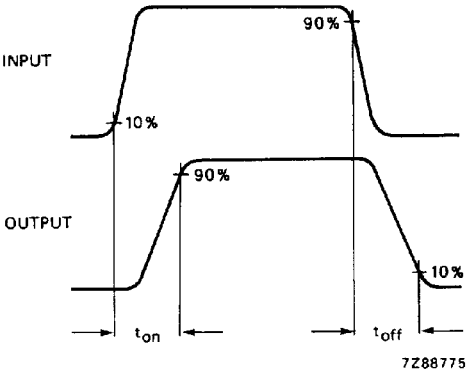


Fig.3 Input and output waveforms.

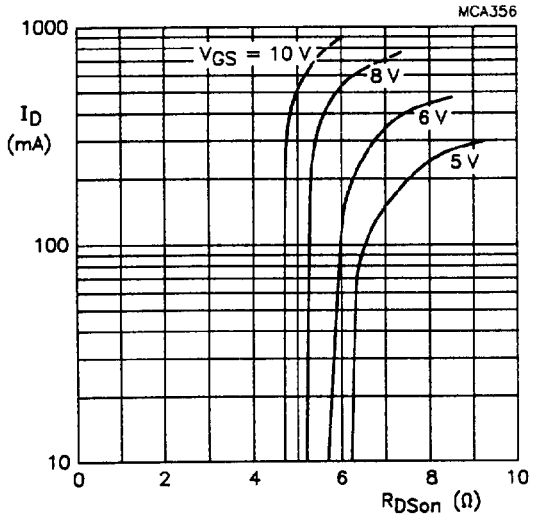


Fig.4 T_j = 25 °C; typical values.

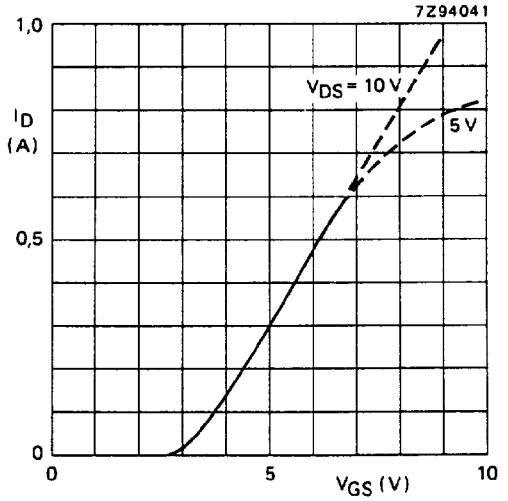


Fig.5 T_j = 25 °C; typical values.

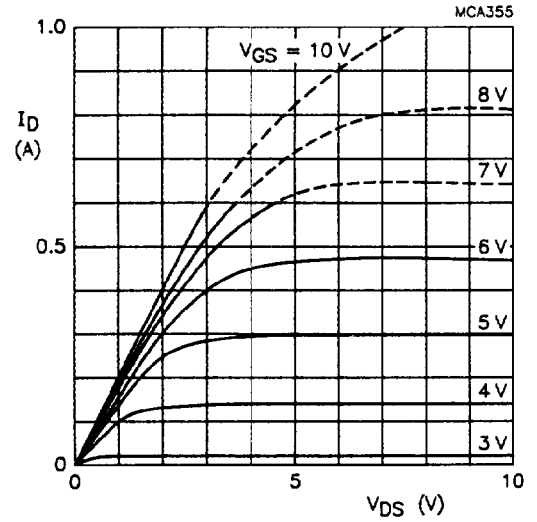


Fig.6 T_j = 25 °C; typical values.

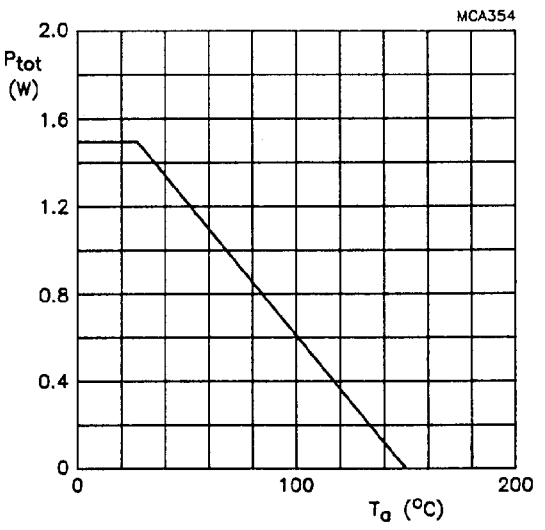


Fig.7 Power derating curve.

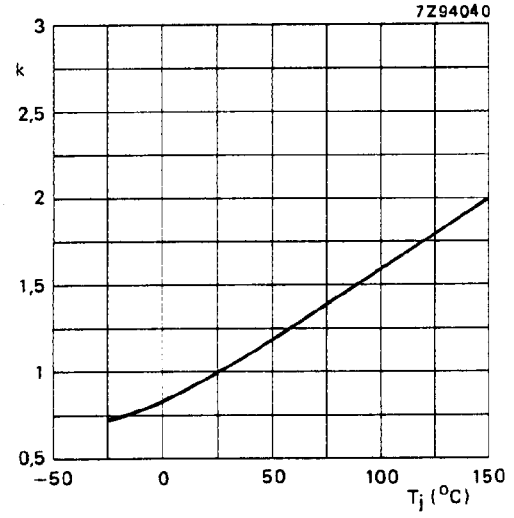


Fig.8

$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C};$$

typical values at 150 mA/5 V.

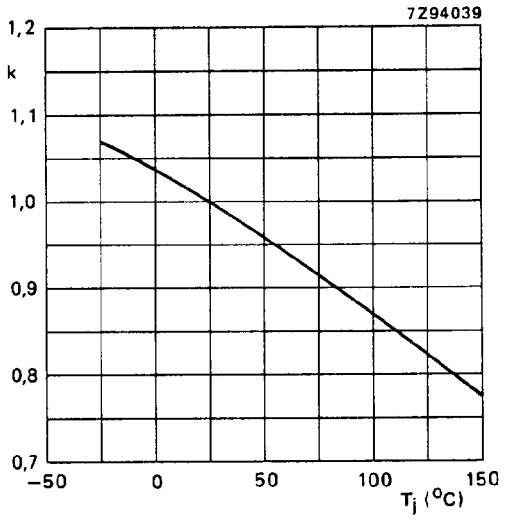


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

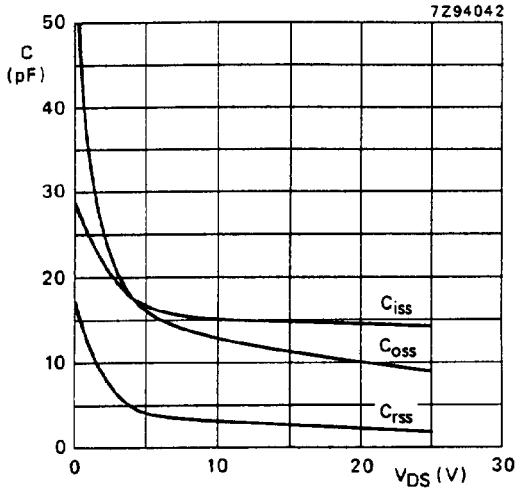
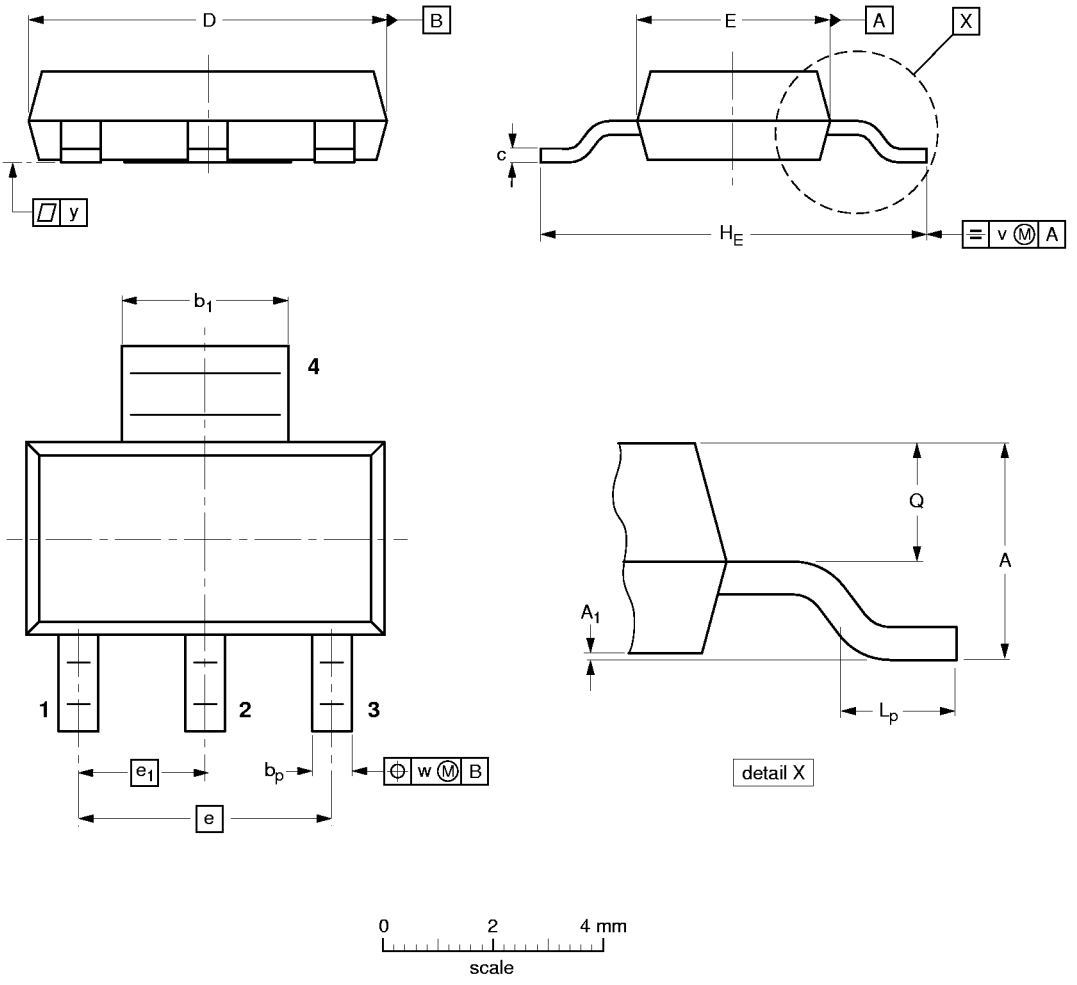


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						~~96-11-11~~ 97-02-28