P-channel enhancement mode vertical D-MOS transistor

BSP250

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Low-loss motor and actuator drivers
- Power switching.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 plastic SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

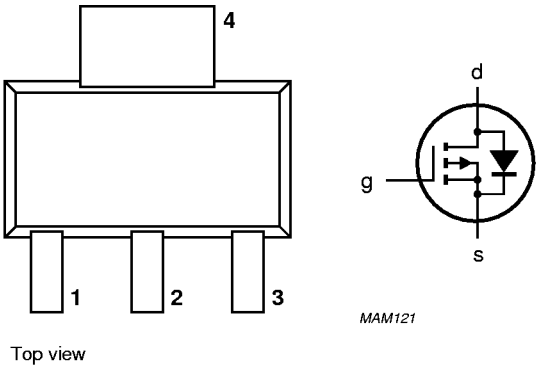

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1	–2.8	V
I_D	drain current (DC)		–	–3	A
R_{DSon}	drain-source on-state resistance	I_D = –1 A; V_{GS} = –10 V	–	0.25	Ω
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 100$ °C	–	–3	A
I_{DM}	peak drain current	note 1	–	–12	A
P_{tot}	total power dissipation	$T_s = 100$ °C	–	5	W
		$T_{amb} = 25$ °C; note 2	–	1.65	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 100$ °C	–	–1.5	A
I_{SM}	peak pulsed source current	note 1	–	–6	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

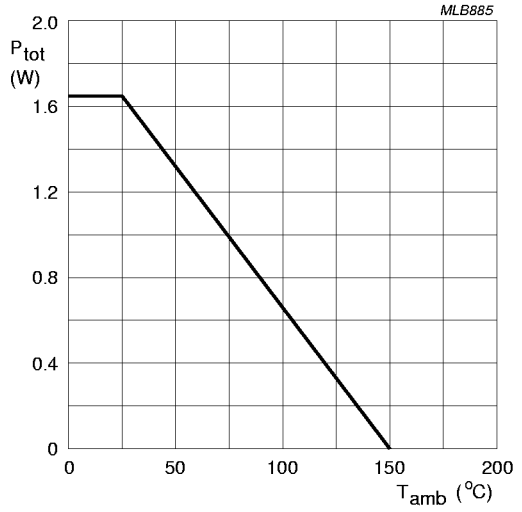
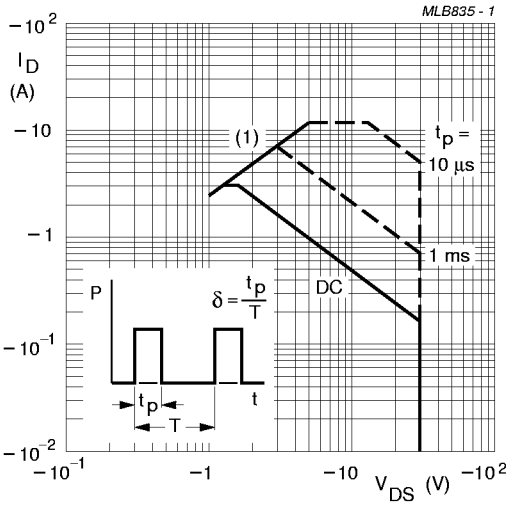


Fig.2 Power derating curve.



δ = 0.01.
Soldering point temperature $T_s = 100$ °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	75	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point		10	K/W

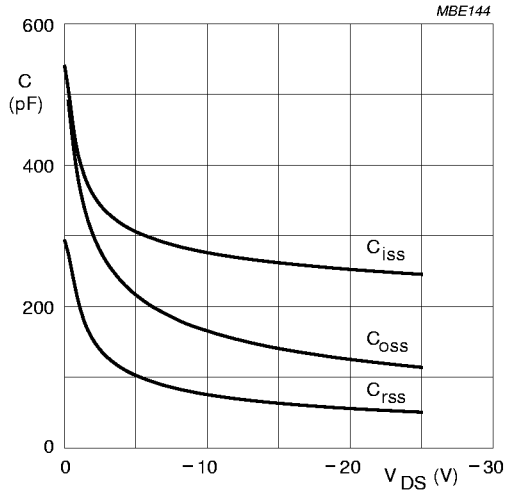
Note

1. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

CHARACTERISTICS

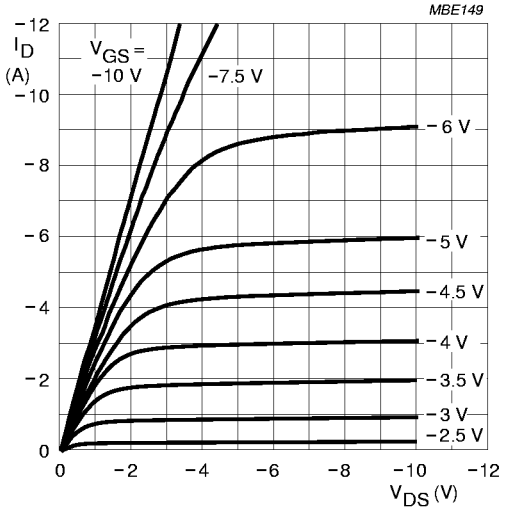
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = −10 V; V_{DS} = −1 V	−3	–	–	A
		V_{GS} = −4.5 V; V_{DS} = −5 V	−1	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	–	0.33	0.4	Ω
		V_{GS} = −10 V; I_D = −1 A	–	0.22	0.25	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = −20 V; I_D = −1 A	1	2	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	10	25	nC
Q_{GS}	gate-source charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	3	–	nC
Switching times						
t_{on}	turn-on time	V_{GS} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	20	80	ns
t_{off}	turn-off time	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	50	140	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.6	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	150	200	ns



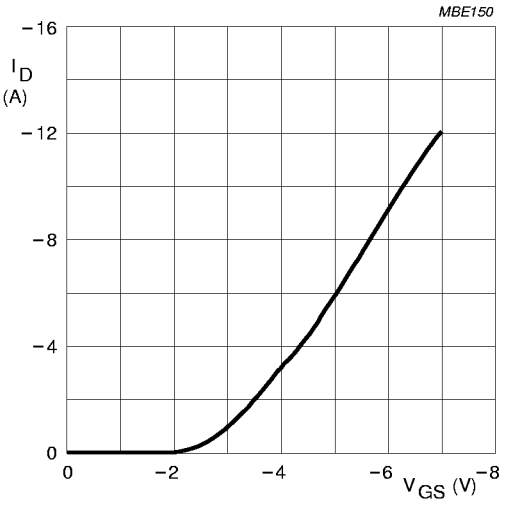
V_{GS} = 0.
T_j = 25 °C.

Fig.4 Capacitance as a function of drain source voltage; typical values.



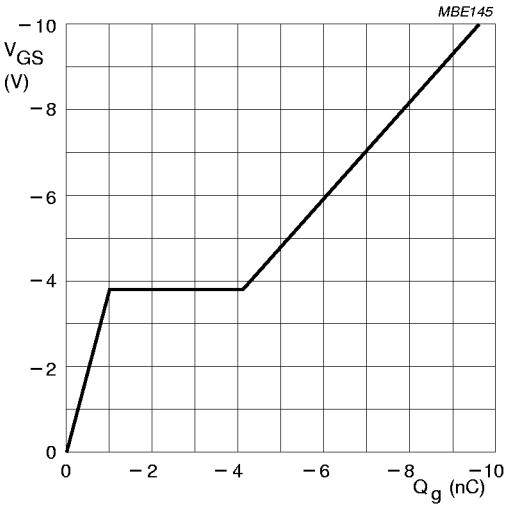
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



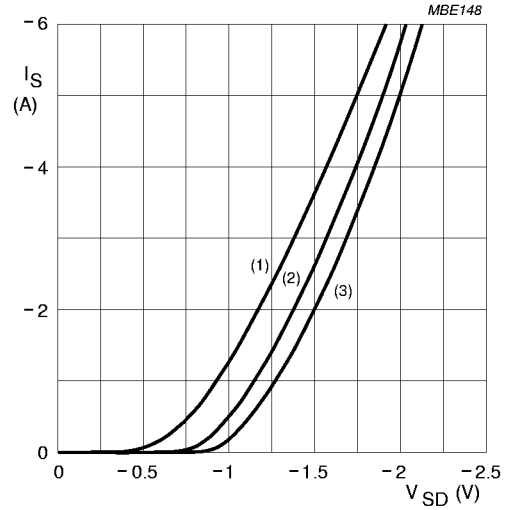
V_{DS} = −10 V.
T_j = 25 °C.

Fig.6 Transfer characteristic, typical values.



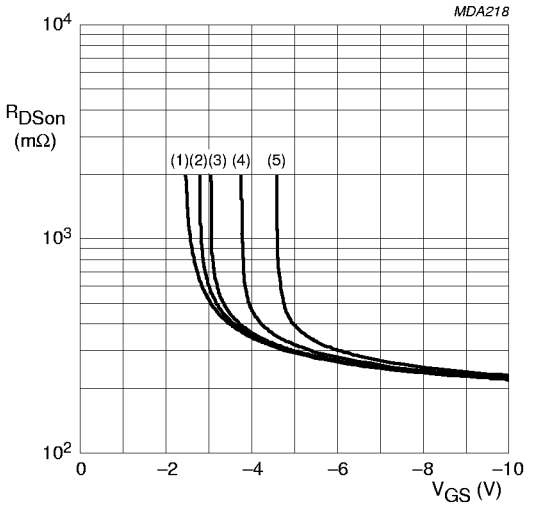
V_{DD} = −15 V.
I_D = −3 A.

Fig.7 Gate-source voltage as a function of total gate charge.



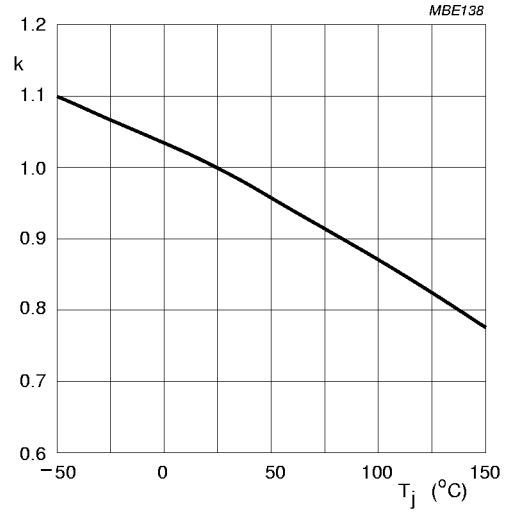
$V_{GD} = 0$.
(1) $T_j = 150$ °C.
(2) $T_j = 25$ °C.
(3) $T_j = -55$ °C.

Fig.8 Source current as a function of source-drain diode forward voltage.



$-V_{DS} \geq -I_D \times R_{DSon}$; $T_j = 25$ °C.
(1) $I_D = -0.1$ A.
(2) $I_D = -0.5$ A.
(3) $I_D = -1$ A.
(4) $I_D = -3$ A.
(5) $I_D = -6$ A.

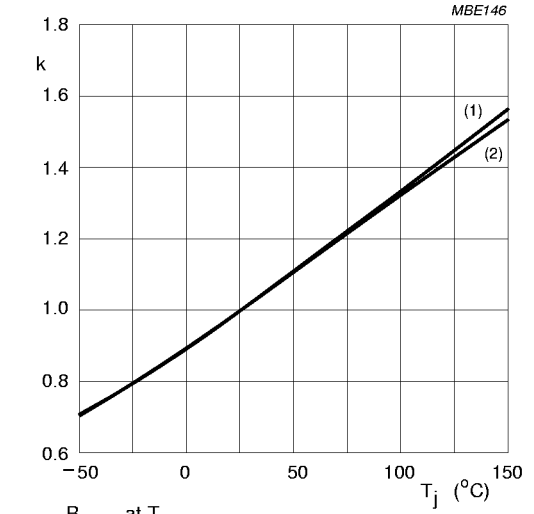
Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at $I_D = -1$ mA; $V_{DS} = V_{GS} = V_{GSth}$.

Fig.10 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:
(1) $I_D = -1$ A; $V_{GS} = -10$ V.
(2) $I_D = -0.5$ A; $V_{GS} = -4.5$ V.

Fig.11 Temperature coefficient of drain-source on-resistance.

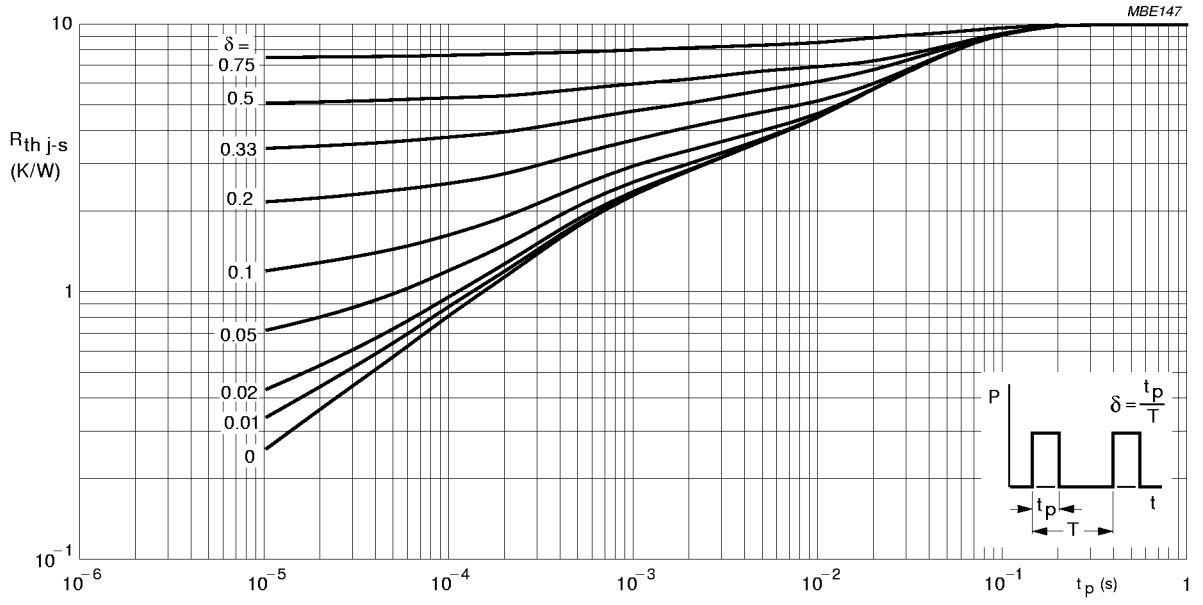
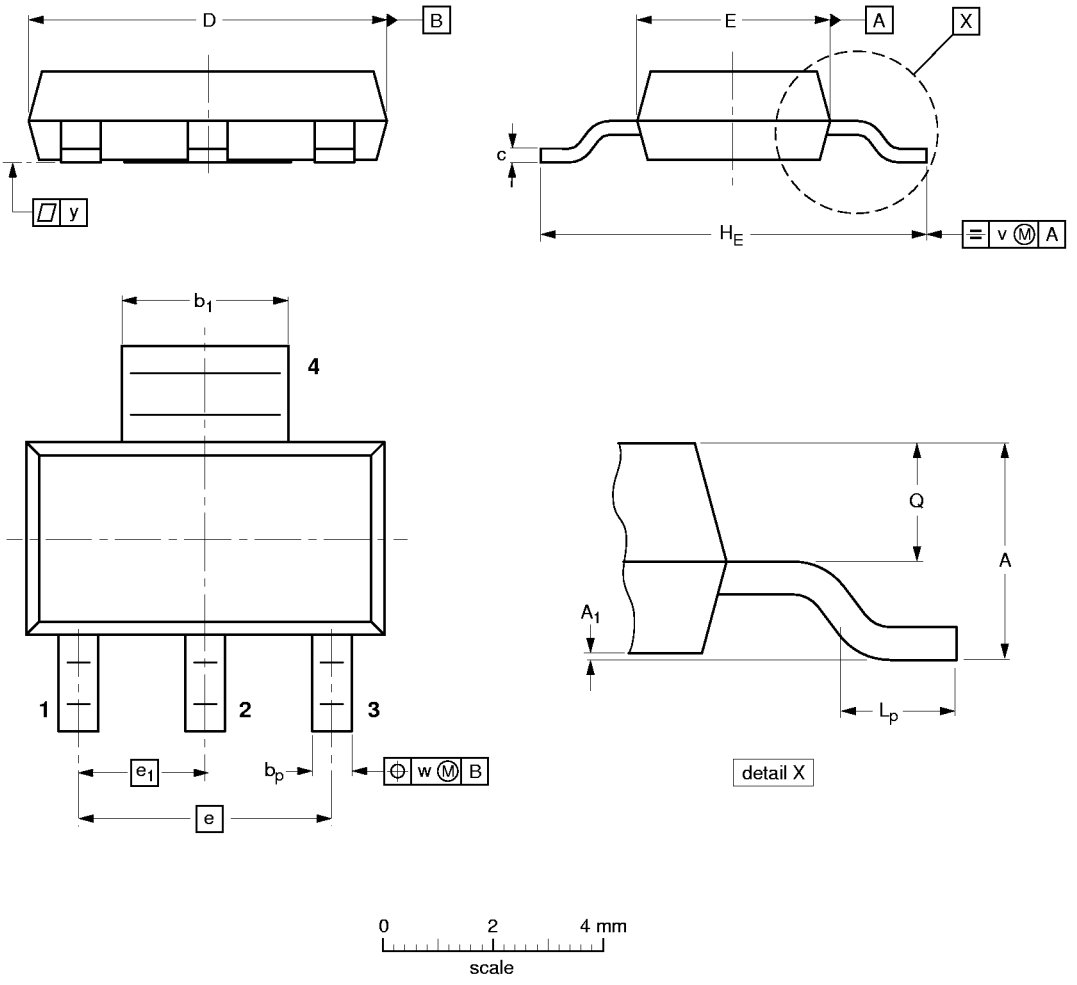


Fig.12 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						~~96-11-11~~ 97-02-28