N-channel enhancement mode vertical D-MOS transistor

BSS123

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

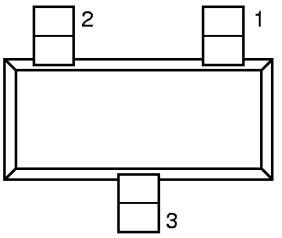
PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

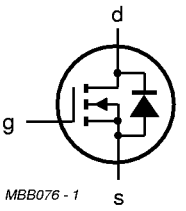
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		100	V
I_D	drain current	DC value	150	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	2.8	V

PIN CONFIGURATION



Top view



Marking: SA.

Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	100	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	150	mA
I_{DM}	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on a FR4 printboard.

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CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	100	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V V_{GS} = 0	–	–	10	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	–	3	6	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 120 mA V_{DS} = 25 V	80	140	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	24	40	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	15	25	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	10	20	ns

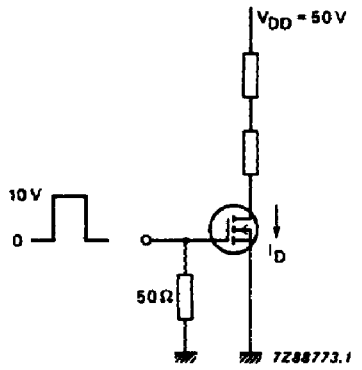


Fig.2 Switching time test circuit.

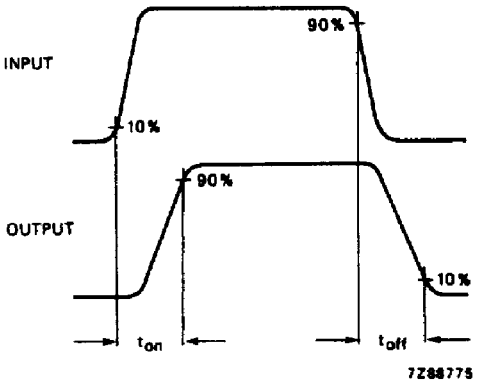
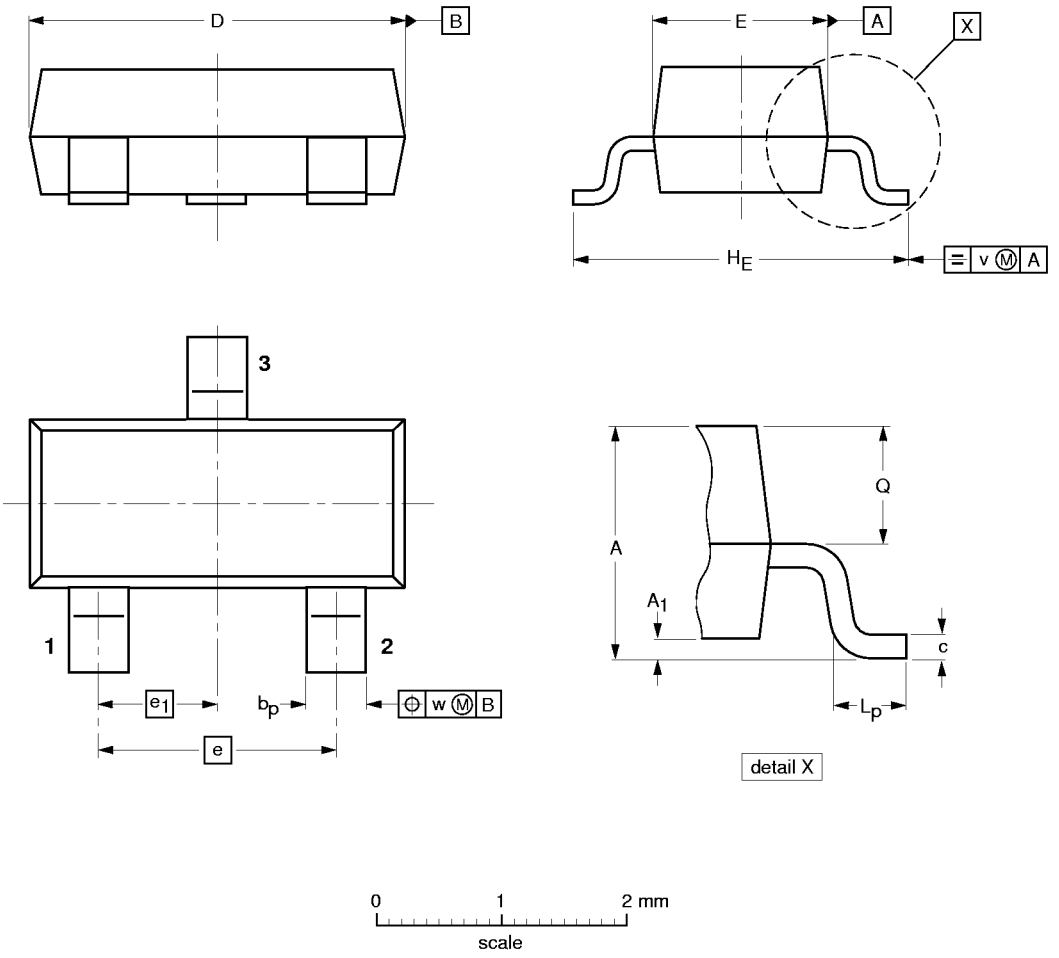


Fig.3 Input and output waveforms.

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28