N-channel enhancement mode vertical D-MOS transistor

BSS87

DESCRIPTION

N-channel vertical D-MOS transistor in a SOT89 envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high-speed transformer drivers etc.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.
- Low $R_{DS(on)}$

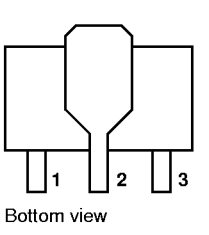
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	280	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source on-resistance				
I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	max.	6	Ω
		typ.	4.5	Ω
Transfer admittance				
I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	typ.	350	mS
		min.	140	mS

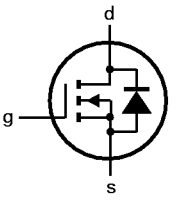
PINNING - SOT89

1 = source
2 = drain
3 = gate

PIN CONFIGURATION



Bottom view



MAM355

marking: KA

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	280	mA
Drain current (peak)	I_{DM}	max.	1.1	A
Total power dissipation up to T_{amb} = 25 °C (1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on ceramic substrate area 2.5 cm^2, thickness 0.7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 250 μA; V_{GS} = 0	$V_{(BR)\ DSS}$	min.	200	V
Drain-source leakage current				
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200	nA
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	60	μA
		typ.	100	nA
Gate-source leakage current				
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.8	V
Drain-source on-resistance				
I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	max.	6	Ω
		typ.	4.5	Ω
Transfer admittance				
I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	typ.	350	mS
		min.	140	mS
Input capacitance f = 1 MHz;				
V_{DS} = 25 V; V_{GS} = 0	C_{iss}	max.	60	pF
		typ.	45	pF
Output capacitance f = 1 MHz;				
V_{DS} = 25 V; V_{GS} = 0	C_{oss}	max.	25	pF
		typ.	15	pF

Feedback capacitance f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{rss}	max.	10 pF
		typ.	3.5 pF
Switching times (see Figs 2 and 3)			
I_D = 250 mA; V_{DD} = 50 V;	t_{on}	typ.	5 ns
		max.	10 ns
V_{GS} = 0 to 10	t_{off}	typ.	15 ns
		max.	25 ns

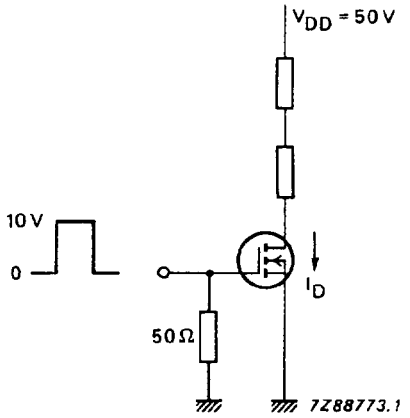


Fig.2 Switching times test circuit.

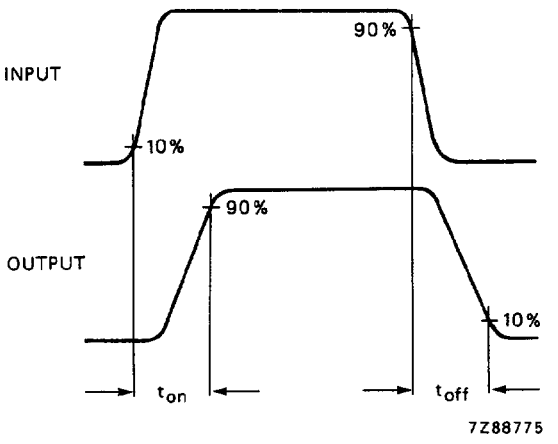
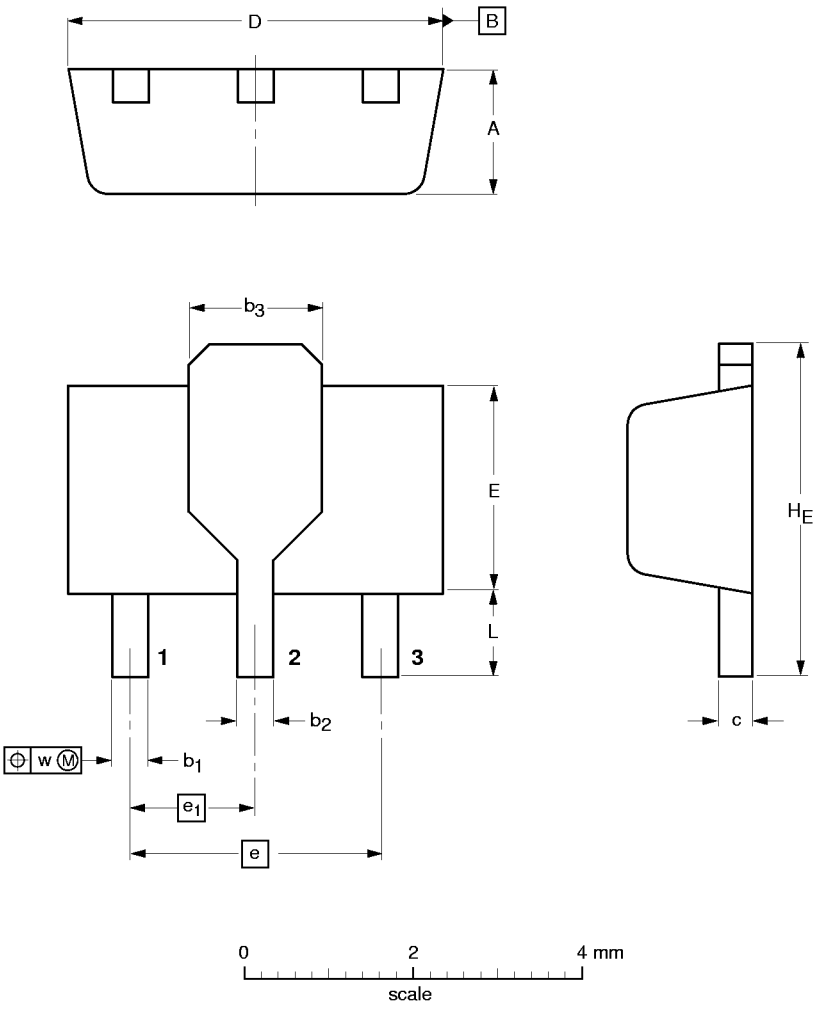


Fig.3 Input and output waveforms.

PACKAGE OUTLINES

Plastic surface mounted package; collector pad for good heat transfer; 3 leads **SOT89**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_1	b_2	b_3	c	D	E	e	e_1	H_E	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89						97-02-28