

TC551001PL-85/PL-10

TC551001FL-85/FL-10

T-4623-14

131,072 WORDS $\times$ 8 BIT STATIC RAM

DESCRIPTION

The TC551001PL/FL is 1,048,576 bits static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operated a single 5 V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5 mA / MHz (Typ.) and minimum cycle time of 85/100 ns. When $\overline{CE1}$ is a logical high, or $\overline{CE2}$ is low, the device is placed in low power standby mode in which standby current is 2 μ A typically. The TC551001PL/FL has three control inputs. Chip enable inputs ($\overline{CE1}$, $\overline{CE2}$) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC551001PL/FL is suitable for use in various microprocessor application system where high speed, low power, and battery back up are required.

The TC551001PL/FL is offered in both a dual-in-line 32 pin standard plastic package and small-out line plastic flat package.

FEATURES

- Low Power Dissipation : 27.5 mW / MHz (Typ.)
- Standby Current : 100 μ A (Max.)
- 5 V Single Power Supply
- Power Down Feature : $\overline{CE1}$, $\overline{CE2}$
- Data retention Supply Voltage : 2.0 ~ 5.5 V
- Directly TTL Compatible : All Inputs and Outputs

• Access Time

	TC551001 PL/FL-85	TC551001 PL/FL-10
Access Time (max.)	85 ns	100 ns
$\overline{CE1}$ Access Time (max.)	85 ns	100 ns
$\overline{CE2}$ Access Time (max.)	85 ns	100 ns
$\overline{OE}$ Access Time (max.)	45 ns	50 ns

- Package : TC551001PL : DIP32-P-600
- TC551001FL : SOP32-P-525

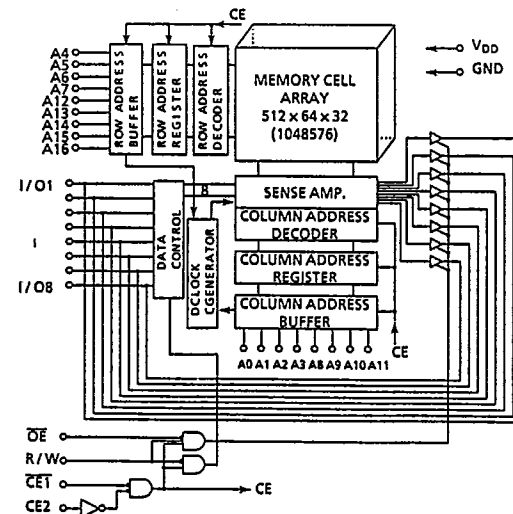
PIN CONNECTION (TOP VIEW)

N.C.	1	32	V_{DD}
A16	2	31	A15
A14	3	30	$\overline{CE2}$
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}$
A2	10	23	A10
A1	11	22	$\overline{CE1}$
A0	12	21	I/O8
I/O1	13	20	I/O7
I/O2	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4

PIN NAMES

A0~A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Input
I/O1~I/O8	Data Input/Output
V_{DD}	Power (+5 V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



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OPERATION MODE

OPERATION MODE	$\overline{CE1}$	$CE2$	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D _{OUT}	I _{DDO}
Write	L	H	*	L	D _{IN}	I _{DDO}
Output Deselect	L	H	H	H	High-Z	I _{DDO}
Standby	H	*	*	*	High-Z	I _{DDO}
	*	L	*	*	High-Z	I _{DDO}

* : H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{IO}	Input and Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{solder}	Soldering Temperature	260 ± 10	°C·sec
T _{strg.}	Storage Temperature	-55 ~ 150	°C
T _{opr.}	Operating Temperature	0 ~ 70	°C

* : -3.0 V at pulse width 50 ns MAX. ** : SOP

D.C. RECOMMENDED OPERATING CONDITIONS.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.3	
V _{IL}	Input Low Voltage	-0.3	-	0.8	
V _{DH}	Data Retention Supply Voltage	2.0	-	5.5	

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D.C. and OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	-	-	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{ V}$	-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{ V}$	4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	-	-	± 1.0	μA
I_{DD01}	Operating Current	$\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ and $R/W = V_{IH}$, $I_{OUT} = 0\text{ mA}$ Other Inputs = V_{IH}/V_{IL} $t_{\text{cycle}} = \text{Min. cycle}$	-	-	80	mA
I_{DD02}		$\overline{CE1} = 0.2\text{ V}$ and $CE2 = V_{DD} - 0.2\text{ V}$ $R/W = V_{DD} - 0.2\text{ V}$, $I_{OUT} = 0\text{ mA}$ Other Inputs = $V_{DD} - 0.2\text{ V}/0.2\text{ V}$ $t_{\text{cycle}} = \text{Min. cycle}$	-	-	70	mA
I_{DD51}	Standby Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$	-	-	3	mA
$I_{DD52}^{(1)}$		$\overline{CE1} = V_{DD} - 0.2\text{ V}$ or $CE2 = 0.2\text{ V}$ $V_{DD} = 2.0\text{ V} \sim 5.5\text{ V}$, $T_a = 0 \sim 70^\circ\text{C}$	-	2	100	μA

Note : (1) In standby mode with $\overline{CE1} \geq V_{DD} - 0.2\text{ V}$, these specification limits are guaranteed under the condition of $CE2 \geq V_{DD} - 0.2\text{ V}$ or $CE2 \leq 0.2\text{ V}$.

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

Note : This parameter periodically sampled is not 100 % tested.

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A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC551001PL-85 TC551001FL-85		TC551001PL-10 TC551001FL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	—	100	—	ns
t_{ACC}	Address Access Time	—	85	—	100	
t_{CO1}	$\overline{CE1}$ Access Time	—	85	—	100	
t_{CO2}	$CE2$ Access Time	—	85	—	100	
t_{OE}	Output Enable to Output in Valid	—	45	—	50	
t_{COE}	Chip Enable ($\overline{CE1}$, $CE2$) to Output in Low-Z	10	—	10	—	
t_{OEE}	Output Enable to Output in Low-Z	0	—	0	—	
t_{OD}	Chip Enable ($\overline{CE1}$, $CE2$) to Output in High-Z	—	30	—	35	
t_{ODO}	Output Enable to Output in High-Z	—	30	—	35	
t_{OH}	Output Data Hold Time	10	—	10	—	

Write Cycle

SYMBOL	PARAMETER	TC551001PL-85 TC551001FL-85		TC551001PL-10 TC551001FL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	—	100	—	ns
t_{WP}	Write Pulse Width	60	—	60	—	
t_{CW}	Chip Selection to End of Write	75	—	80	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	R/W to Output in High-Z	—	30	—	35	
t_{OEW}	R/W to Output in Low-Z	0	—	0	—	
t_{DS}	Data Setup Time	35	—	40	—	
t_{DH}	Data Hold Time	0	—	0	—	

A.C. TEST CONDITIONS

Output Load : 100 pF + 1 TTL Gate
 Input Pulse Level : 0.6 V, 2.4 V
 Timing Measurement V_{IN} : 0.8 V, 2.2 V
 Reference Level V_{OUT} : 0.8 V, 2.2 V
 t_r , t_f : 5 ns

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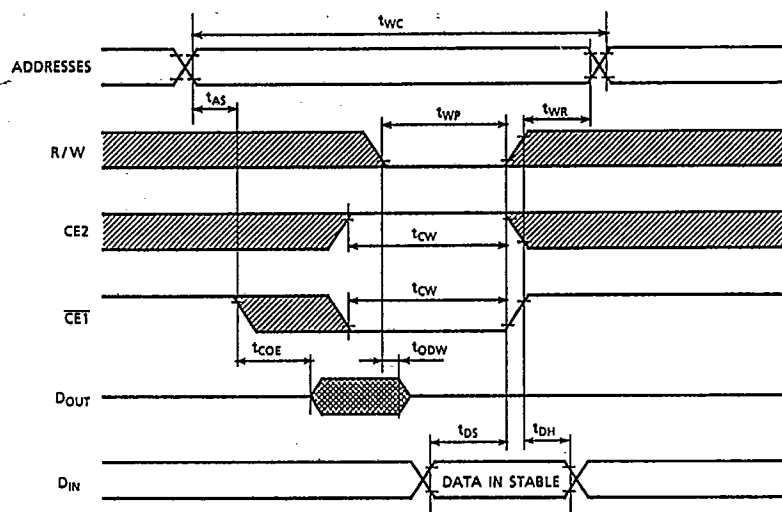
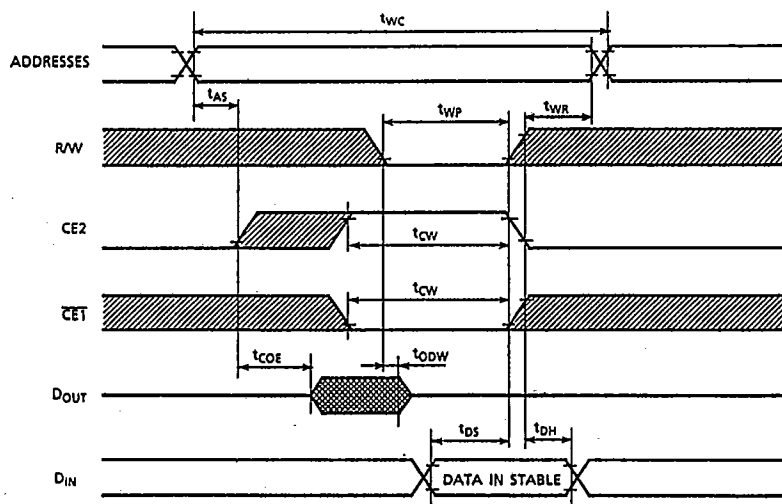
Read Cycle (1)



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WRITE CYCLE 2 (4) (CE1 Controlled Write)WRITE CYCLE 3 (4) (CE2 Controlled Write)

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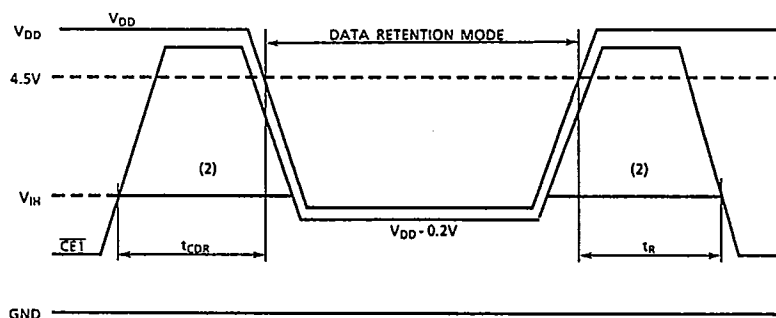
Note : (1) R/W is High for Read Cycle.

- (2) Assuming that $\overline{\text{CE1}}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
- (3) Assuming that $\overline{\text{CE1}}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.
- (4) Assuming that $\overline{\text{OE}}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{OH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DDS2}	Standby Current	$V_{DD} = 3.0\text{V}$	—	50	μA
		$V_{DD} = 5.5\text{V}$	—	100	
t_{CDR}	Chip Deselection to Data Retention Mode	0	—	—	nS
t_R	Recovery Time	5	—	—	mS

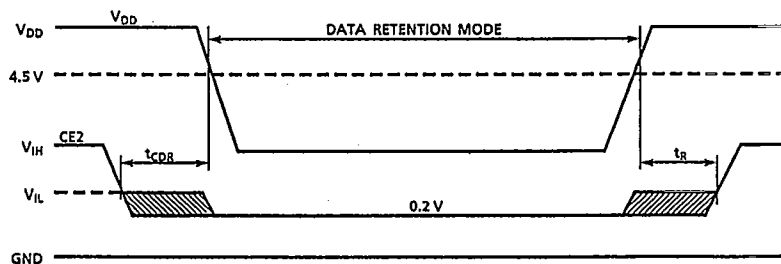
$\overline{\text{CE1}}$ Controlled Data Retention Mode (1)



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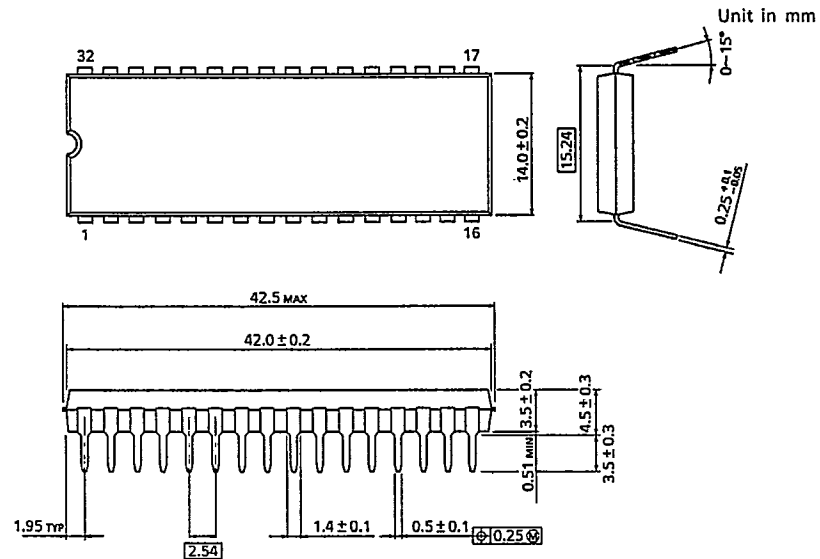
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CE2 Controlled Data Retention Mode (3)

- Note : (1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE2 \leq 0.2V$ or $CE2 \geq V_{DD} - 0.2V$.
- (2) If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDSI} current flows.
- (3) In $CE2$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE2 \leq 0.2V$.

OUTLINE DRAWING (DIP32 - P - 600)

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Weight : 4.53g (Typ.)

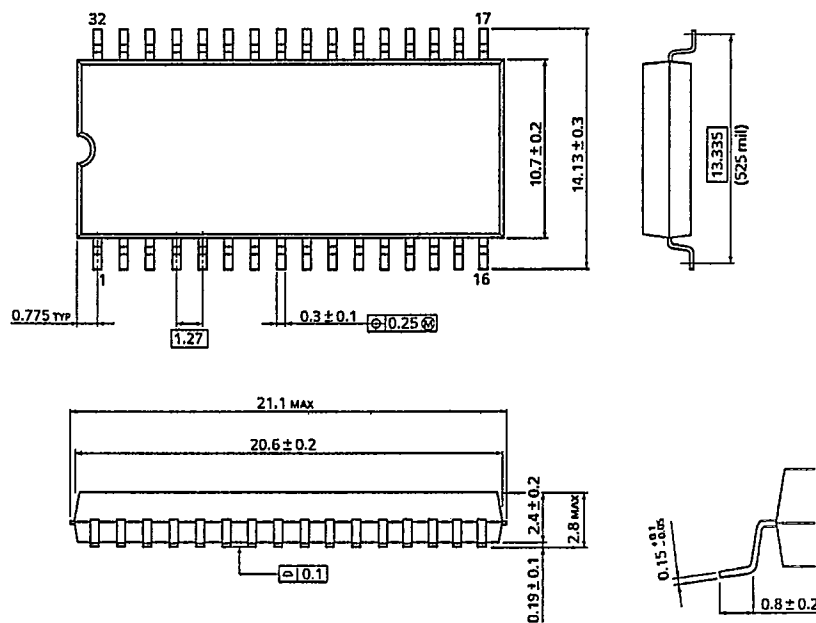
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OUTLINE DRAWING (SOP32 - P - 525)

Unit in mm



Weight : 1.10g (Typ.)