Bt438

250 MHz Clock Generator Chip for CMOS RAMDACs™

Distinguishing Features

- 250 MHz Operation
- Differential ECL Clock Generation
- Ability to Divide by 3, 4, 5, or 8 of the Clock
- Ability to Divide by 2 and 4 of the Load
- Ability to Reset Pipeline Delay of the RAMDAC
- 1.2 V Voltage Reference Output
- Single +5 V Power Supply
- 20-pin DIP or 28-pin PLCC Package
- Typical Power Dissipation: 325 mW

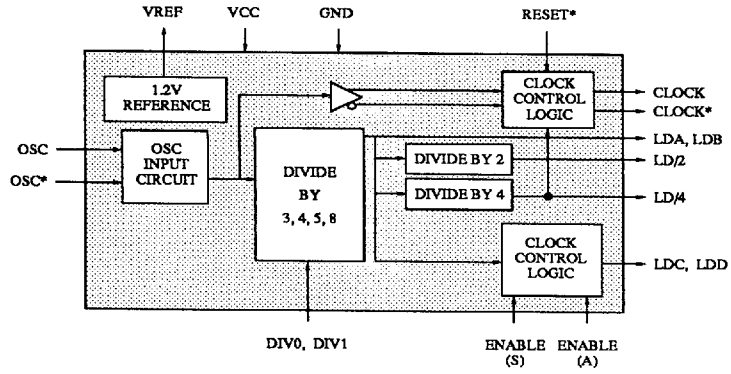
Customer Benefits

- Reduces PC Board Area
- Simplifies RAMDAC Design
- Reduces Cost over Discretes
- Increases System Reliability

Related Products

- Bt439
- Bt440

Functional Block Diagram



Product Description

The Bt438 is a clock generator for the high-speed Brooktree CMOS RAMDACs. It interfaces a 10KH ECL oscillator operating from a single +5 V supply to the RAMDAC, generating the necessary clock and control signals.

The clock output can be divided by 3, 4, 5, or 8 to generate the load signal. The load signal can also be divided by 2 and 4 to, for example, clock video timing logic.

A second load signal may be synchronously or asynchronously controlled to enable starting and stopping the clocking of the video DRAMs.

The Bt438 optionally configures the pipeline delay of the RAMDAC to a fixed pipeline delay.

An on-chip 1.2 V voltage reference is also provided, and may be used to provide the reference voltage for up to four RAMDACs.

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L438001 Rev. M

Brooktree®

Circuit Description

The Bt438 is designed to interface to a 10KH ECL crystal oscillator and generate the clock signals required by the RAMDACs. The OSC and OSC* inputs are designed to interface to a 10KH ECL oscillator operating from a single +5 V power supply.

The CLOCK and CLOCK* outputs are designed to interface directly to the CLOCK and CLOCK* inputs of the RAMDACs. The output levels are compatible with 10KH ECL logic operating from a single +5 V power supply.

DIV0 and DIV1 are used to specify whether the pixel clock is to be divided by 3, 4, 5, or 8 to generate the LDA and LDB signals. LDA is also divided by 2 and 4 to generate the LD/2 and LD/4 signals, respectively.

ENABLE (S) is internally synchronized to LDA and may be used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be logical zeros. ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the state they were in when the ENABLE (A) input went to a logical zero.

ENABLE (A) and ENABLE (S) should not be a logical zero simultaneously. If this occurs, synchronous control of LDC and LDD by ENABLE (S) is not guaranteed.

While both ENABLE (S) and ENABLE (A) are logical ones, LDC and LDD will be free running, and in phase with LDA and LDB. This architecture allows the shift registers of the video DRAMs to be optionally nonclocked during the retrace intervals. Figure 1 illustrates the ENABLE implementation within the Bt438, while Figure 2 shows the load output timing.

The RESET* input is designed to enable the Bt438 to set the pipeline delay of the RAMDACs to a specified number of clock cycles. (The exact number depends on the RAMDAC.) Following the first rising edge of LD/4 after the rising edge of RESET*, the CLOCK and CLOCK* outputs are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are restarted. Figure 3 shows the operation of the RESET* input.

The Bt438 also generates a 1.2 V (typical) voltage reference that may be used to drive the VREF input of up to four RAMDACs.

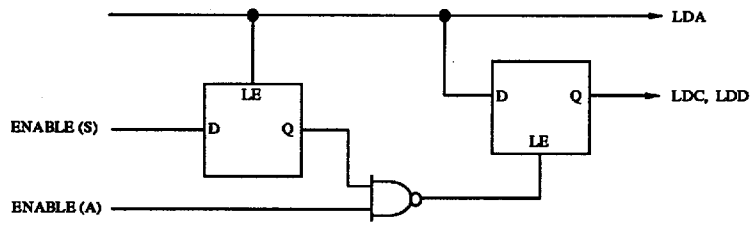


Figure 1. ENABLE Control Implementation.

Circuit Description *(continued)*

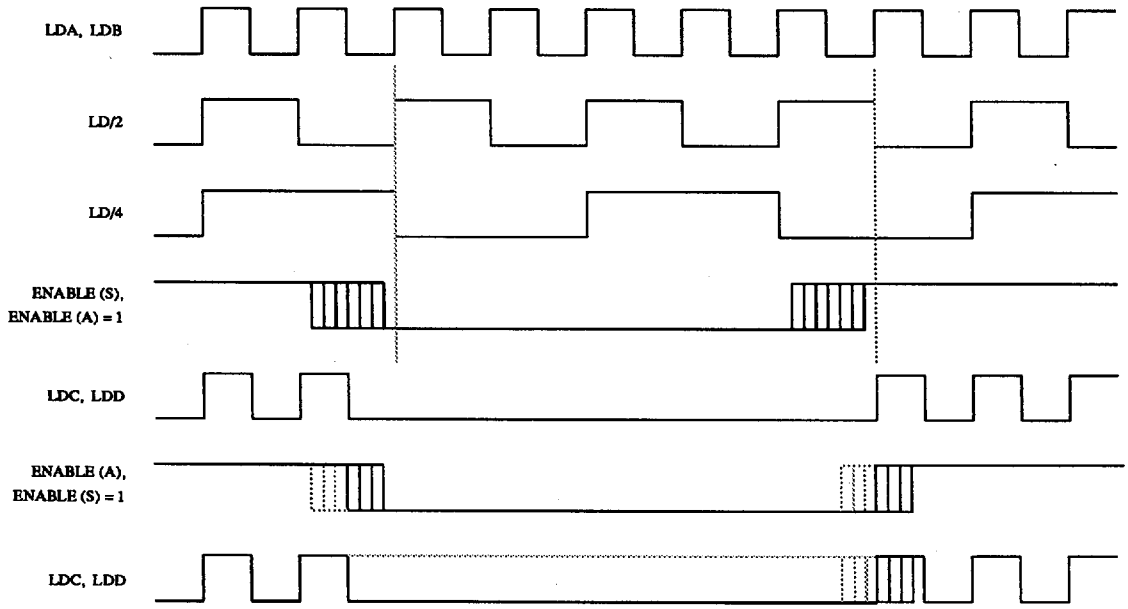


Figure 2. Load Output Timing.

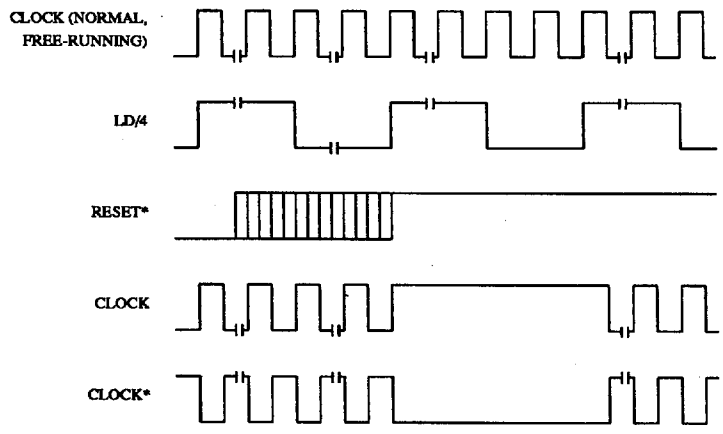


Figure 3. RESET* Timing.

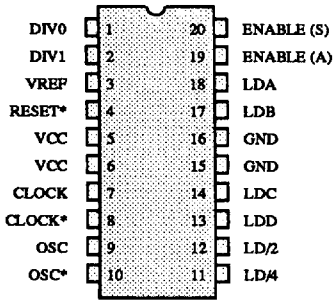
Pin Descriptions

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>VREF</td><td>Voltage reference output. This output provides a 1.2 V (typical) reference and may be used to drive the VREF input of up to four RAMDACs.</td></tr>
<tr><td>OSC, OSC*</td><td>Differential ECL oscillator inputs. These inputs are designed to interface to a 10KH ECL crystal oscillator operating from a single +5 V supply.</td></tr>
<tr><td>CLOCK, CLOCK*</td><td>Differential clock outputs. These outputs connect directly to the CLOCK and CLOCK* inputs of the RAMDAC. The clock rate is equal to the OSC rate, and these outputs can drive up to four RAMDACs directly. The output levels are equivalent to 10KH ECL logic operating from a single +5 V supply.</td></tr>
<tr><td>DIV0, DIV1</td><td>Divide control inputs (TTL compatible). These inputs specify the division factor (3, 4, 5, or 8) for the generation of the LDA and LDB signals, as specified below:
<table>
<tr><th>DIV1</th><th>DIV0</th><th>Division Factor</th><th>Clock Cycles Low</th><th>Clock Cycles High</th></tr>
<tr><td>0</td><td>0</td><td>÷3</td><td>1</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>÷4</td><td>2</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>÷5</td><td>2</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>÷8</td><td>4</td><td>4</td></tr>
</table></td></tr>
<tr><td>LDA, LDB</td><td>Load outputs (TTL compatible). LDA and LDB are generated by dividing CLOCK by 3, 4, 5, or 8, as determined by the DIV0 and DIV1 inputs.</td></tr>
<tr><td>LD/2</td><td>Load output (TTL compatible). LD/2 is generated by dividing LDA by 2.</td></tr>
<tr><td>LD/4</td><td>Load output (TTL compatible). LD/4 is generated by dividing LDA by 4.</td></tr>
<tr><td>LDC, LDD</td><td>Load outputs (TTL compatible). When both ENABLE inputs are a logical one, these outputs have the same timing as the LDA and LDB outputs.</td></tr>
<tr><td>ENABLE (S)</td><td>Synchronous load enable control input (TTL compatible). ENABLE (S) is internally synchronized to LDA, and is used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be logical zeros. While both ENABLE (A) and ENABLE (S) are logical ones, LDC and LDD are free-running and in phase with the LDA and LDB outputs.</td></tr>
<tr><td>ENABLE (A)</td><td>Asynchronous load enable control input (TTL compatible). ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the state they were in when the ENABLE (A) input went to a logical zero. While both ENABLE (A) and ENABLE (S) are logical ones, LDC and LDD are free running and in phase with the LDA and LDB outputs. Glitches should be avoided on this asynchronous input.</td></tr>
</table>

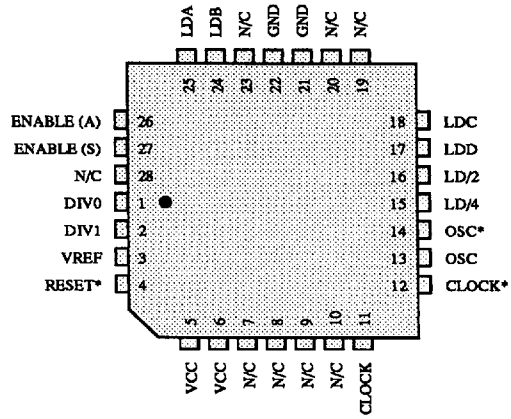
Pin Descriptions *(continued)*

Pin Name	Description
RESET*	Reset control input (TTL compatible). Following the first rising edge of LD/4 after the rising edge of RESET*, CLOCK and CLOCK* are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are set to be free running. Glitches should be avoided on this edge-triggered input.
VCC	Device power. All VCC pins must be connected.
GND	Device ground. All GND pins must be connected.

A 20-pin DIP Package



A 28-pin Plastic J-Lead (PLCC) Package



Note: N/C pins may be left floating without affecting the performance of the Bt438.

Application Information

Interfacing to the RAMDAC

Figure 4 illustrates interfacing the Bt438 to a RAMDAC when using a differential ECL oscillator. The Bt438 should be located as close as possible to the RAMDAC. The 220 Ω resistors at the oscillator should be located as close as possible to the OSC and OSC* outputs. The 150 Ω resistor at the Bt438 should be located as close as possible to the Bt438 OSC and OSC* inputs.

The 220 Ω resistors at the Bt438 should be located as close as possible to the Bt438 CLOCK and CLOCK* outputs. The 150 Ω resistor at the RAMDAC should be as close as possible to the CLOCK and CLOCK* inputs.

Figure 5 illustrates interfacing to a single-ended ECL oscillator.

Figure 6 shows interfacing to a TTL clock for applications less than 80 MHz. The +5 V of the resistor divider should be tied directly to the device +5 V. At VCC max, noise margin is at the minimum (100 mV).

Because of the inability to ensure proper synchronization between Bt438s, multiple devices should not be used in applications where multiple RAMDACs drive the same monitor.

A 1 kΩ resistor must be used to isolate the VREF output between multiple RAMDACs. This keeps noise on the Bt438 voltage reference from being coupled into the RAMDAC's VREF pin. The VREF input of the RAMDAC must still have a decoupling capacitor to VAA or GND, as specified in the RAMDAC's datasheet.

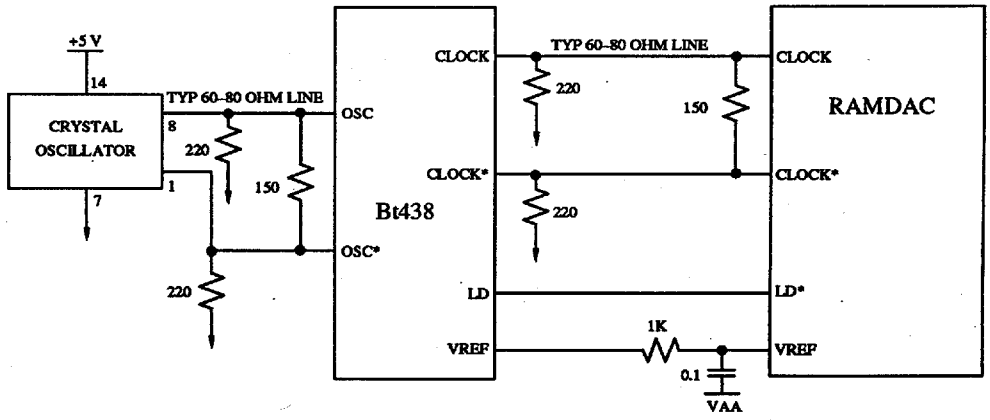


Figure 4. Interfacing to a Differential Crystal Oscillator.

Application Information *(continued)*

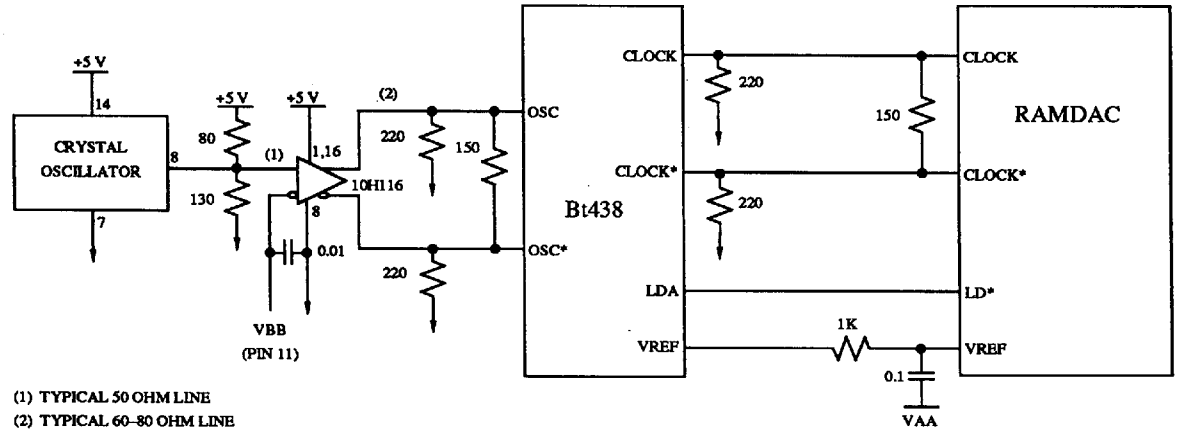


Figure 5. Interfacing to a Single-Ended Crystal Oscillator.

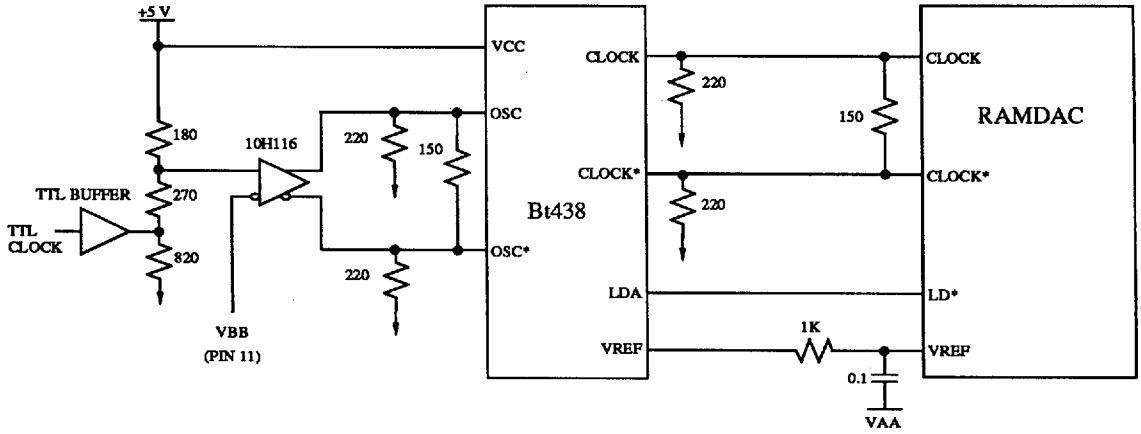


Figure 6. Interfacing to a TTL Clock.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
OSC/OSC* Duty Cycle		40			%

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	V
Voltage on any Pin		GND–0.5		VCC + 0.5	V
CLOCK, CLOCK* Output Current				30	mA
Ambient Operating Temperature Storage Temperature Junction Temperature Ceramic Package Plastic Package	TA TS TJ	–55 –65		+125 +150 +175 +150	°C °C °C °C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C
Air Flow		0			l.f.p.m.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification isnot implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL Inputs					
Input High Voltage (general)	VIH	2.0		VCC + 0.5	V
DIV0, DIV1		2.2		VCC + 0.5	V
RESET* (at 0 °C)		2.2		VCC + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			10	µA
Input Low Current (Vin = 0.4 V)	IIL			–0.7	mA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4		pF
ECL Inputs					
Input High Voltage	VIH	VCC–1.1		VCC–0.8	V
Input Low Voltage	VIL	GND–0.5		VCC–1.5	V
Input High Current (Vin = 4.0 V)	IIH			15	µA
Input Low Current (Vin = 0.4 V)	IIL			15	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CIN		4		pF
Load Outputs					
Output High Voltage (IOH =–2 mA)	VOH	2.4			V
Output Low Voltage (IOL = 20 mA)	VOL			0.65	V
Output Capacitance			10		pF
Clock Outputs					
Differential Output Voltage	ΔVOUT	0.6			V
Output Capacitance	COUT		7		pF
Voltage Reference					
Output Voltage (Bt438 Rev. C) (Note 1)	VREF	1.12	1.2	1.27	V
Output Current	IREF		100		µA
VCC Supply Current (Note 2)	ICC		65	85	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions." CLOCK and CLOCK* have 50 Ω to VCC–2 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: RSET of the RAMDAC should be adjusted because the output voltage of the Bt438 Rev. C is lower than the recommended VREF for the RAMDAC. $IOG\ (mA) = \frac{11294\ VREF}{RSET}$, IOG (typ) = 26.7 mA.

Note 2: Measured without 50 Ω to VCC–2 V on CLOCK and CLOCK*.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

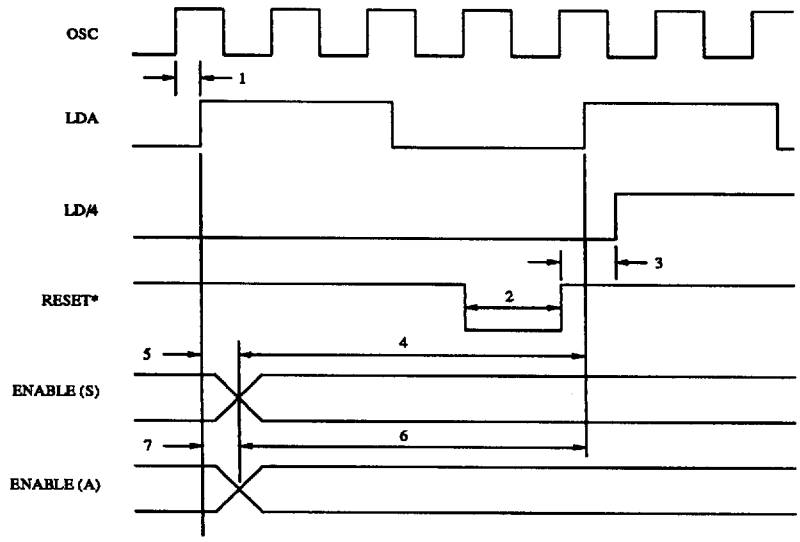
AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
OSC, OSC* Clock Rate	Fmax			250	MHz
LDA Output Delay (Note 1)	1		4	10	ns
LDA, LDB Pulse Width Low (Note 2)		5			ns
LDA to LDB Output Skew (Note 3)		–2.0	0	2.0	ns
LDA to LDC Output Skew (Note 3)		–1.0	1.5	4.0	ns
LDA to LD/2 Output Skew (Note 3)		0	1.5	5.0	ns
LDA to LD/4 Output Skew (Note 3)		0	1.5	6.0	ns
LDC to LDD Output Skew (Note 3)		–2.0	0	2.0	ns
RESET* Active Low Time	2	15			ns
RESET* Setup Time	3	12			ns
ENABLE (S) Setup Time	4	12			ns
ENABLE (S) Hold Time	5	–2			ns
ENABLE (A) Setup Time	6	12			ns
ENABLE (A) Hold Time	7	–2			ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions". CLOCK and CLOCK* have 50 Ω to VCC–2 V. TTL outputs have –2 mA/20 mA load applied with 1.5 V switching point. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between 10-percent and 90-percent points. ECL input values are VCC–1.8 to VCC–0.8 V with input rise/fall times ≤ 1 ns, measured between 20-percent and 80-percent points. Timing reference points at 50-percent for inputs and outputs, except TTL outputs measured at 1.5 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Output load = 50 pF.
Note 2: LD outputs not used in +3 over 200 MHz.
Note 3: LD outputs equally loaded. Unequal loading may result in additional output skew.

Timing Waveforms



Input/Output Timing

Ordering Information

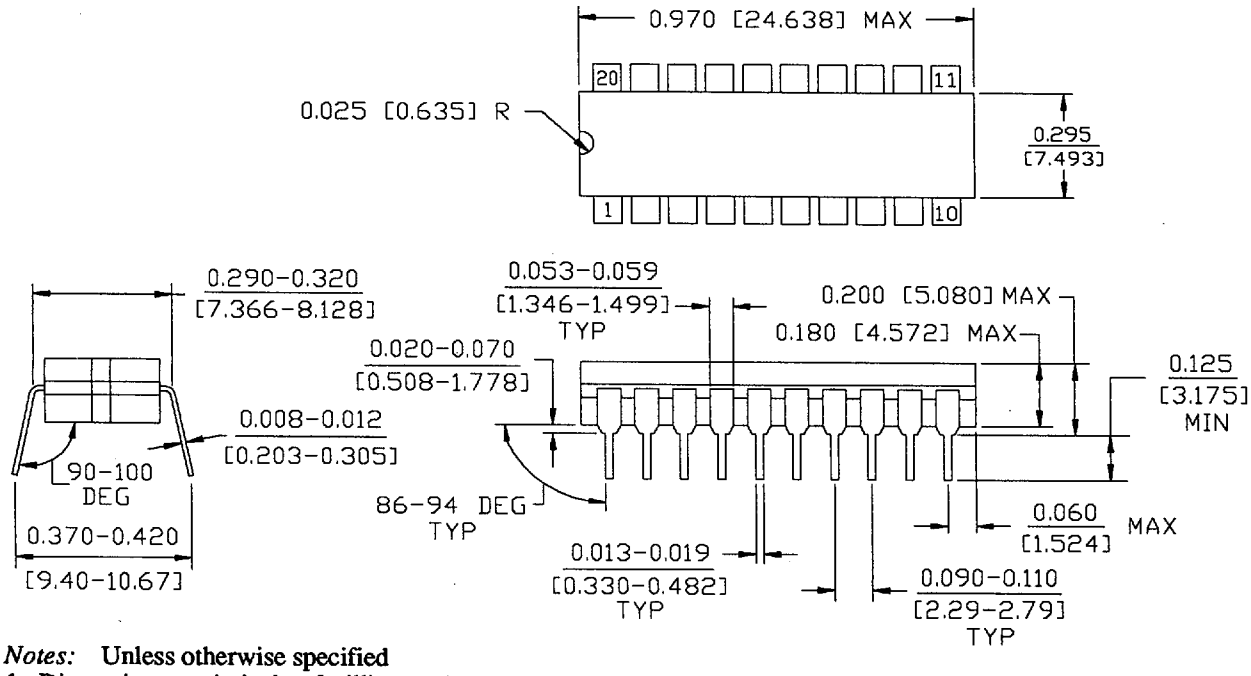
Model Number	Package	Ambient Temperature Range
Bt438KC	20-pin 0.3" CERDIP	0° to +70° C
Bt438KPJ	28-pin Plastic J-Lead	0° to +70° C

Revision History

Datasheet Revision	Change from Previous Revision
H	Thermal equilibrium notes added to Recommended Operating Conditions and DC Characteristic sections.
I	Rev. B silicon voltage reference limits changed.
J	Rev. C silicon voltage reference limits changed.
K	Datasheet status upgraded to Final. DIV0 and DIV1 added to DC Characteristics section.
L	Changed Load Outputs (TTL) VOL maximum from 0.8 V to 0.65 V. Added RESET* VIH 2.2 V minimum at 0 °C. Deleted "(at 25 °C)" note from ECL inputs and outputs.
M	Revised Figure 2. Revised the RAMDAC interface in the Application Information section and Figures 4, 5, and 6.

Device Revision	
C	VREF limits changed.

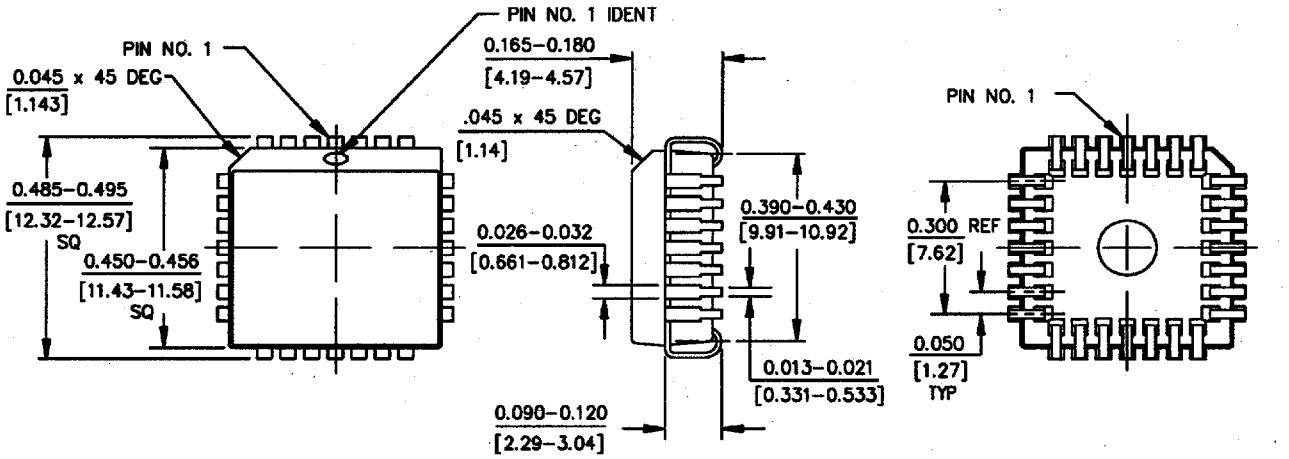
Package Drawing—20-pin 0.300" CERDIP



Notes: Unless otherwise specified

1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ± 0.005 [0.127].
3. Pins are intended for insertion in hole rows on 0.300" [7.62] centers.

Package Drawing—28-pin Plastic J-Lead (PLCC)



Notes: Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.