Bt9021

135 MHz Monolithic CMOS 256 x 24 Color Palette RAMDAC™

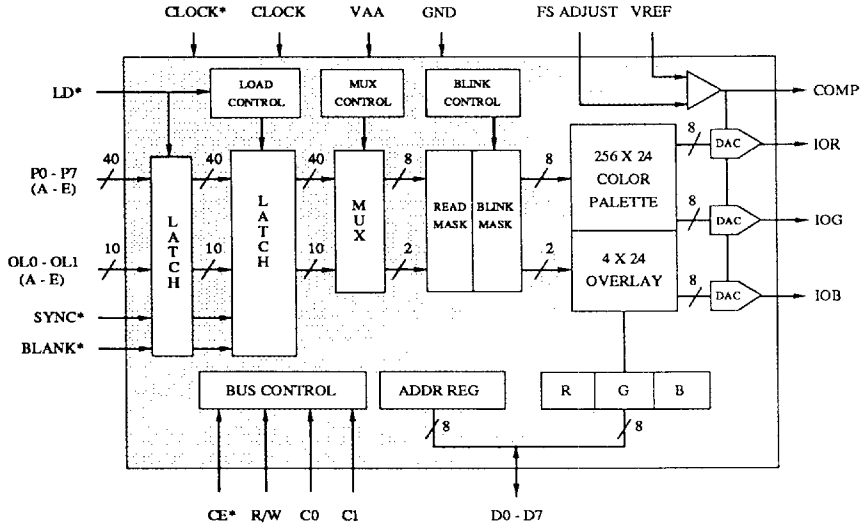
Distinguishing Features

- 135 MHz Pipelined Operation
- 1:1, 4:1, or 5:1 Multiplexed Pixel Ports
- Pixel Pan Support
- Frame Buffer Interleave Support
- Triple 8-bit D/A Converters
- 256 x 24 Dual Port Color Palette
- 4 x 24 Dual Port Overlay Registers
- RS-343A-Compatible Outputs
- Bit Plane Read and Blink Masks
- Standard MPU Interface
- 84-pin PGA, 84-pin J-Lead (PLCC) Packages
- +5 V CMOS Monolithic Construction

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Functional Block Diagram



Product Description

The Bt9021 RAMDAC is designed specifically as an upgrade for Bt458 high-performance, high-resolution color graphics. The architecture enables the display of 1280 x 1024 bit-mapped color graphics (up to 8 bits per pixel plus up to 2 bits of overlay information). This minimizes the use of costly ECL interfacing, as most of the high-speed (pixel clock) logic is contained on chip. The multiple pixel ports and internal multiplexing enables TTL-compatible interfacing to the frame buffer, while maintaining the 135 MHz video data rates required for sophisticated color graphics. Programmable 1:1, 4:1, and 5:1 input multiplexing of pixel and overlay data is supported. In addition to being Bt458 register and pin compatible, the Bt9021 contains pixel interleave and pixel panning features for improved graphics performance.

Features include a 256 x 24 color lookup table with triple 8-bit video D/A converters. On-chip features include programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port color palette RAM.

The Bt9021 generates RS-343A-compatible red, green, and blue video signals, and is capable of driving doubly-terminated 75-Ω coax directly, without requiring external buffering.

The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt9021 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and dual-port overlay registers allow color updating without contention with the display refresh process.

Table 1 shows the C0 and C1 control inputs in conjunction with the internal address register, that specify which control register, color palette RAM entry, or overlay register will be accessed by the MPU.

The 8-bit address register (ADDR0–7) is used to address the internal RAM and registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0.

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green, and blue data.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa and ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR0–7) are accessible to the MPU. ADDR0 corresponds to data bus bit D0.

For Bt458 compatibility, register locations $08 and $09 must be loaded with $00.

	Value	C1	C0	Addressed by MPU
ADDRa, b (counts modulo 3)	00	x	1	red value
	01	x	1	green value
	10	x	1	blue value
ADDR0–7 (counts binary)	$00–$FF	0	1	color palette RAM
	$00	1	1	overlay color 0
	$01	1	1	overlay color 1
	$02	1	1	overlay color 2
	$03	1	1	overlay color 3
	$04	1	0	read mask register
	$05	1	0	blink mask register
	$06	1	0	command register
	$07	1	0	test register
	$08	1	0	pan/zoom register
	$09	1	0	interleave register

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Additional Information

Although the color palette RAM and overlay registers are dual-ported, it is possible for one or more of the pixels on the display screen to be disturbed if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the blue write cycle. A maximum of 1 pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers is also done through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing when accessing the Bt9021.

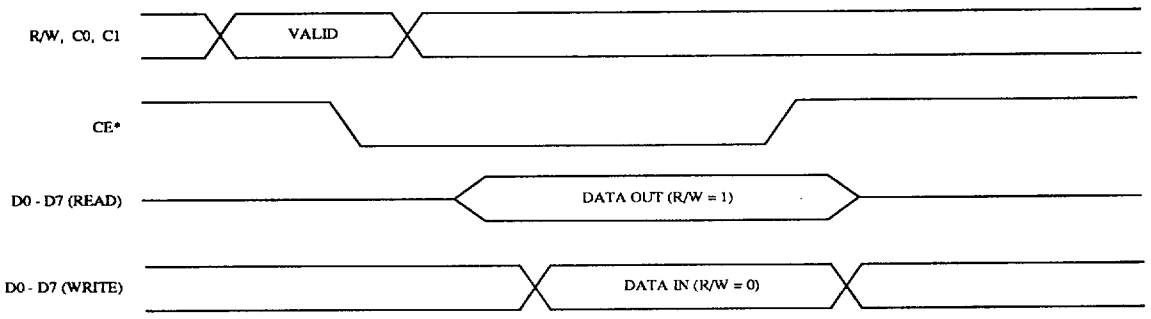


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt9021 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color (up to 8 bits per pixel), and overlay (up to 2 bits per pixel) information, for either 1, 4, or 5 consecutive pixels, are latched into the device. Note that with this configuration, the sync and blank timing will be recognized only with 1-, 4-, or 5-pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing.

For 4:1 or 5:1 input multiplexing, the Bt9021 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, etc., until all 4 or 5 pixels have been output, at which point the cycle repeats. In 1:1 input multiplexing mode, the {B}, {C}, {D}, and {E} inputs are ignored.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external character or cursor generation logic.

To simplify the frame buffer interface timing, LD* may be phase shifted in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by 1, 4, or 5, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than 4, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every 4 clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every 5 clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

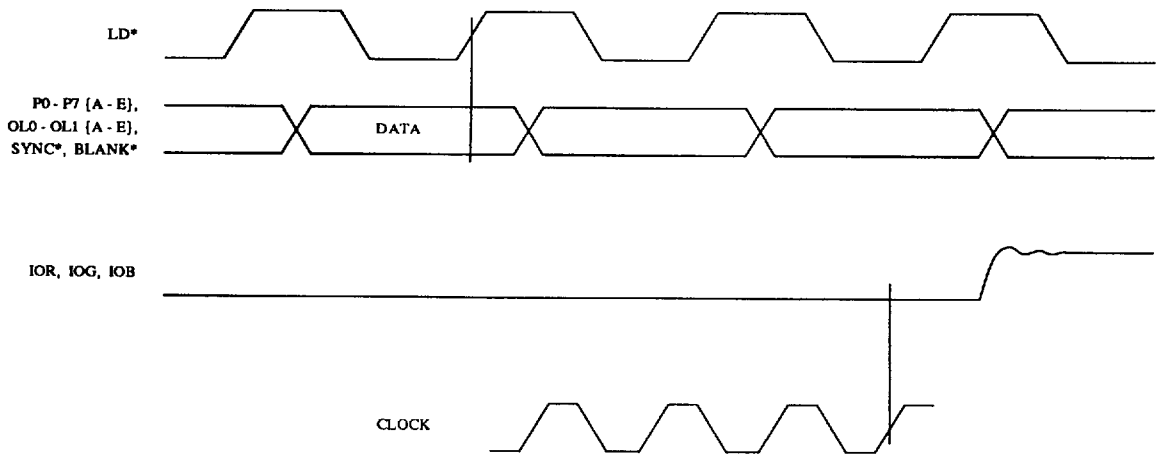


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

If 1:1 multiplexing is specified, LD* is also used for clocking the Bt9021 (at a maximum of 66 MHz). The rising edge of LD* still latches the P0–P7, OL0–OL1, SYNC*, and BLANK* inputs. However, analog information is output following the rising edge of LD* rather than CLOCK. Note that CLOCK must still run, but is ignored.

Color Selection

Each clock cycle, 8 bits of color information (P0–P7) and 2 bits of overlay information (OL0, OL1) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt9021 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval is recognized by determining that BLANK* has been a logical zero for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAM. Table 2 illustrates the truth table used for color selection.

Pixel Panning

To support pixel panning, command register1 specifies by how many clock cycles to pan. Both the P0–P7 and OL0–OL1 inputs are panned by delaying the SYNC* and BLANK* signals an additional 1, 2, 3, or 4 clock cycles.

If 0 pixel panning is specified, pixel {A} is output first, followed by pixel {B}, etc., until all 3, 4, or 5 pixels have been output, at which point the cycle repeats.

If 1-pixel panning is specified, pixel {B} will be first, followed by pixel {C}, etc. Pixel {A} will have been processed during the last clock cycle of the blanking interval, and will not be seen on the display screen. At the end of the active display line, pixel {A} will be output. Pixels {B}, {C}, {D}, and {E} will be output during the blanking interval, and will not be seen on the display screen.

The process is similar for panning by 2, 3, or 4 pixels.

Note that when a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt9021 during the first LD* cycle in which BLANK* is a logical zero.

Panning does not operate in the 1:1 multiplex mode.

CR6	OL1	OL0	P0–P7	Addressed by frame buffer
1	0	0	$00	color palette entry $00
1	0	0	$01	color palette entry $01
:	:	:	:	:
1	0	0	$FF	color palette entry $FF
0	0	0	$xx	overlay color 0
x	0	1	$xx	overlay color 1
x	1	0	$xx	overlay color 2
x	1	1	$xx	overlay color 3

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)

Video Generation

Every clock cycle, the selected 24 bits of color information (8 bits each of red, green, and blue) are presented to the three 8-bit D/A converters.

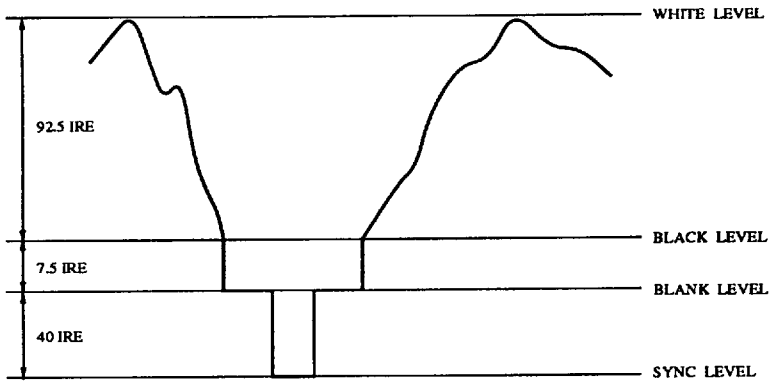
The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately-weighted currents to the analog outputs. This produces the specific output levels required for video applications, as illustrated in Figure 3.

The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Note that only the green output (IOG) contains sync information. Table 3 details how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt9021 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full-scale output current against temperature and power supply variations.

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75-Ω doubly-terminated load, RSET = 523 Ω, VREF = 1.235 V. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 523 Ω, VREF = 1.235 V.

Table 3. Video Output Truth Table.

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. CR0 corresponds to data bus bit D0.

CR07 Multiplex select

(0) 4:1 multiplexing
(1) 5:1 multiplexing

This bit specifies whether 4:1 or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and {E} overlay inputs are ignored and should be connected to GND, and the LD* input should be one fourth of the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be one fifth of the CLOCK rate.

CR06 RAM enable

(0) use overlay color 0
(1) use color palette RAM

When the overlay select bits are 00, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information.

CR05, CR04 Blink rate selection

(00) 16 on, 48 off (25/75)
(01) 16 on, 16 off (50/50)
(10) 32 on, 32 off (50/50)
(11) 64 on, 64 off (50/50)

These two bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off).

CR03 OL1 blink enable

(0) disable blinking
(1) enable blinking

If a logical one, this bit forces the OL1 {A–E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL1 {A–E} inputs. In order for overlay 1 bit plane to blink, bit CR1 must be set to a logical one.

CR02 OL0 blink enable

(0) disable blinking
(1) enable blinking

If a logical one, this bit forces the OL0 {A–E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL0 {A–E} inputs. In order for overlay 0 bit plane to blink, bit CR0 must be set to a logical one.

Internal Registers (continued)

Command Register (continued)

CR01	OL1 display enable (0) disable (1) enable	If a logical zero, this bit forces the OL1 {A–E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL1 {A–E} inputs.
CR00	OL0 display enable (0) disable (1) enable	If a logical zero, this bit forces the OL0 {A–E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL0 {A–E} inputs.

Read Mask Register

The read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. D0 corresponds to bit plane 0 (P0 {A–E}) and D7 corresponds to bit plane 7 (P7 {A–E}). Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized.

Blink Mask Register

The blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by the command register. D0 corresponds to bit plane 0 (P0 {A–E}) and D7 corresponds to bit plane 7 (P7 {A–E}). In order for a bit plane to blink, the corresponding bit in the read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized.

Internal Registers (continued)

Pan Register

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR17–CR15 Pan select

(000) 0 pixels
(001) 1 pixel
(010) 2 pixels
(011) 3 pixels
(100) 4 pixels
(101) reserved
:
(111) reserved

These bits specify the number of pixels to be panned and are typically modified only during the vertical retrace interval. They should be set immediately upon power-up to ensure that sync pulses reach the monitor.

Pan select should be set to 0 pixel mode (000) when utilizing the 1:1 MUX mode.

CR14–CR10 Reserved (logical zero)

Internal Registers (continued)

Interleave Register

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0. CR14–CR11 are always a logical zero.

CR17–CR15 Interleave select

(000) 0 pixels
(001) 1 pixel
(010) 2 pixels
(011) 3 pixels
(100) 4 pixels
(101) reserved
(110) reserved
(111) reserved

These bits specify the order in which the pixels are to be output. The order is repeated every LD* cycle for a given scan line. Thus, if the output sequence is DABC, it is that sequence for all pixels on that scan line.

The phrase "repeats every x" in the table below means that the output sequence repeats every x scan lines. Thus, for 4:1 multiplexing and a 1 pixel interleave select, ABCD would be repeated every fourth scan line.

	5:1 muxltiplexing		4:1 muxltiplexing	
interleave select	output sequence	scan line number	output sequence	scan line number
0	ABCDE	each line	ABCD	each line
1	ABCDE BCDEA CDEAB DEABC EABCD	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD BCDA CDAB DABC	n n + 1 n + 2 n + 3 (repeats every 4)
2	ABCDE CDEAB EABCD BCDEA DEABC	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD CDAB ABCD CDAB	n n + 1 n + 2 n + 3 (repeats every 2)
3	ABCDE DEABC BCDEA EABCD CDEAB	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD DABC CDAB BCDA	n n + 1 n + 2 n + 3 (repeats every 4)
4	ABCDE EABCD DEABC CDEAB BCDEA	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	invalid	invalid

Internal Registers (continued)

Interleave Register (continued)

CR14–CR12 First pixel select

(000) pixel {A}
(001) pixel {B}
(010) pixel {C}
(011) pixel {D}
(100) pixel {E} (5:1 only)
(101) reserved
(110) reserved
(111) reserved

These bits are used to support panning in the Y direction with an interleaved frame buffer. These bits are ignored in the 1:1 multiplex mode.

Due to the interleave capability, it is necessary to specify the value of the first pixel on the first scan line following a vertical retrace. The pixel {E} selection is only used in the 5:1 multiplex mode.

In the 1:1 multiplex mode, pixel {A} must be selected.

CR11 reserved (logical zero)

CR20 1:1 multiplex select

(1) 1:1 multiplex
(0) 4:1 or 5:1 multiplex

This bit specifies if 1:1 multiplexing is to be used on the P0–P7 and OL0–OL1 inputs. A logical zero selects either 4:1 or 5:1 multiplexing as selected by CR07 in the command register.

Note that in the 1:1 multiplex mode, the maximum clock rate is 66 MHz. LD* is used for the pixel clock. Although CLOCK is ignored in the 1:1 mode, it must remain running.

Internal Registers (continued)

Test Register

The test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converters. It may be written to or read by the MPU at any time, and is not initialized. When writing to the register, the upper 4 bits (D4–D7) are ignored.

The contents of the test register are defined as follows:

D7–D4	color information (4 bits of red, green, or blue)
D3	low (logical one) or high (logical zero) nibble
D2	blue enable
D1	green enable
D0	red enable

To use the test register, the host MPU writes to it, setting 1, and only 1, of the (red, green, blue) enable bits. These bits specify which 4 bits of color information the MPU wishes to read (R0–R3, G0–G3, B0–B3, R4–R7, G4–G7, or B4–B7). When the MPU reads the test register, the 4 bits of color information from the DAC inputs are contained in the upper 4 bits, and the lower 4 bits contain the enable information (red, green, blue, low or high nibble) previously written. Note that either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

For example, to read the upper 4 bits of red color information being presented to the D/A converters, the MPU writes to the test register, setting only the red enable bit. The MPU then proceeds to read the test register, keeping the pixel data stable, which results in D4–D7 containing R4–R7 color bits, and D0–D3 containing enable information (red, green, blue, low or high nibble), as illustrated below:

D7	R7
D6	R6
D5	R5
D4	R4
D3	0
D2	0
D1	0
D0	1

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Table 3. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 3). SYNC* does not override any other control or data input, as shown in Table 3. Therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0–P7 {A–E}, OL0–OL1 {A–E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is either equal to the CLOCK rate, or is one fourth or one fifth of the CLOCK rate, may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the AC Characteristics section.
P0–P7 {A–E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. Either 1, 4, or 5 consecutive pixels (up to 8 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Note that the {A} pixel is output first, followed by the {B} pixel, etc., until all 1, 4, or 5 pixels have been output, at which point the cycle repeats.
OL0– OL1 {A–E}	Overlay select inputs (TTL compatible). These control inputs are latched on the rising edge of LD*, and in conjunction with bit 6 of the command register, specify which palette is to be used for color information, as follows:

OL1	OL0	CR6 = 1	CR6 = 0
0	0	color palette RAM	overlay color 0
0	1	overlay color 1	overlay color 1
1	0	overlay color 2	overlay color 2
1	1	overlay color 3	overlay color 3

When accessing the overlay palette, the P0–P7 {A–E} inputs are ignored. Overlay information bits (up to 2 bits per pixel) for either 1, 4, or 5 consecutive pixels are input through this port. Unused inputs should be connected to GND.

IOR, IOG, IOB	Red, green, and blue video current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75-Ω coaxial cable (Figure 4).
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 4). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum, and maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. Refer to PC Board Layout Considerations for critical layout criteria.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 4). Note that the IRE relationships in Figure 3 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is: RSET (Ω) = 11,294 * VREF (V) / IOG (mA) The full-scale output current on IOR and IOB for a given RSET is: IOR, IOB (mA) = 8,067 * VREF (V) / RSET (Ω)
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 4, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 4. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (Figure 1). Care should be taken to avoid glitches on this edge triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

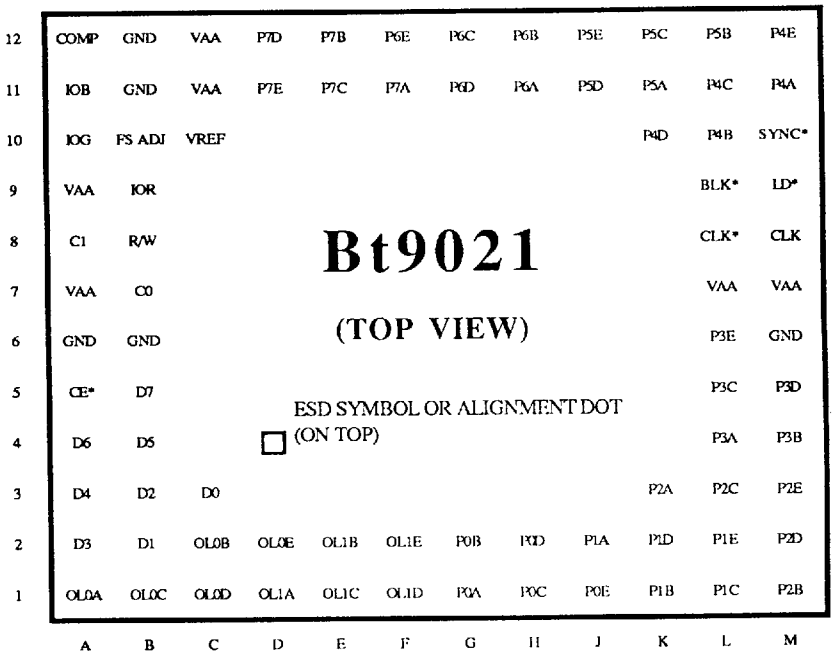
Pin Descriptions (continued)—84-pin PGA Package

Signal	Pin Number
BLANK*	L9
SYNC*	M10
LD*	M9
CLOCK*	L8
CLOCK	M8
P0A	G1
P0B	G2
P0C	H1
P0D	H2
P0E	J1
P1A	J2
P1B	K1
P1C	L1
P1D	K2
P1E	L2
P2A	K3
P2B	M1
P2C	L3
P2D	M2
P2E	M3
P3A	L4
P3B	M4
P3C	L5
P3D	M5
P3E	L6
P4A	M11
P4B	L10
P4C	L11
P4D	K10
P4E	M12

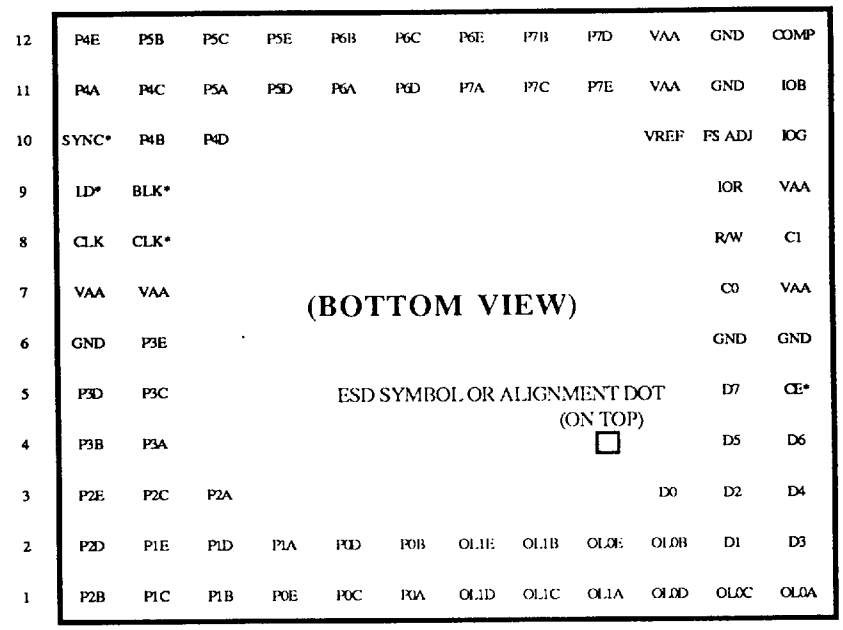
Signal	Pin Number
P5A	K11
P5B	L12
P5C	K12
P5D	J11
P5E	J12
P6A	H11
P6B	H12
P6C	G12
P6D	G11
P6E	F12
P7A	F11
P7B	E12
P7C	E11
P7D	D12
P7E	D11
OL0A	A1
OL0B	C2
OL0C	B1
OL0D	C1
OL0E	D2
OL1A	D1
OL1B	E2
OL1C	E1
OL1D	F1
OL1E	F2
IOG	A10
IOB	A11
IOR	B9

Signal	Pin Number
VAA	C12
VAA	C11
VAA	A9
VAA	L7
VAA	M7
VAA	A7
GND	B12
GND	B11
GND	M6
GND	B6
GND	A6
COMP	A12
FS ADJUST	B10
VREF	C10
CE*	A5
R/W	B8
C1	A8
C0	B7
D0	C3
D1	B2
D2	B3
D3	A2
D4	A3
D5	B4
D6	A4
D7	B5

Pin Descriptions (continued)—84-pin PGA Package

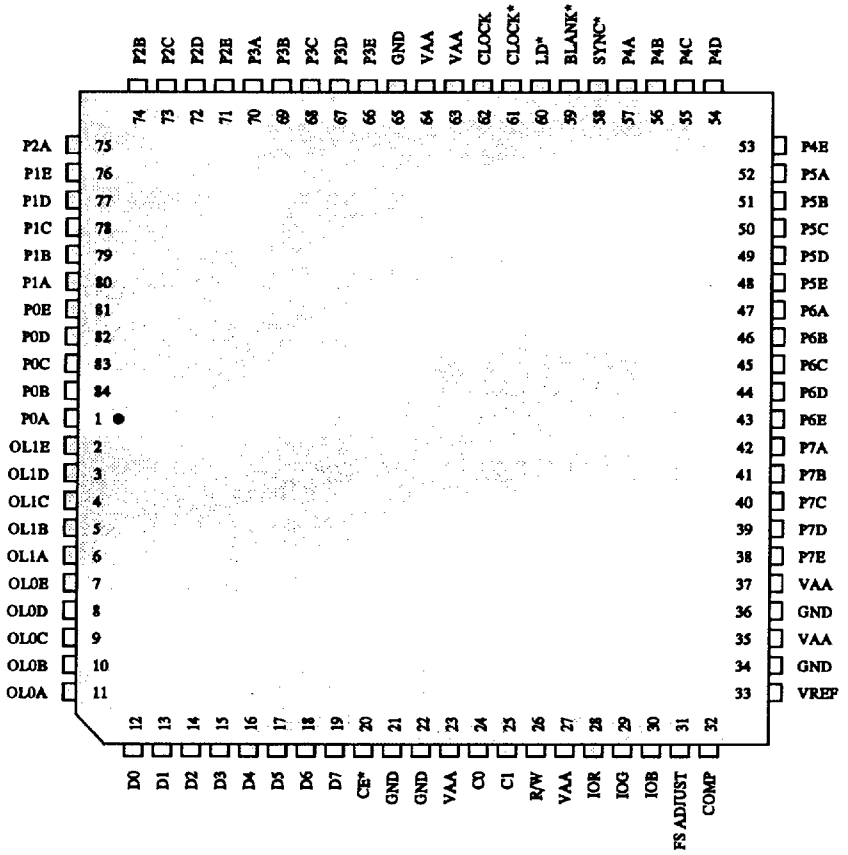


	A	B	C	D	E	F	G	H	J	K	L	M
12	COMP	GND	VAA	P7D	P7B	P6E	P6C	P6B	P5E	P5C	P5B	P4E
11	IOB	GND	VAA	P7E	P7C	P7A	P6D	P6A	P5D	P5A	P4C	P4A
10	IOG	FS ADJ	VREF							P4D	P4B	SYNC*
9	VAA	IOR									BLK*	LD*
8	C1	R/W									CLK*	CLK
7	VAA	C0									VAA	VAA
6	GND	GND									P3E	GND
5	CE*	D7									P3C	P3D
4	D6	D5									P3A	P3B
3	D4	D2	D0							P2A	P2C	P2E
2	D3	D1	OL0B	OL0E	OL1B	OL1E	P0B	P0D	P1A	P1D	P1E	P2D
1	OL0A	OL0C	OL0D	OL1A	OL1C	OL1D	P0A	P0C	P0E	P1B	P1C	P2B



	M	L	K	J	H	G	F	E	D	C	B	A
12	P4E	P5B	P5C	P5E	P6B	P6C	P6E	P7B	P7D	VAA	GND	COMP
11	P4A	P4C	P5A	P5D	P6A	P6D	P7A	P7C	P7E	VAA	GND	IOB
10	SYNC*	P4B	P4D							VREF	FS ADJ	IOG
9	LD*	BLK*									IOR	VAA
8	CLK	CLK*									R/W	C1
7	VAA	VAA									C0	VAA
6	GND	P3E									GND	GND
5	P3D	P3C									D7	CE*
4	P3B	P3A									D5	D6
3	P2E	P2C	P2A							D0	D2	D4
2	P2D	P1E	P1D	P1A	P0D	P0B	OL1E	OL1B	OL0E	OL0B	D1	D3
1	P2B	P1C	P1B	P0E	P0C	P0A	OL1D	OL1C	OL1A	OL0D	OL0C	OL0A

Pin Descriptions (continued)—84-Pin J-Lead Package



PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in "Bt451/457/458 Evaluation Module Operation and Measurements," application note (AN-16). This application note can be found in Brooktree's *1990 Applications Handbook*.

The layout should be optimized for lowest noise on the Bt9021 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminate digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a 6-layer PC board is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferably analog ground plane), layer 3 the analog power plane, and using the remaining layers for digital traces and digital power supplies.

The optimum layout enables the Bt9021 to be located as close to the power supply connector and the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground partitioning isolation technique is constrained by the noise margin degradation during digital readback of the Bt9021.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and VREF circuitry should be used, as shown in Figure 4. Another isolated ground plane is used for the GND pins of the Bt9021 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt9021 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within 3 inches of the Bt9021 and provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each of three groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 33 µF capacitor is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance so that the self-resonance frequency is greater than the LD* frequency.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt9021 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit by using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than one fourth the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10–50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10–50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt9021 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt9021 to minimize reflections. Unused analog outputs should be connected to GND.

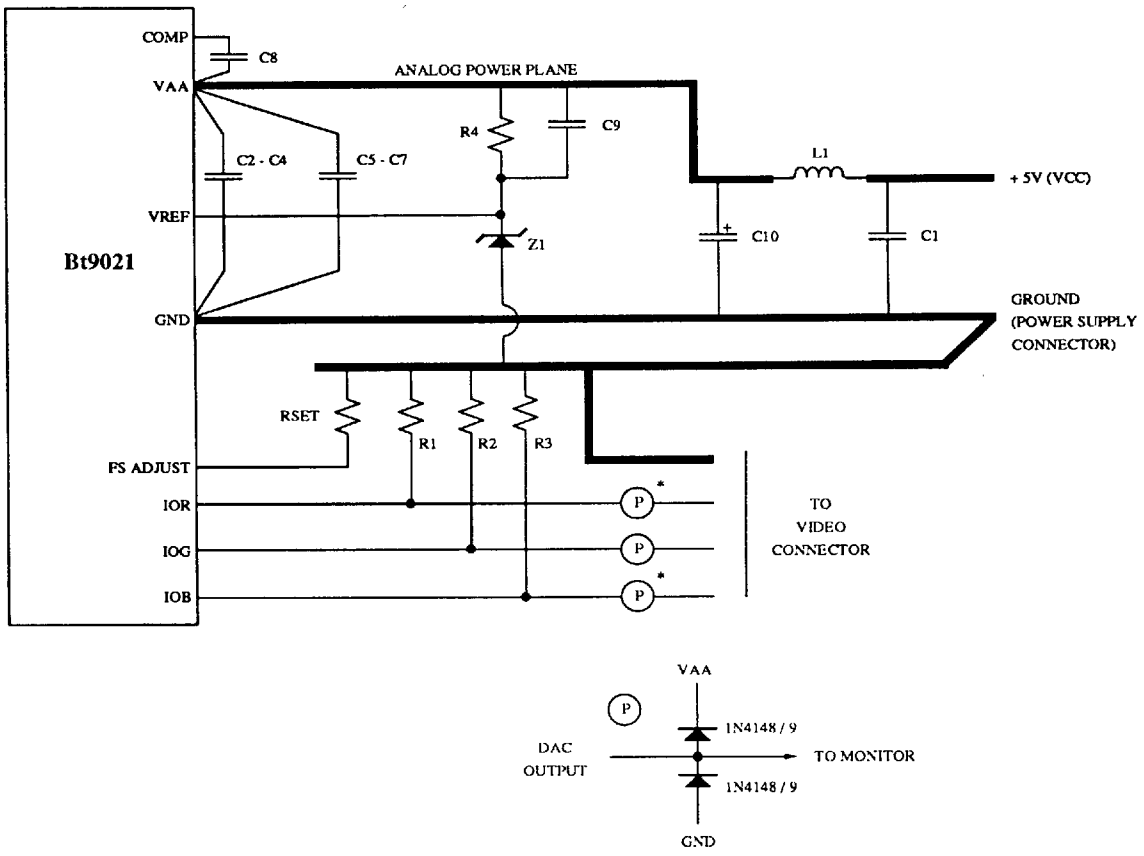
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

Analog Output Protection

The Bt9021 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 4 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1–C4, C8, C9	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5–C7	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C10	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt9021.

Figure 4. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Due to the high clock rates at which the Bt9021 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (220-Ω resistor to VCC and a 330-Ω resistor to GND). The termination resistors should be as close as possible to the Bt9021.

The CLOCK and CLOCK* inputs must be differential signals due to the noise margins of the CMOS process. The Bt9021 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by four or five (depending on whether 4:1 or 5:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

It is recommended that the Bt438 Clock Generator chip be used to generate the clock and load signals. It supports both the 4:1 and 5:1 input multiplexing of the Bt9021, and will also optionally set the pipeline delay of the Bt458 to 8 clock cycles. The Bt438 may also be used to interface the Bt9021 to a TTL clock. Figure 5 illustrates use of the Bt438 with the Bt9021.

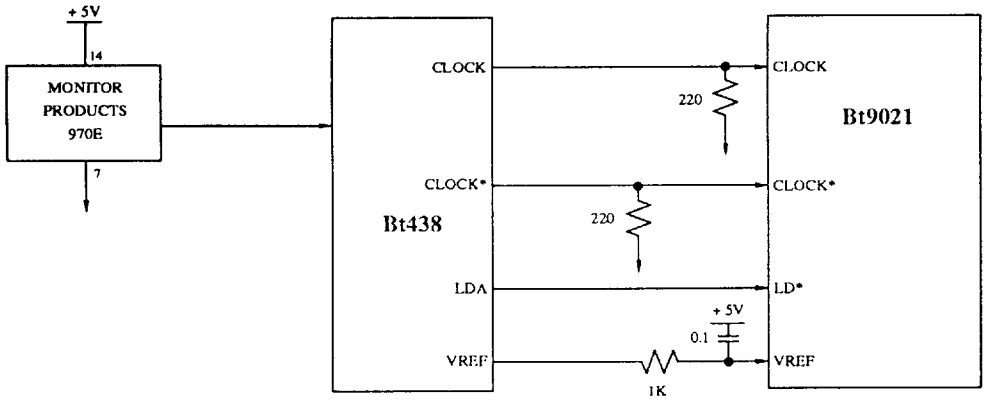


Figure 5. Generating the Bt9021 Clock Signals.

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt9021, although fixed after a power-up condition, may be anywhere from 6–10 clock cycles. The Bt9021 contains additional circuitry enabling the pipeline delay to be fixed at 8 clock cycles. The Bt438 Clock Generator chip supports this mode of operation when used with the Bt9021.

To reset the Bt9021, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for *at least* three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

The resetting of the Bt9021 to an 8 clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if multiple Bt9021s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	V
FS ADJUST Resistor	RSET		523		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	V
Voltage on any Digital Pin		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Input High Voltage	VKIH	VAA–1.0		VAA + 0.5	V
Input Low Voltage	VKIL	GND–0.5		VAA – 1.6	V
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –800 µA)	VOH	2.4			V
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	V
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	−1.0		+1.2	V
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		%/% ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax				
1:1 multiplexing				135	MHz
4:1 or 5:1 multiplexing				135	MHz
LD* Rate	LDmax				
1:1 multiplexing				66	MHz
4:1 multiplexing				33.75	MHz
5:1 multiplexing				27	MHz
R/W, C0, C1 Setup Time	1	0			ns
R/W, C0, C1 Hold Time	2	15			ns
CE* Low Time	3	50			ns
CE* High Time	4	25			ns
CE* Asserted to Data Bus Driven	5	10			ns
CE* Asserted to Data Valid	6			75	ns
CE* Negated to Data Bus 3-Stated	7			15	ns
Write Data Setup Time	8	35			ns
Write Data Hold Time	9	3			ns
Pixel and Control Setup Time	10	3			ns
Pixel and Control Hold Time	11	2			ns
Clock Cycle Time	12	7.4			ns
Clock Pulse Width High Time	13	3			ns
Clock Pulse Width Low Time	14	3			ns
LD* Cycle Time	15				
1:1 multiplexing		15.15			ns
4:1 multiplexing		29.6			ns
5:1 multiplexing		37			ns
LD* Pulse Width High Time	16				
1:1 multiplexing		6			ns
4:1 or 5:1 multiplexing		13			ns
LD* Pulse Width Low Time	17				
1:1 multiplexing		6			ns
4:1 or 5:1 multiplexing		13			ns
Analog Output Delay	18		20		ns
Analog Output Rise/Fall Time	19		2		ns
Analog Output Settling Time	20		8		ns
Clock and Data Feedthrough*			35		pV - sec
Glitch Impulse*			50		pV - sec
Analog Output Skew			0	2	ns
Pipeline Delay		6		10	Clocks
VAA Supply Current**	IAA		310	345	mA

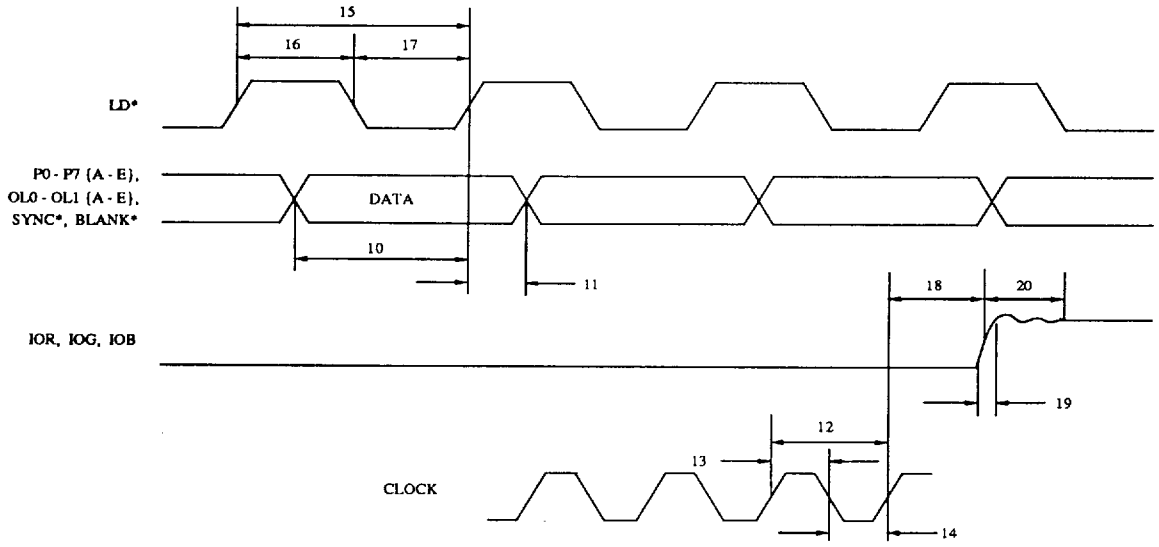
See test conditions on next page.

AC Characteristics (continued)

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA –0.8 to VAA –1.8 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 6. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 k-Ω resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**at Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C. IAA (max) at VAA = 5.25 V, TA = 0° C.



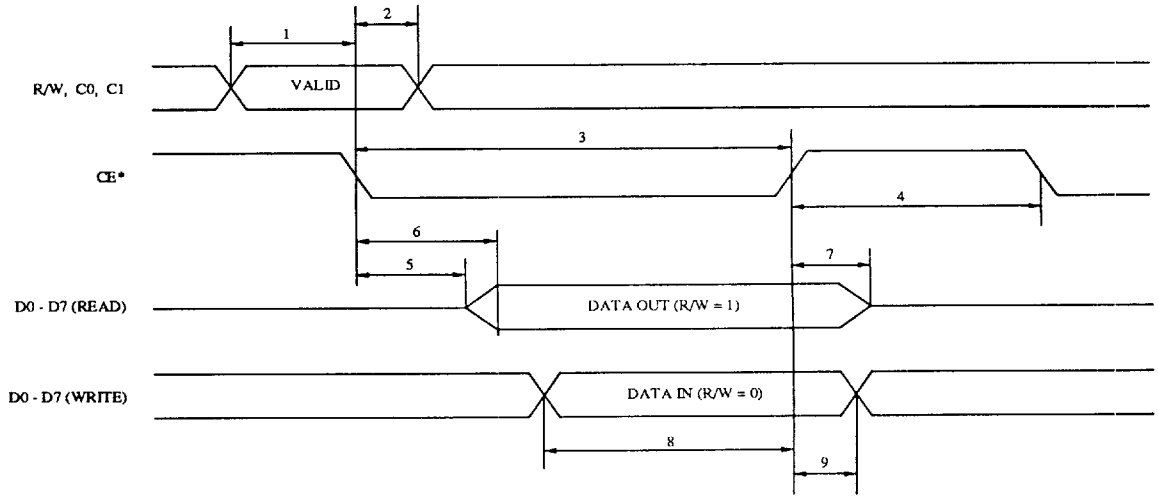
Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full-scale transition.

Note 2: Output settling time measured from 50% point of full-scale transition to output settling within ±1 LSB.

Note 3: Output rise/fall time measured between 10% and 90% points of full-scale transition.

Figure 6. Video Input/Output Timing.

Timing Waveforms (continued)



MPU Read/Write Timing.

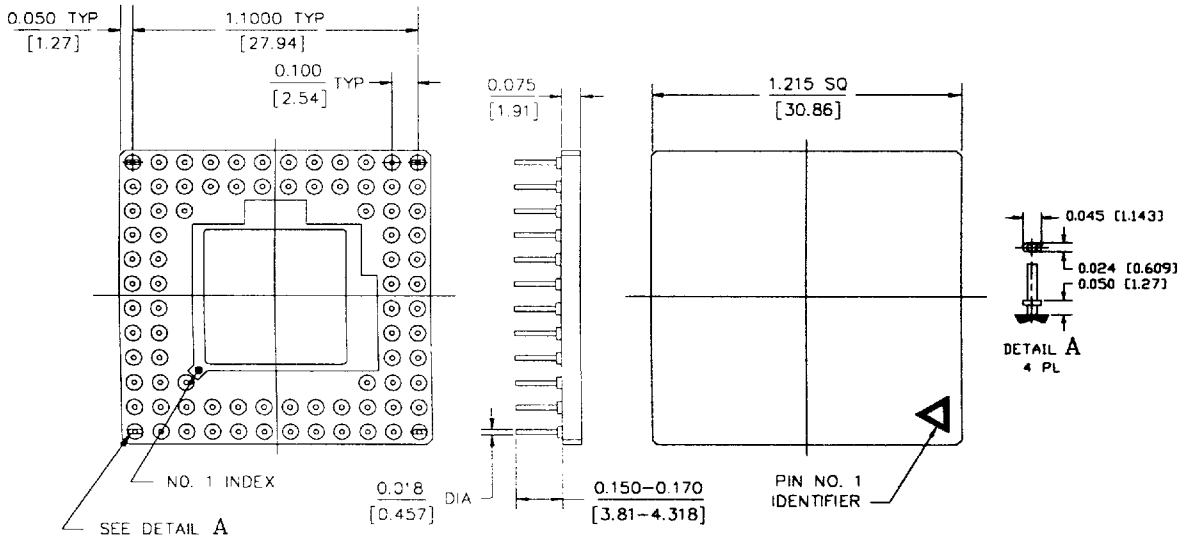
Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt9021KG	135 MHZ	84-pin Ceramic PGA	0° to +70° C
Bt9021KPJ	135 MHZ	84-pin Plastic J-Lead (PLCC)	0° to +70° C

Revision History

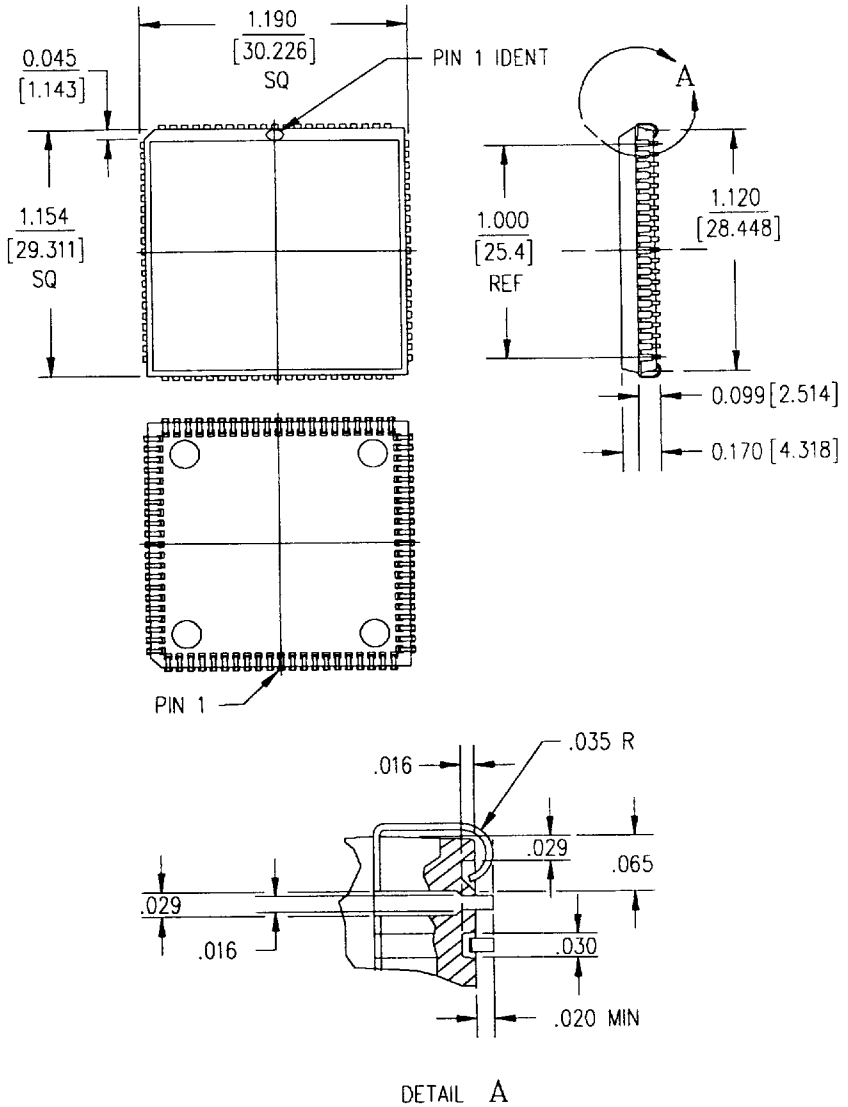
Datasheet Revision	*Change from Previous Revision*
B	Speed change from 125 to 135 MHz.

Package Drawing—84-pin Ceramic Pin Grid Array



NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

Package Drawing—84-pin Plastic J-Lead (PLCC)



NOTES—Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.