PHOTO DIODE SIGNAL PROCESSOR FOR COMPACT DISC PLAYERS

GENERAL DESCRIPTION

The TDA8808 is a bipolar integrated circuit designed for use in compact disc players with a single spot read-out system. It amplifies the photo-diode signals and processes the error signals for the focus- and radial control network.

Features

- Data amplifier with equalizer and AGC
- Offset-free pre-amplifier with AGC for the servo signals
- Trackloss and drop-out detection
- Start-up procedure for focus
- Normalizing focus error output signal to minimize radial error interference
- Laser supply amplifier and reference source
- Both TDA8808T and TDA8808AT versions suitable for car, portable and home applications
- Single and dual supply application
- Focus in-lock signal; ready signal output (RD)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
TDA8808T		V_{ext}	−5,5	−5,0	0	V
TDA8808AT		V_{ext}	V_P	10	12	V
Quiescent supply current	Si/$\overline{RD}$ = 0 V	I_Q	7,5	10	12,5	mA
HF input current (peak-to-peak value)	f_{HFin} = 100 kHz	$I_{HFin(p-p)}$	3	–	10	μA
LF input current (for each diode input)		I_D	0	–	6	μA
Laser supply output current	Si/$\overline{RD}$ = HIGH Z	I_{LO}	−8	−4	−2	mA
Operating ambient temperature range		T_{amb}	−30	–	+85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

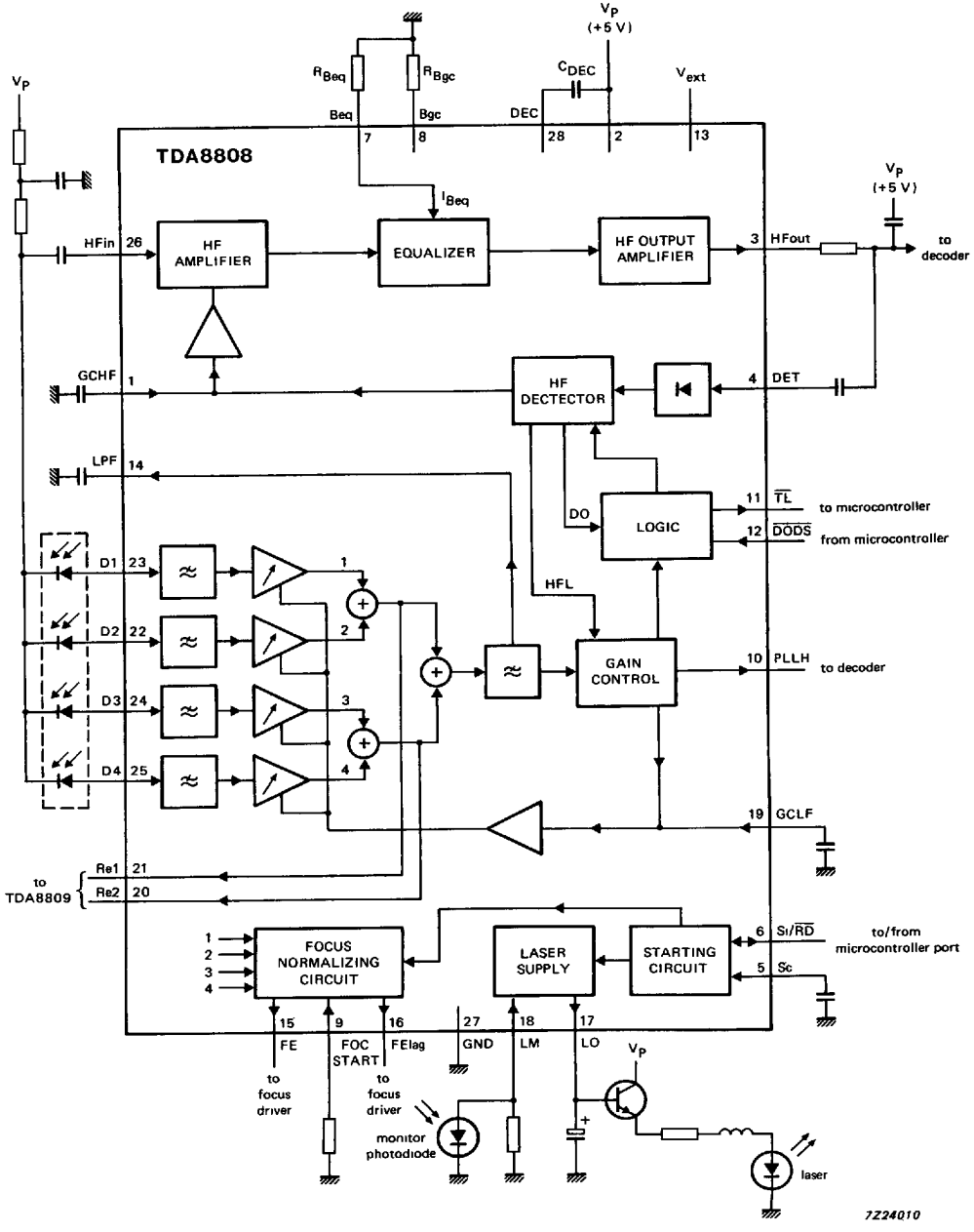


Fig. 1 Block diagram.

PINNING

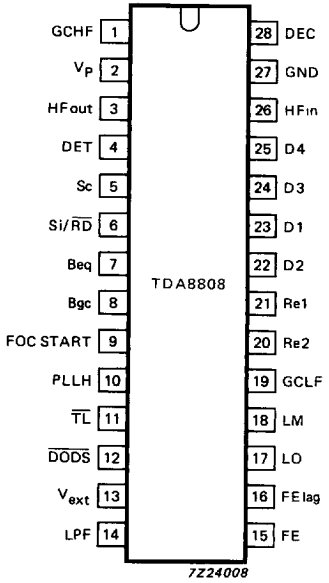


Fig. 2 Pinning diagram.

Pin functions

pin	mnemonic	description
1	GCHF	Gain control input of HF amplifier. Current output from HF amplitude detector
2	V_P	Positive supply voltage
3	HFout	HF amplifier and equalizer voltage output
4	DET	HF detector voltage input
5	Sc	Starting up capacitor input
6	Si/$\overline{RD}$	On/off control (start input); ready signal output (starting up procedure successful)
7	Beq	Equalizer reference current input
8	Bgc	DC and LF gain control reference current input
9	FOC START	Focus normalizing circuit starting current
10	PLLH	PLL on hold output
11	$\overline{TL}$	Track loss output
12	$\overline{DODS}$	Drop out detector suppression input
13	V_{ext}	TDA8808T Negative supply connection for FE and FElag output stage; also substrate connection TDA8808AT Positive supply connection for FE and FElag output stage
14	LPF	Low pass filter for I_{ret}, used in track loss ($\overline{TL}$) detector and LF gain control
15	FE	Current output of normalized, switched focus error signal
16	FElag	Current output of switched focus error signal, intended for lag network.
17	LO	Laser amplifier current output
18	LM	Laser monitor diode input
19	GCLF	Gain control input for AC and LF amplifiers. Current output from LF amplitude detector
20	Re2	Summation of amplified currents from D3 and D4
21	Re1	Summation of amplified currents from D1 and D2
23, 22	D1, D2	Current inputs to DC and LF photo diode amplifier
24, 25	D3, D4	Current inputs to DC and LF photo diode amplifier
26	HFin	Current input to HF amplifier
27	GND	Ground connection of device: also substrate connection for TDA8808AT
28	DEC	Decoupling input (internal bypass)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges (see Fig. 3)				
TDA8808T				
pin 2 to pin 13	$V_P - V_{(ext)}$	−0,3	13	V
pin 27 to pin 13	$V_{GND} - V_{(ext)}$	−0,3	13	V
TDA8808AT				
pin 13 to 27	$V_{ext} - V_{GND}$	−0,3	13	V
pin 2 to pin 27	$V_P - V_{GND}$	−0,3	13	V
Output voltage ranges				
except FE and FE_{lag}	V_O	0	V_P	V
FE and FE_{lag} (TDA8808T)	V_O	V_{ext}	V_P	V
FE and FE_{lag} (TDA8808AT)	V_O	V_{GND}	V_{ext}	V
LM (open loop)	V_O	V_{GND}	V_P	V
Total power dissipation	P_{tot}	see Fig. 4		
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Operating junction temperature	T_j	–	150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ = 140 K/W

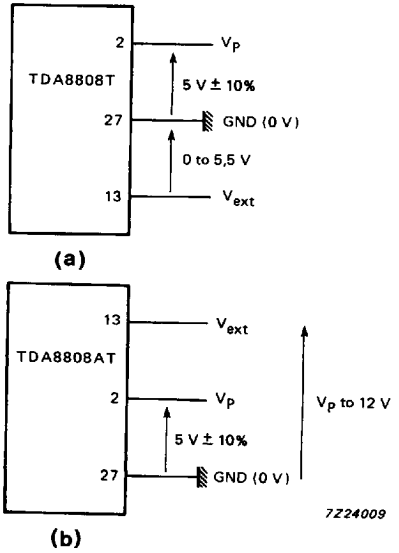


Fig. 3 Supply voltages; (a) TDA8808T, (b) TDA8808AT.

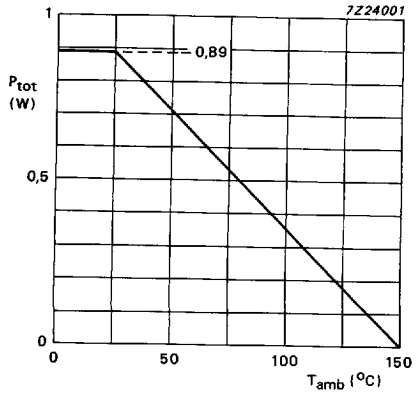


Fig. 4 Power derating curve.

CHARACTERISTICS

V_P = + 5 V; V_{GND} = 0 V; V_{ext} = −5 V (TDA8808T); V_{ext} = + 10 V (TDA8808AT); $V_{RE1} = V_{RE2}$ = 3,5 V; $V_{FE} = V_{FElag}$ = 0 V (TDA8808T); $V_{FE} = V_{FElag}$ = 5 V (TDA8808AT); $R_{FOC\ START}$ = 3,3 kΩ; $I_{Beq} = I_{Bgc}$ = 50 μA (current sources); T_{amb} = 25 °C; all voltages measured with respect to V_{GND}, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	4,5	5,0	5,5	V
External voltage range						
TDA8808T		V_{ext}	−5,5	−5,0	0	V
TDA8808AT		V_{ext}	V_P	10	12	V
Quiescent supply current	$V_{Si/\overline{RD}}$ = 0 V	I_Q	7,5	10	12,5	mA
Reference input (Beq)						
Input voltage level		V_{Beq}	500	560	620	mV
Input current		I_{Beq}	–	−50	–	μA
Reference input (Bgc)						
Input voltage level		V_{Bgc}	1,15	1,25	1,35	V
Input current		I_{Bgc}	–	−50	–	μA
Decoupling input (DEC)						
Input voltage level		V_{DEC}	–	V_P−1,4	–	V
Input impedance		$\lvert Z_{DEC}\rvert$	–	2	–	kΩ
HF input (HFin)						
Input voltage level		V_{HFin}	–	1,4	–	V
HF input current (peak-to-peak value)	f_{HFin} = 100 kHz	$I_{HFin(p-p)}$	3	–	10	μA
Input impedance		$\lvert Z_{HFin}\rvert$	0,5	1	2	kΩ
HF part						
DC characteristics						
Gain (G1) = $\frac{\Delta V_{HFout}}{\Delta I_{HFin}}$	I_{HFin} = ± 1 μA					
Maximum gain	V_{GCHF} = 4 V	G1(max)	390	480	570	mV/μA
Minimum gain	V_{GCHF} = 1,5 V	G1(min)	−5	0	5	mV/μA

parameter	conditions	symbol	min.	typ.	max.	unit
HF part (continued)						
AC characteristics						
Gain (G2) = 20 log $\frac{V_{O1}}{V_{O2}}$	note 1	G2	2	3,5	5	dB
Gain (G3) = 20 log $\frac{V_{O1}}{V_{O2}}$	note 2	G3	4	5,5	7	dB
Phase of input/output signal at 1 MHz	note 3	ϕ	–	$\pi/2$	–	rad.
Group delay at f_{HFin} = 300 kHz + Δf	note 3	$\tau 300$	–	290	–	ns
Flatness between 0,1 and 1 MHz	note 3	$\Delta\tau$	*	9	*	ns
HF output (HFout)						
Output voltage at I_{HFin} = 0	V_{GCHF} = 4 V	V_{HFout}	1,5	2,4	3,3	V
Output voltage (peak-to-peak value)						
at $I_{HFin(p-p)}$ = 7 μA	note 4	$V_{O1(p-p)}$	1	1,20	–	V
at $I_{HFin(p-p)}$ = 4 to 10 μA	note 5	$V_{O(p-p)}$	−20%	M_1	+20%	V
Output impedance		$\lvert Z_{HFout}\rvert$	–	60	–	Ω
HF detector input (DET)	see Fig. 5					
DC voltage level	I_{DET} = 0	V_{DET0}	–	2,2	–	V
Positive reference voltage V_{DET} to V_{DET0}		V_{refp}	−10%	540	+10%	mV
Negative reference voltage V_{DET} to V_{DET0}		V_{refn}	−5%	$-V_{refp}$	+5%	mV
Input impedance		$\lvert Z_{DET}\rvert$	–	9	–	kΩ

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Gain control (GCHF)						
Input voltage for:						
minimum HF gain		V_{GCHF}	–	1,8	–	V
maximum HF gain		V_{GCHF}	–	3,4	–	V
Input impedance at V_{GCHF} = 1,5 to 4 V		$\lvert Z_{GCHF}\rvert$	–	25	–	MΩ
Output current (see Fig. 5)						
$\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS}$ = LOW	I_{GCHF}	90	100	110	μA
$\Delta V_{DET} < V_{refn}$ or $\Delta V_{DET} > V_{refp}$	$\overline{DODS}$ = HIGH	I_{GCHF}	86	96	106	μA
$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS}$ = LOW	I_{GCHF}	−0,65	−0,35	−0,2	μA
$V_{refn} < \Delta V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{refp}$	$\overline{DODS}$ = HIGH	I_{GCHF}	−5,0	−4,4	−3,8	μA
$V_{DETn1} < \Delta V_{DET} < V_{DETp1}$	$\overline{DODS}$ = X*	I_{GCHF}	−0,65	−0,35	−0,2	μA
V_{DETp1}/V_{refp}; V_{DETn1}/V_{refn}			10	12,5	15	%
PLLH output (pin 10)						
Output voltage LOW						
I_{PLLH} = 400 μA (sink current)		V_{PLLHL}	–	–	0,4	V
Output voltage HIGH						
I_{PLLH} = −50 μA (source current)		V_{PLLHH}	2,4	–	–	V
Output sink current		I_{PLLH}	0,5	1,5	–	mA
Output source current		I_{PLLH}	–	−100	−50	μA
Threshold total LF current	V_{GCLF} = 3,5 V	I_{DT1}	–	2,0	–	μA
V_{DETp2}/V_{refp}; V_{DETn2}/V_{refn}			57,5	62,5	67,5	%
LF photo diode inputs (pins 22 to 25)						
(values given for each input)						
DC voltage level		V_D	–	1,2	–	V
Input current range		I_D	0	–	6	μA
Input impedance at 1 MHz	I_D = 1 μA	$\lvert Z_D\rvert$	–	10	–	kΩ

* X = don't care.

parameter	conditions	symbol	min.	typ.	max.	unit
LF gain						
Maximum DC gain						
for: $A_1 = \left\lvert \frac{I_{Re1}}{I_{D1} + I_{D2}} \right\rvert$;						
$I_{D3} = I_{D4} = 0$	$V_{GCLF} = 3{,}5$ V					
at $I_{D1} = 0\ \mu A$; $I_{D2} = 1\ \mu A$		A_{11}	$S_1 - 10\%$	S_1	S_1	
at $I_{D1} = 1\ \mu A$; $I_{D2} = 0\ \mu A$		A_{12}	S_1 or 55	S_1	S_1	
for: $A_2 = \left\lvert \frac{I_{Re2}}{I_{D3} + I_{D4}} \right\rvert$;						
$I_{D1} = I_{D2} = 0$	$V_{GCLF} = 3{,}5$ V					
at $I_{D3} = 0\ \mu A$; $I_{D4} = 1\ \mu A$		A_{21}	$S_1 - 10\%$	S_1	S_1	
at $I_{D3} = 1\ \mu A$; $I_{D4} = 0\ \mu A$		A_{22}	S_1 or 55	S_1	S_1	
S_1 mean value of A_{11}, A_{12}, A_{21}, A_{22}			55	64	84	
Minimum DC gain						
for: $A_3 = \left\lvert \frac{I_{Re1}}{I_{D1} + I_{D2}} \right\rvert$;						
$I_{D3} = I_{D4} = 0$	$V_{GCLF} = 0{,}8$ V					
at $I_{D1} = 0\ \mu A$; $I_{D2} = 1\ \mu A$		A_{31}	$S_2 - 1$	S_2	$S_2 + 1$	
at $I_{D1} = 1\ \mu A$; $I_{D2} = 0\ \mu A$		A_{32}	$S_2 - 1$	S_2	$S_2 + 1$	
for: $A_4 = \left\lvert \frac{I_{Re2}}{I_{D3} + I_{D4}} \right\rvert$;						
$I_{D1} = I_{D2} = 0$	$V_{GCLF} = 0{,}8$ V					
at $I_{D3} = 0\ \mu A$; $I_{D4} = 1\ \mu A$		A_{41}	$S_2 - 1$	S_2	$S_2 + 1$	
at $I_{D3} = 1\ \mu A$; $I_{D4} = 0\ \mu A$		A_{42}	$S_2 - 1$	S_2	$S_2 + 1$	
S_2 mean value of A_{31}, A_{32}, A_{41}, A_{42}			−0,1	0,7	3	

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
LF gain (continued)						
AC gain for:						
$G_4 = 20 \log P_1$; $I_{D3} = I_{D4} = 0$						
at $I_{D1} = 0$; $I_{D2(p-p)} = 1\ \mu A + 2\ \mu ADC$	note 6	G_4	−4,5	−3	−1,5	dB
at $I_{D1(p-p)} = 1\ \mu A + 2\ \mu ADC$; $I_{D2} = 0$	note 6	G_4	−4,5	−3	−1,5	dB
$G_5 = 20 \log P_2$; $I_{D1} = I_{D2} = 0$						
at $I_{D3} = 0$; $I_{D4(p-p)} = 1\ \mu A + 2\ \mu ADC$	note 7	G_5	−4,5	−3	−1,5	dB
at $I_{D3(p-p)} = 1\ \mu A + 2\ \mu ADC$; $I_{D4} = 0$	note 7	G_5	−4,5	−3	−1,5	dB
Gain control (GCLF)						
Input voltage for:						
minimum LF gain		V_{GCLF}	–	1	–	V
maximum LF gain		V_{GCLF}	–	2,8	–	V
Input impedance		$\lvert Z_{GCLF} \rvert$	–	25	–	MΩ
Threshold total LF current	I_{DT3}		–	1,6	–	mA
Output current (see Fig. 7)						
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	$I_{DT} < I_{DT3}$	I_{GCLF}	–	−0,6 I_{Bgc}	± 10	μA
	$I_{DT} > I_{DT3}$; note 8	I_{GCLF}	S_6−10	S_6	S_6+10	μA
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$		I_{GCLF}	–	−0,2 I_{Bgc}	± 2	μA
Re1, Re2 outputs (pin 21, pin 20)						
Output current	V_{GCLF} = 3,5 V					
at $I_{D1} = I_{D2} = 1\ \mu A$; $I_{D3} = I_{D4} = 0$		I_{Re1}	110	128	168	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$		I_{Re1}	–	0	–	μA
at $I_{D1} = I_{D2} = 0$; $I_{D3} = I_{D4} = 1\ \mu A$		I_{Re2}	110	128	168	μA
at $I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$		I_{Re2}	–	0	–	μA
Output voltage						
pin 21		V_{Re1}	1	–	V_P	V
pin 20		V_{Re2}	1	–	V_P	V
Output impedance						
pin 21		$\lvert Z_{Re1} \rvert$	–	1	–	MΩ
pin 20		$\lvert Z_{Re2} \rvert$	–	1	–	MΩ

parameter	conditions	symbol	min.	typ.	max.	unit
Reference current (I_{ret})						
$I_{ret} = I_{Re1} = I_{Re2}$	note	I_{ret}	200	220	240	μA
LPF output (pin 14)						
DC voltage level	note 9	V_{LPF}	$V_P-2,1$	$V_P-1,7$	$V_P-1,4$	V
Input impedance		$\lvert Z_{LPF}\rvert$	–	3	–	kΩ
FOC START input (pin 9)						
Start current (ST) for FE ($-I_{FOC\ START} = I_{ST}$)	Si/$\overline{RD}$ = HIGH Z	I_{ST}	75	150	500	μA
	Si/$\overline{RD}$ = LOW	I_{ST}	–	0	–	μA
Start voltage (ST) for FE ($V_{FOC\ START} = V_{ST}$)	Si/$\overline{RD}$ = HIGH Z	V_{ST}	430	530	630	mV
	Si/$\overline{RD}$ = LOW	V_{ST}	−20	0	20	mV
FElag output (pin 16)	see Fig. 8					
Output voltage						
TDA8808T		V_{FElag}	$V_{ext}+1,5$	–	$V_P-1,5$	V
TDA8808AT		V_{FElag}	+1,5	–	$V_{ext}-1,5$	V
Output impedance		$\lvert Z_{FElag}\rvert$	–	8	–	MΩ
Output current	Si/$\overline{RD}$ = HIGH Z; V_{GCLF} = 3,5 V					
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	$I_{FElag} = I_O$	−10	0	+10	μA
$I_{D2} = I_{D3} = 1\ \mu A$; $I_{D1} = I_{D4} = 2\ \mu A$	$V_{Sc} = V_P$	I_{FElag}	−10%	$-2S_1 + I_O$	+10%	μA
$I_{D2} = I_{D3} = 2\ \mu A$; $I_{D1} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	I_{FElag}	−10%	$-2S_1 + I_O$	+10%	μA
$I_{D2} = I_{D3} = 2\ \mu A$; $I_{D1} = I_{D4} = 1\ \mu A$	V_{Sc} = 1,5 V	I_{FElag}	−5	0	+5	μA
$I_{D2} = I_{D3} = 1\ \mu A$; $I_{D1} = I_{D4} = 2\ \mu A$	V_{Sc} = 1,5 V	I_{FElag}	−5	0	+5	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
FE output (pin 15)	see Fig. 8					
Output voltage						
TDA8808T		V_{FE}	$V_{ext}+1,5$	–	$V_P-1,5$	V
TDA8808AT		V_{FE}	+1,5	–	$V_{ext}-1,5$	V
Output impedance		$\lvert Z_{FE}\rvert$	–	8	–	MΩ
Output current	note 10					
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 0$	I_{FE}	−10%	$-2S_1-134-I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 0$	I_{FE}	−10%	$-4S_1-67-I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 1,25$ V	I_{FE}	−10%	$-2S_1-134+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 1,25$ V	I_{FE}	−10%	$-4S_1-67+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = 1,75$ V	I_{FE}	−20%	$-2S_1+67+I_{ST}$	+10%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = 1,75$ V	I_{FE}	−10%	$-4S_1-67+I_{ST}$	+20%	μA
$I_{D1} = I_{D4} = 2\ \mu A$; $I_{D2} = I_{D3} = 1\ \mu A$	$V_{Sc} = V_P$	$I_{FE} = S_6$	−20%	67	+20%	μA
$I_{D1} = I_{D4} = 1\ \mu A$; $I_{D2} = I_{D3} = 2\ \mu A$	$V_{Sc} = V_P$	I_{FE}	−15%	$-S_6$	+15%	μA
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 1\ \mu A$	$V_{Sc} = V_P$	I_{FE}	−10	0	+10	μA
$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0$	$V_{Sc} = V_P$	I_{FE}	−5	0	+5	μA

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{\text{DODS}}$ logic input (pin 12)						
Switching levels						
input voltage LOW		$V_{\overline{DODS}}$	–	–	+0,8	V
input voltage HIGH		$V_{\overline{DODS}}$	+2	–	–	V
Input source current		$I_{\overline{DODS}}$	−35	−25	−15	μA
Starting input (Sc)	see Fig. 9					
Output voltage	Si/$\overline{RD}$ = LOW	V_{Sc}	–	0	–	V
Output voltage	S1/$\overline{RD}$ = HIGH Z	V_{Sc}	–	–	V_P−0,5	V
Output impedance		$\lvert Z_{Sc} \rvert$	–	*	–	MΩ
Output source current	Si/$\overline{RD}$ = HIGH Z; V_{Sc} = 1,5 V	I_{Sc}	−1,2	−1	−0,8	μA
Output sink current	Si/$\overline{RD}$ = LOW	I_{Sc}	0,5	1,2	2,0	mA
Si/$\overline{RD}$ logic input/output (pin 20)	see Fig. 9					
Voltage "forced LOW"	$I_{Si/\overline{RD}}$ = 400 μA; V_{Sc} = 2,5 V; V_{GCLF} < 2,8 V	$V_{Si/\overline{RD}}$	–	0,15	0,4	V
Switching levels						
input voltage LOW		$V_{Si/\overline{RD}}$	–	–	+0,8	V
input voltage HIGH Z	$I_{Si/\overline{RD}}$ = −5 μA	$V_{Si/\overline{RD}}$	2,4	2,8	–	V
Input source current LOW		$I_{Si/\overline{RD}}$	−35	−25	−15	μA
$\overline{\text{TL}}$ logic output (pin 11)	see Fig. 6					
Output voltage level LOW	$I_{\overline{TL}}$ = 400 μA; (sink current)	$V_{\overline{TL}}$	–	0,15	0,4	V
Output voltage level HIGH	$I_{\overline{TL}}$ = −50 μA; (source current)	$V_{\overline{TL}}$	2,4	–	–	V
Threshold total LF current	I_{DT2}		–	3,9	–	μA
Output voltage	DODS = HIGH (≥ 2,4 V)					
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn1} < \Delta V_{DET} < V_{DETp1}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < V_{DET} < V_{DETn1}$ or $V_{DETp1} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} < I_{DT2}$	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < V_{DET} < V_{DETn1}$ or $V_{DETp1} < V_{DET} < V_{DETp2}$	$I_{DT} > I_{DT2}$	$V_{\overline{TL}}$	–	0,15	0,4	V

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
$\overline{TL}$ logic output (continued)						
Output voltage	$\overline{DODS}$ = LOW (≤ 0,8 V)					
$\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$	I_{DT} don't care	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} < I_{DT2}$	$V_{\overline{TL}}$	2,4	–	–	V
$V_{DETn2} < \Delta V_{DET} < V_{DETp2}$	$I_{DT} > I_{DT2}$	$V_{\overline{TL}}$	–	0,15	0,4	V
Output sink current	$V_{\overline{TL}}$ = LOW	$I_{\overline{TL}}$	1	2,2	–	mA
Output source current	$V_{\overline{TL}}$ = HIGH	$I_{\overline{TL}}$	–	−100	−50	μA
Delay times (see Fig. 10)	see Fig. 6	$\tau 1$	7	8,5	10	μs
		$\tau 2$	$\tau 1$−15% or 6,5	–	$\tau 1$+ 5% or 10	μs
		$\tau 3$	7	8,5	10	μs
		$\tau 4$	$\tau 3$−10% or 7	–	$\tau 3$+10% or 10	μs
LO output (pin 17)						
Output voltage		V_{LO}	–	–	V_P − 0,5	V
Output impedance		$\lvert Z_{LO} \rvert$	–	95	–	kΩ
Output leakage current	Si/$\overline{RD}$ = LOW	I_{LO}	−10	−0,1	0	μA
Maximum output current	Si/$\overline{RD}$ = HIGH Z	I_{LO}	−8	−4	−2	mA
LM input (pin 18)						
Input voltage	closed loop	V_{LM}	185	205	225	mV
Input bias current		I_{LM}	−2	–	–	μA
Laser supply						
Transconductance						
For DC (note 11)	Si/$\overline{RD}$ = HIGH Z	G_{LDC}	–	0,5	–	A/V
	Si/$\overline{RD}$ = LOW	G_{LDC}	–	0	–	A/V
For AC (note 12) delay time		τLO	–	*	–	ns

* Value to be fixed.

Notes to the characteristics

1. Voltage output signal V_{O1} measured at f_{HFin} = 700 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
   Voltage output signal V_{O2} measured at f_{HFin} = 100 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
2. Voltage output signal V_{O1} measured at f_{HFin} = 1 MHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
   Voltage output signal V_{O2} measured at f_{HFin} = 100 kHz; $I_{HFin(p-p)}$ = 7 μA; V_{GCHF} = 2,4 V.
3. Phase of input/output signal, group delay and flatness measured at $I_{HFin(p-p)}$ = 1 μA; V_{GCHF} = 4 V.

   Group delay: $\tau = \frac{d\phi}{dw}$; $\Delta f \approx 50$ kHz.

   Flatness: $\Delta\tau = \tau_{max} - \tau_{min}$.
4. HF part output vpltage for closed loop conditions; f_{HFin} = 500 kHz.
5. HF part output voltage for closed loop conditions; f_{HFin} = 0,1 to 1 MHz.
   M_1 is the measured value of V_{O1}.
6. P_1 is the measured value of $\frac{I_{Re1}(1)}{I_{D1}(1) + I_{D2}(1)} \cdot \frac{I_{D1}(2) + I_{D2}(2)}{I_{Re1}(2)}$

   Where:

   (1) are the current levels at f_i = 25 kHz.
   (2) are the current levels at f_i = 1 kHz.

   Measurement taken at V_{GCLF} = 3,5 V.
7. P_2 is the measured value of $\frac{I_{Re2}(1)}{I_{D3}(1) + I_{D4}(1)} \cdot \frac{I_{D3}(2) + I_{D4}(2)}{I_{Re2}(2)}$

   Where:

   (1) are the current levels at f_i = 25 kHz.
   (2) are the current levels at f_i = 1 kHz.

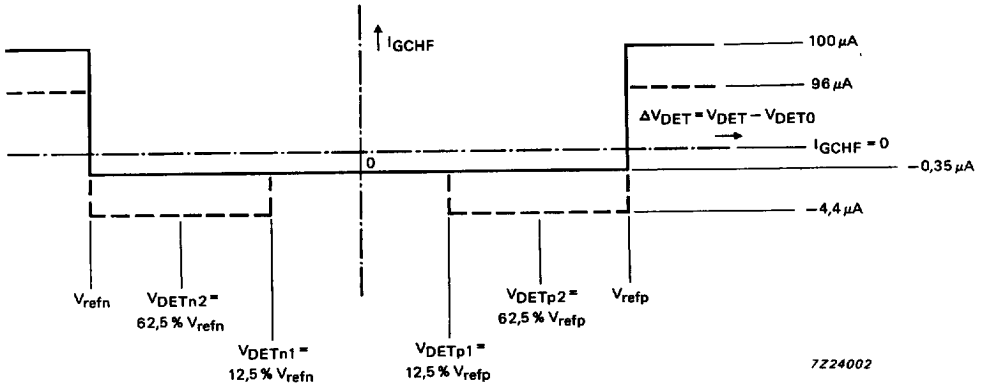
   Measurement taken at V_{GCLF} = 3,5 V.
8. S_6 is the measured value of $S_1 \cdot \frac{I_{DT}}{4} - 1{,}1\ I_{Bgc}$

   Measurement taken at V_{GCLF} = 3,5 V.
9. LF part reference current I_{ret} and low-pass filter output voltage for closed loop conditions.
   Measurement taken at $I_{DT} > I_{DT3}$; $\Delta V_{DET} < V_{DETn2}$ or $\Delta V_{DET} > V_{DETp2}$.
10. FE output current measured at V_{GCLF} = 3,5 V and Si/$\overline{RD}$ = HIGH Z; $I_{ST} = \frac{V_{FOC\ START}}{R_{FOC\ START}}$.
11. Laser supply transconductance for DC

    $G_{LDC} = \frac{\Delta I_{LO}}{\Delta V_{LM}}$ $(0 < -I_{LO} < 2\ mA)$.
12. Laser supply transconductance for AC

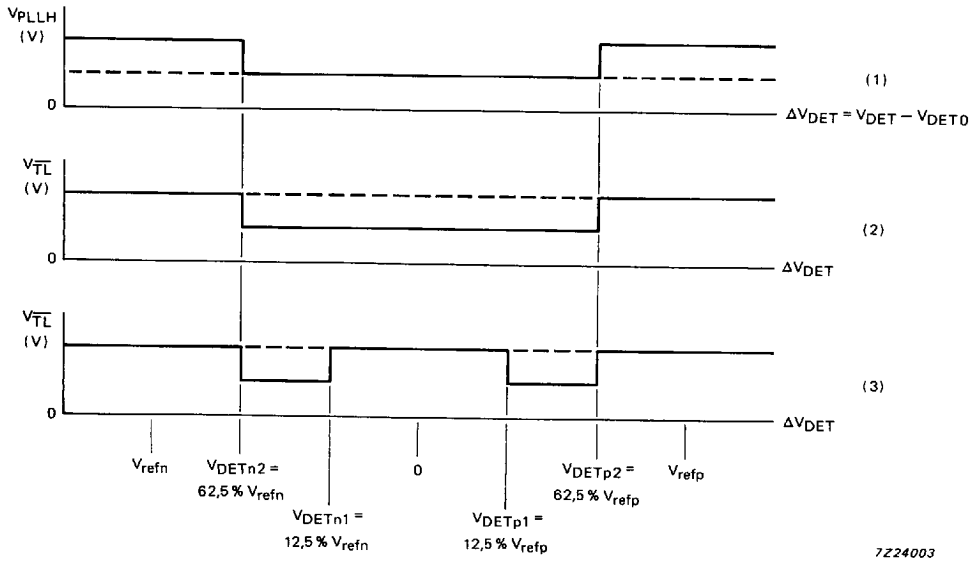
    $G_{LAC} = G_{LO} \cdot \frac{1}{1 + S \cdot \tau LO}$

    Where: S is the laplace operator in the frequency domain.



---------- $\overline{DODS}$ = HIGH
———— $\overline{DODS}$ = LOW

Fig. 5 HF gain control current (I_{GCHF}) as a function of input voltage ΔV_{DET}.



(1)

——— $I_{DT} > I_{DT1}$

---------- $I_{DT} < I_{DT1}$

$I_{DT} = I_{D1} + I_{D2} + I_{D3} + I_{D4}$

$I_{DT1} = 2{,}67\ I_{Bgc}/S_1$

$I_{DT2} = 5\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

(2)

——— $I_{DT} > I_{DT2}$

---------- $I_{DT} < I_{DT2}$

$\overline{DODS}$ = LOW

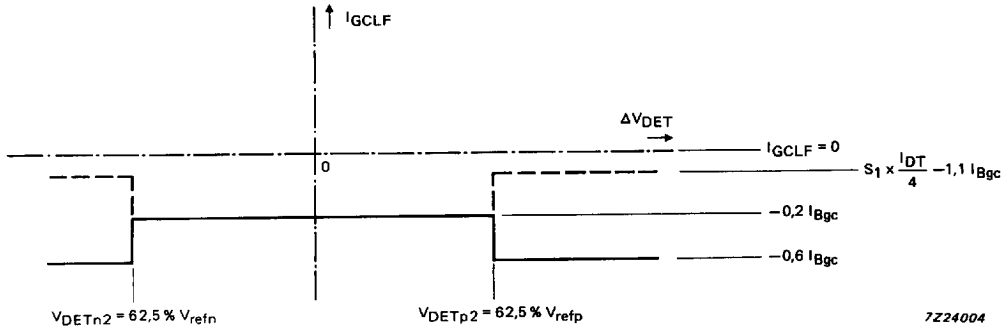
(3)

——— $I_{DT} > I_{DT2}$

---------- $I_{DT} < I_{DT2}$

$\overline{DODS}$ = HIGH

Fig. 6 $\overline{TL}$ voltage as a function of input voltage ΔV_{DET}.



---------- $I_{DT} > I_{DT3}$

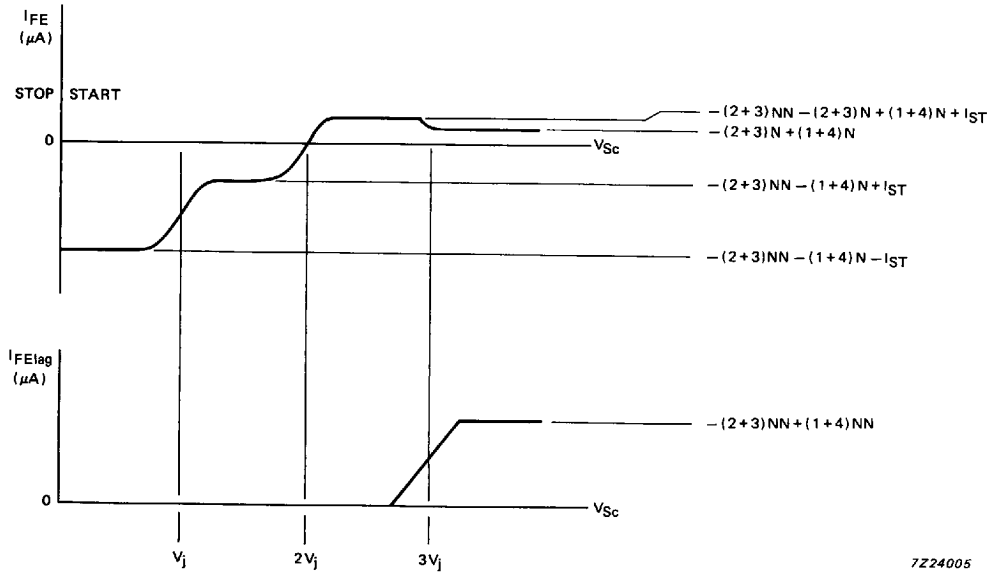
——— $I_{DT} < I_{DT3}$

$I_{DT} = I_{D1} + I_{D2} + I_{D3} + I_{D4}$

$I_{DT3} = 2\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

Fig. 7 LF gain control current (I_{GCLF}) as a function of input voltage ΔV_{DET}.



I_{ST} = $-I_{FOC\ START}$

I_{cont} = $2\ I_{Bgc}$ if $I_{DT} > I_{DT3}$

I_{cont} = $I_{DT} \times S_1$ if $I_{DT} < I_{DT3}$

I_{DT} = $I_{D1} + I_{D2} + I_{D3} + I_{D4}$

I_{DT3} = $2\ I_{Bgc}/S_1$

S_1 = average maximum LF gain

(1 + 4)NN = not normalized currents = $(I_{D1} + I_{D4})\ S_1$

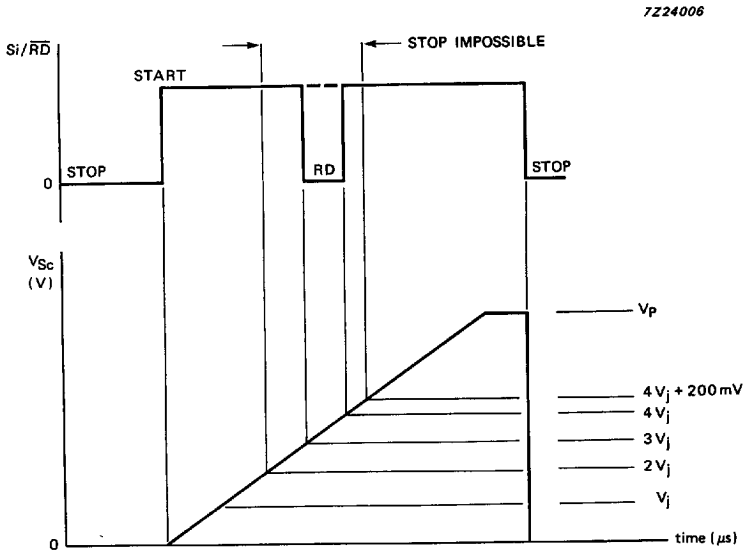
(2 + 3)NN = not normalized currents = $(I_{D2} + I_{D3})\ S_1$

(1 + 4)N = normalized currents = $\left(\frac{I_{D1}}{I_{D1} + I_{D2}} + \frac{I_{D4}}{I_{D3} + I_{D4}}\right) \times I_{cont}$

(2 + 3)N = normalized currents = $\left(\frac{I_{D2}}{I_{D1} + I_{D2}} + \frac{I_{D3}}{I_{D3} + I_{D4}}\right) \times I_{cont}$

V_j is the junction voltage (0,7 V typ.).

Fig. 8 FElag current output as a function of starting voltage input (V_{Sc}).



RD : Si/$\overline{RD}$ forced LOW for ready signal

——— $V_{GCLF} < 2{,}8$ V

--------- $V_{GCLF} > 3{,}5$ V

V_j is the junction voltage (0,7 V typ.)

Fig. 9 Si/$\overline{RD}$ signal as a function of V_{Sc}.

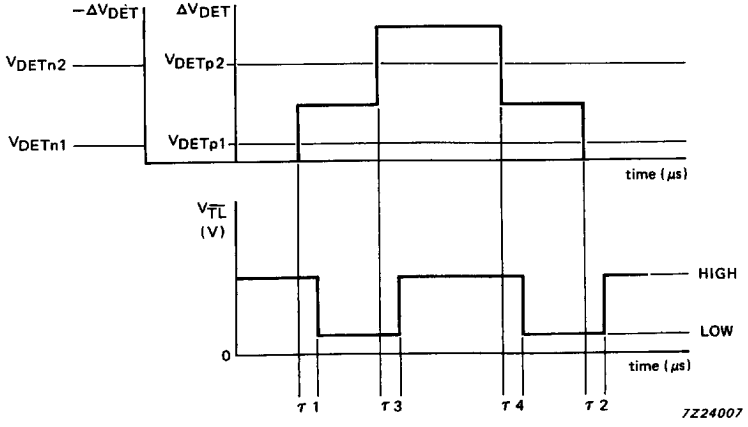


Fig. 10 Delay times between ΔV_{DET} and $V_{\overline{TL}}$.