Data sheet	
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TEA0655

Dual Dolby* B-type noise reduction circuit for playback applications

FEATURES

- Dual noise reduction channels
- Head preamplifiers
- Equalization with electronically switched time constants
- Dolby reference level = 387.5 mV

GENERAL DESCRIPTION

The TEA0655 is an integrated circuit that provides two Dolby B-type noise reduction channels for playback applications in car radios. The TEA0655 includes head and equalization amplifiers with electronically switched time constants. The device will operate with power supplies in the range 9 to 15 volts, the output overload level increasing with an increase in supply voltage. Current drain varies with supply voltage and noise reduction ON/OFF, therefore it is advisable to use a regulated power supply or a supply with a long time constant.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage range	8	–	15	V
I_{CC}	supply current	–	20	25	mA
(S+N)/N	signal plus noise-to-noise ratio	78	84	–	dB

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA0655	20	DIL	plastic	SOT146

* Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, USA, from whom licensing and application information must be obtained. Dolby is a registered trade-mark of Dolby Laboratories Licensing Corporation.

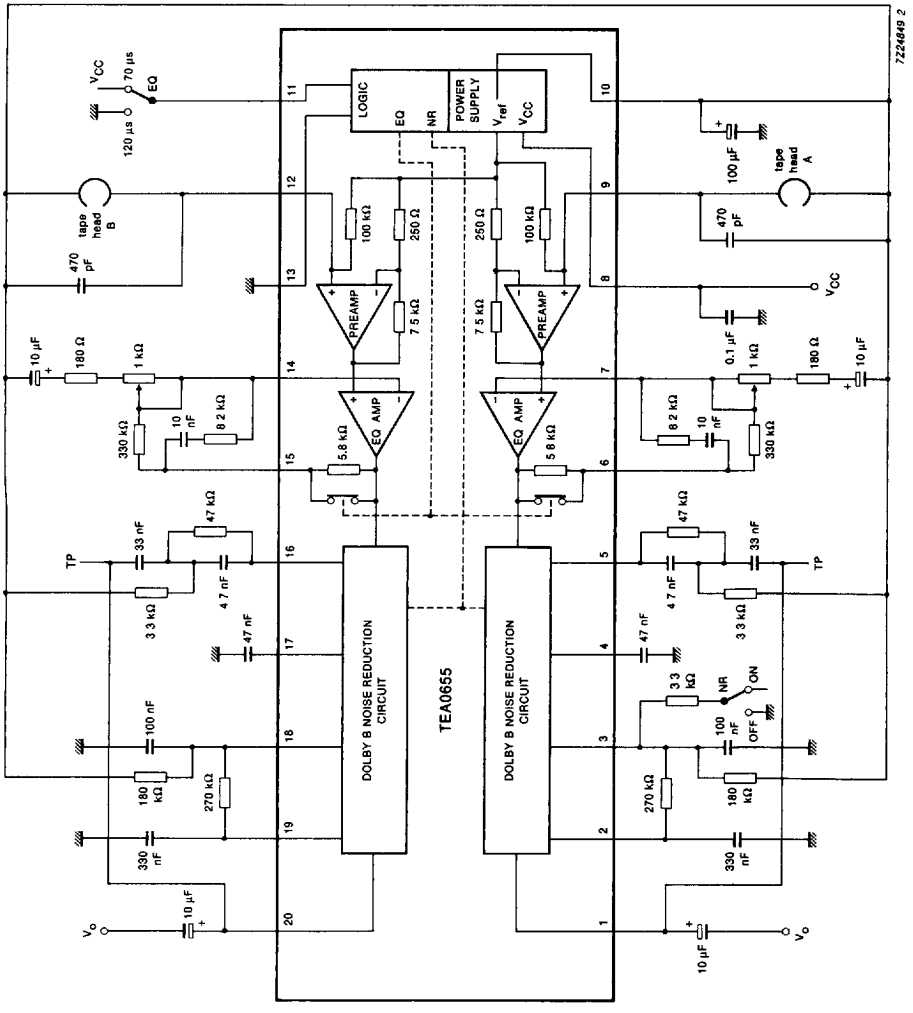

Fig.1 Block and application diagram.

Dual Dolby B-type noise reduction circuit for playback applications

TEA0655

FUNCTIONAL DESCRIPTION

Noise reduction is enabled when pin 3 is open-circuit and disabled when pin 3 is connected to GRD (pin 13) via a 3.3 kΩ resistor (see Fig.1).

Pin 3 performs the functions of a logic input for noise reduction switching for both channels. It also provides smoothing for the control signal in one channel. It is important that no voltage is applied to pin 3 when in the NR ON mode as this will cause irregular noise reduction characteristics in the selected channel. Time constant switching is achieved by applying a DC voltage to pin 11.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output channel A
INTA	2	integrating filter channel A
CONTRA	3	control voltage channel A
HPA	4	high-pass filter channel A
SCA	5	side chain channel A
EQA	6	equalizing output channel A
EQFA	7	equalizing input channel A
V_{CC}	8	voltage supply
INA	9	input channel A
V_{ref}	10	reference voltage
SWEQ	11	equalizing switch
INB	12	input channel B
GRD	13	ground
EQFB	14	equalizing input channel B
EQB	15	equalizing output channel B
SCB	16	side chain channel B
HPB	17	high-pass filter channel B
CONTRB	18	control voltage channel B
INTB	19	integrating filter channel B
OUTB	20	output channel B

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–	16	V
V_I	input voltage (pins 1 to 20)	−0.3	V_{CC}	V
T_{amb}	operating ambient temperature range	−40	+85	°C
T_{stg}	storage temperature range	−65	+150	°C
V_{es}	electrostatic handling *	–	–	–

* Classification A: human body model; C = 100 pF, R = 1.5 kΩ, V = ≥ 2 kV; charge device model; C = 200 pF, R = 0 Ω, V ≥ 500 V.

CHARACTERISTICS

V_{CC} = 10 V; f = 20 Hz to 20 kHz; T_{amb} = +25 °C; all levels referenced to 387.5 mV RMS (0 dB) at test point (TP) (pin 1 or 20); test circuit Fig.1; NR ON; EQ switch in the 70 µs position; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8	10	15	V
I_{CC}	supply current		–	20	25	mA
	channel matching	NR OFF	−0.5	–	+0.5	dB
THD	distortion 2nd and 3rd harmonic	f = 1 kHz; 0 dB	–	0.08	0.15	%
		f = 10 kHz; +10 dB	–	0.15	0.3	%
	signal handling	V_{CC} = 8 V; 1% distortion at 1 kHz	12	15	–	dB
(S+N)/N	signal-plus-noise to noise ratio (see Fig.2; decode mode)	internal gain 40 dB linear; CCIR/ARM weighted	78	84	–	dB
PSRR	power supply ripple rejection	f = 1 kHz; 250 mV; see Fig.3	52	57	–	dB
	frequency response measured in encode mode see Fig.2 referenced to test point	note 1				
		f = 1 kHz; 0 dB	−1.5	0	+1.5	dB
		f = 1 kHz; −25 dB	−17.8	−19.3	−20.8	dB
		f = 0.2 kHz; −25 dB	−22.9	−24.4	−25.9	dB
		f = 5 kHz; −25 dB	−18.1	−19.6	−21.1	dB
		f = 10 kHz; −35 dB	−24.4	−25.9	−27.4	dB
α_{CR}	channel separation	f = 1 kHz; see Fig.4	57	63	–	dB
R_{Lmin}	minimum load resistance on output (pins 1 and 20)	12 dB; 1 kHz; 1% THD	10	–	–	kΩ
G_V	voltage gain (pin 9 to 7 or pin 12 to 14)	1 kHz	29	30	31	dB
V_{off}	input offset voltage		–	2	–	mV
I_B	input bias current		–	0.1	0.4	µA
R_{EQ}	equalizing resistor		4.7	5.8	6.9	kΩ
R_I	input resistance pins 9 and 12		60	100	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
A_V	open loop gain pins 12/15 and pins 9/6	10 kHz	80	86	–	dB
		400 kHz	104	110	–	dB
	DC output voltage pins 1 and 20	NR OFF with reference to $V_{CC}/2$	–	–	±0.15	V
Z_O	output impedance		–	50	70	Ω
I_{OGRD}	DC output current capability	to ground	–	–	–2	mA
I_{OVCC}		to V_{CC}	–	–	300	μA
En	equivalent input noise voltage (RMS value)	NR OFF; unweighted; 20 Hz to 20 kHz; $R_S = 0\ \Omega$	–	0.7	1.4	μV
Switching thresholds						
V_{OFF}	NR switch OFF (pin 3)		0	–	$0.2V_{CC}$	V
I_3	NR switch ON		–	open	–100	nA
	equalizing (EQ) switch (pin 11) at 70 μs		$0.5V_{CC}$	–	V_{CC}	V
	equalizing switch at 120 μs		0	–	$0.2V_{CC}$	V
I_{11}	input current		–	–	–1	μA

Note to the characteristics

1. Equals the corresponding decode mode cut with reference to test point level, see Fig.1.

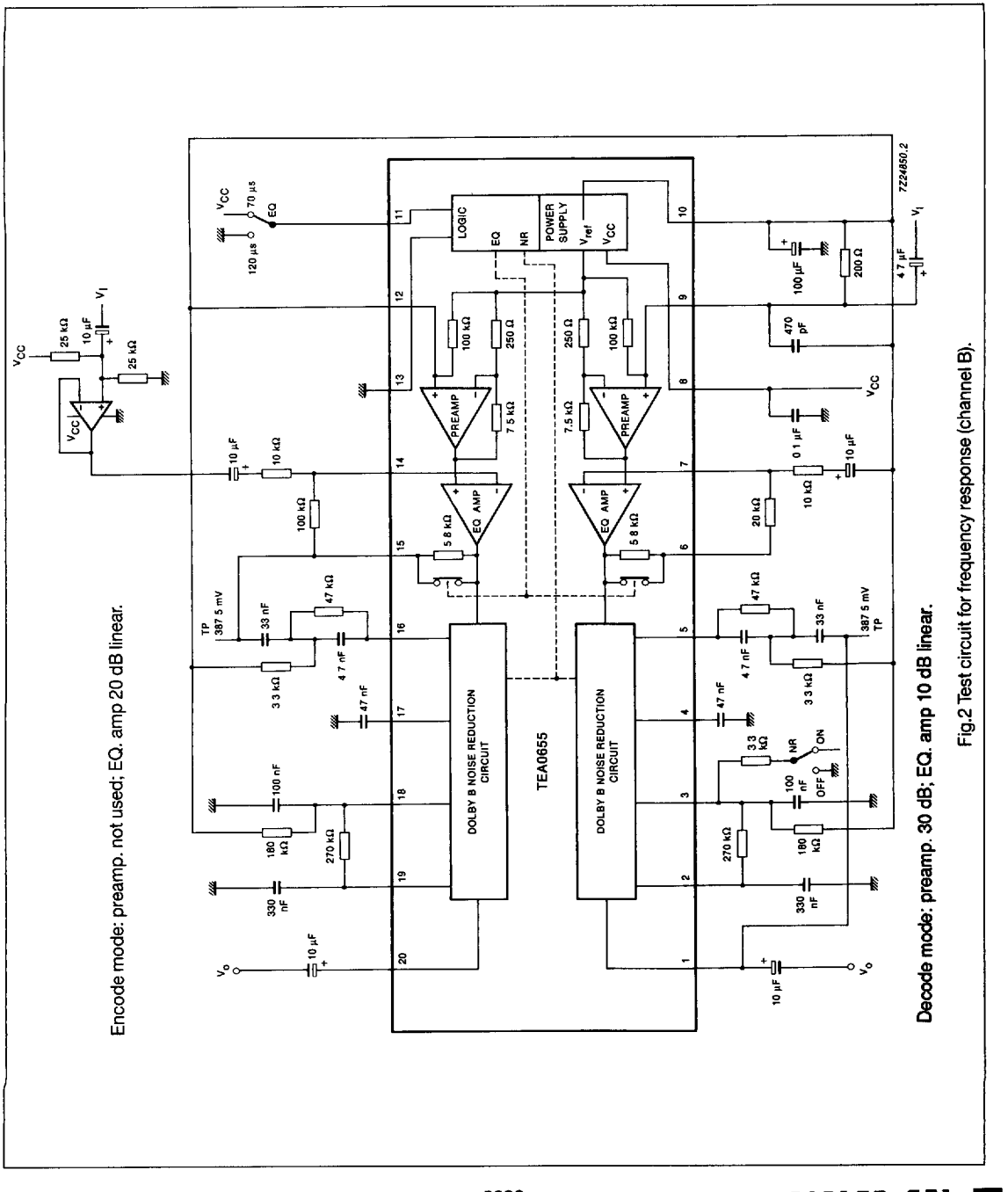

Fig.2 Test circuit for frequency response (channel B).

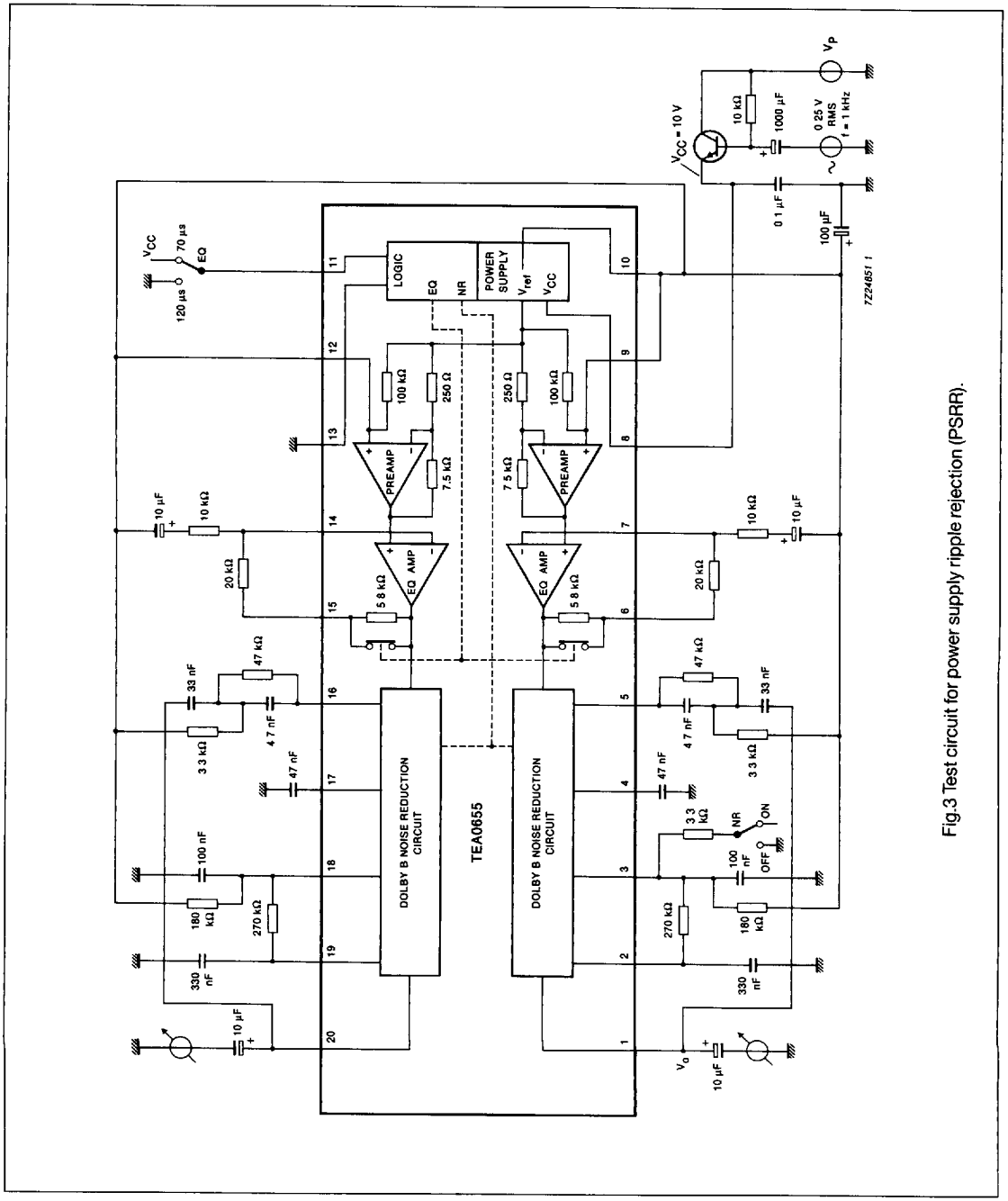

Fig.3 Test circuit for power supply ripple rejection (PSRR).

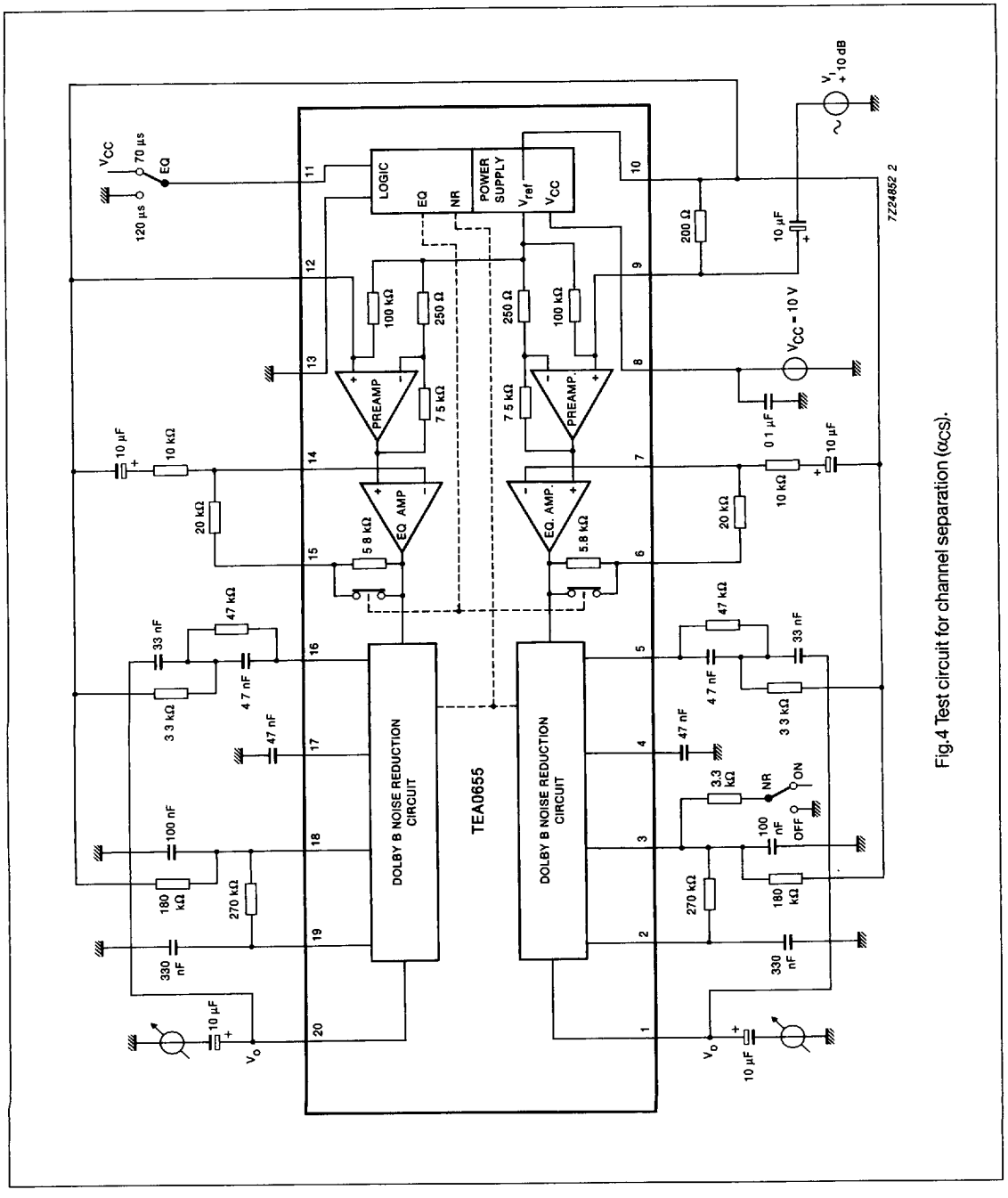

Fig.4 Test circuit for channel separation (α_{CS}).