Low voltage transmission circuit with dialler interface

TEA1062; TEA1062A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides a supply for external circuits
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
  - TEA1062: active HIGH (MUTE)
  - TEA1062A: active LOW ($\overline{MUTE}$)
- Receiving amplifier for dynamic, magnetic or piezo-electric earpieces
- Large gain setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers
- Gain control curve adaptable to exchange supply
- DC line voltage adjustment facility.

GENERAL DESCRIPTION

The TEA1062 and TEA1062A are integrated circuits that perform all speech and line interface functions required in fully electronic telephone sets. They perform electronic switching between dialling and speech. The ICs operate at line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel.

All statements and values refer to all versions unless otherwise specified.

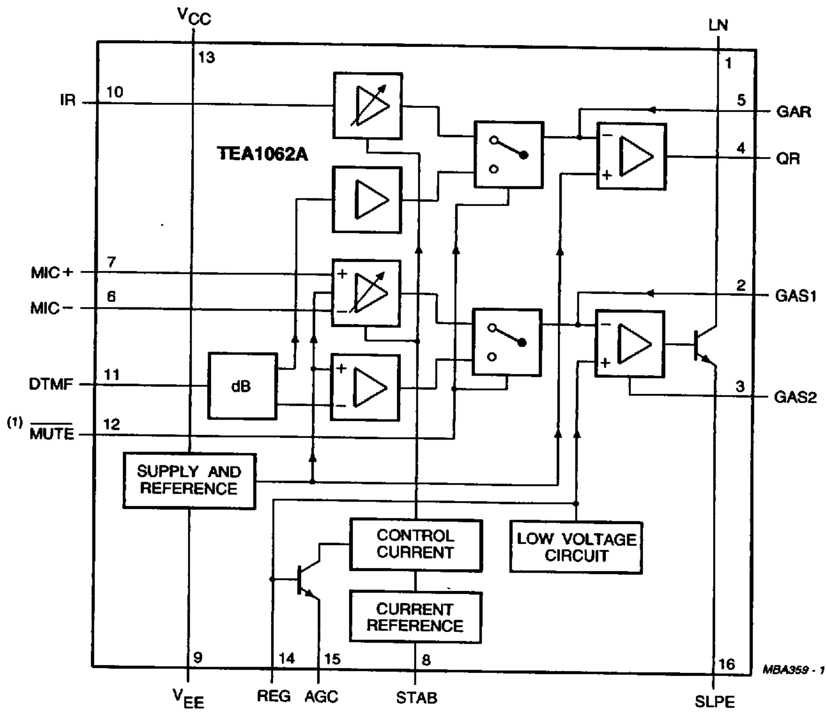
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	3.55	4.0	4.25	V
I_{line}	operating line current					
	normal operation		11	–	140	mA
	with reduced performance		1	–	11	mA
I_{CC}	internal supply current	V_{CC} = 2.8 V	–	0.9	1.35	mA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA				
	TEA1062	I_p = 1.2 mA; MUTE = HIGH	2.2	2.7	–	V
		I_p = 0 mA; MUTE = HIGH	–	3.4	–	V
	TEA1062A	I_p = 1.2 mA; $\overline{MUTE}$ = LOW	2.2	2.7	–	V
		I_p = 0 mA; $\overline{MUTE}$ = LOW	–	3.4	–	V
G_v	voltage gain					
	microphone amplifier		44	–	52	dB
	receiving amplifier		20	–	31	dB
T_{amb}	operating ambient temperature		−25	–	+75	°C
Line loss compensation						
ΔG_v	gain control		–	5.8	–	dB
V_{exch}	exchange supply voltage		36	–	60	V
R_{exch}	exchange feeding bridge resistance		0.4	–	1	kΩ

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1062	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
TEA1062C3M1	IDF16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
TEA1062C4M1	IDF16	plastic dual in-line package; 16 leads (300 mil)	SOT38-8
TEA1062A	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
TEA1062T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TEA1062AT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM



(1) Pin 12 is active HIGH (MUTE) for TEA1062.

Fig.1 Block diagram for TEA1062A.

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; transmitting amplifier
GAS2	3	gain adjustment; transmitting amplifier
QR	4	non-inverting output; receiving amplifier
GAR	5	gain adjustment; receiving amplifier
MIC−	6	inverting microphone input
MIC+	7	non-inverting microphone input
STAB	8	current stabilizer
V_{EE}	9	negative line terminal
IR	10	receiving amplifier input
DTMF	11	dual-tone multi-frequency input
$\overline{MUTE}$	12	mute input (see note 1)
V_{CC}	13	positive supply decoupling
REG	14	voltage regulator decoupling
AGC	15	automatic gain control input
SLPE	16	slope (DC resistance) adjustment

Note

1. Pin 12 is active HIGH (MUTE) for TEA1062.

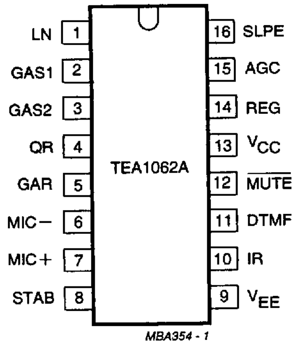


Fig.2 Pin configuration for TEA1062A.

FUNCTIONAL DESCRIPTION

Supplies V_{CC}, LN, SLPE, REG and STAB

Power for the IC and its peripheral circuits is usually obtained from the telephone line. The supply voltage is derived from the line via a dropping resistor and regulated by the IC. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE}. The internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch} and the DC resistance of the telephone line R_{line}.

The circuit has an internal current stabilizer operating at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig.9). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.

The regulated voltage on the line terminal (V_{LN}) can be calculated as:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9$$

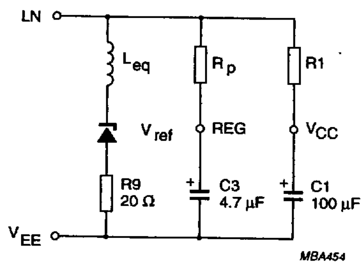
$$V_{LN} = V_{ref} + \{(I_{line} - I_{CC} - 0.5 \times 10^{-3}\ A) - I_p\} \times R9$$

V_{ref} is an internally generated temperature compensated reference voltage of 3.7 V and R9 is an external resistor connected between SLPE and V_{EE}.

In normal use the value of R9 would be 20 Ω.

Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, sidetone level, maximum output swing on LN and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} >> I_{CC} + 0.5\ mA + I_p$, the static behaviour of the circuit is that of a 3.7 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig.3 shows the equivalent impedance of the circuit.



$L_{eq} = C3 \times R9 \times R_p$.
$R_p = 16.2\ k\Omega$.

Fig.3 Equivalent impedance circuit.

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that more sets can be operated in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At line currents below 9 mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor when connected between LN and REG will decrease the internal reference voltage and when connected between REG and SLPE will increase the internal reference voltage.

Current (I_p) available from V_{CC} for peripheral circuits depends on the external components used. Fig.10 shows this current for $V_{CC} > 2.2$ V. If MUTE is LOW (TEA1062) or $\overline{MUTE}$ is HIGH (TEA1062A) when the receiving amplifier is driven, the available current is further reduced. Current availability can be increased by connecting the supply IC (TEA1081) in parallel with R1 as shown in Fig.19(c) and Fig.20(c), or by increasing the DC line voltage by means of an external resistor (R_{VA}) connected between REG and SLPE (Fig.18).

Microphone inputs MIC+ and MIC− and gain pins GAS1 and GAS2

The circuit has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 × 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Figures 14 and 15). Dynamic, magnetic, piezo-electric or electret (with built-in FET source followers) can be used. Microphone arrangements are illustrated in Fig.11.

The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2.

Stability is ensured by two external capacitors, C6 connected between GAS1 and SLPE and C8 connected between GAS1 and V_{EE}. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The value of C8 is 10 times the value of C6. The cut-off frequency corresponds to the time constant R7 × C6.

Input MUTE (TEA1062)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligible clicking on the line and earpiece output. If the number of parallel sets in use causes a drop in line current to below 6 mA the speech amplifiers remain active independent to the DC level applied to the MUTE input.

Input $\overline{MUTE}$ (TEA1062A)

When $\overline{MUTE}$ is LOW or open-circuit, the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when $\overline{MUTE}$ is HIGH. $\overline{MUTE}$ switching causes only negligible clicking on the line and earpiece output. If the number of parallel sets in use causes a drop in line current to below 6 mA the DTMF amplifier becomes active independent to the DC level applied to the $\overline{MUTE}$ input.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled dialling tones may be sent on to the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier IR, QR and GAR

The receiving amplifier has one input (IR) and a non-inverting output (QR). Earpiece arrangements are illustrated in Fig.12. The IR to QR gain is typically 31 dB (when R4 = 100 kΩ). It can be adjusted between 20 and 31 dB to match the sensitivity of the transducer in use. The gain is set with the value of R4 which is connected between GAR and QR. The overall receive gain, between LN and QR, is calculated by subtracting the anti-sidetone network attenuation (32 dB) from the amplifier gain. Two external capacitors, C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 times the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 × C4.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

Automatic gain control input AGC

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}.

The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.8 dB which corresponds to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and average attenuation of 1.2 dB/km). Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.13 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line-loss compensation is required the AGC pin may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Sidetone suppression

The anti-sidetone network, R1//Z_{line}, R2, R3, R8, R9 and Z_{bal}, (see Fig.4) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

$$R9 \times R2 = R1 \times \left(R3 + \frac{R8 \times Z_{bal}}{R8 + Z_{bal}} \right) \qquad (1)$$

$$\frac{Z_{bal}}{Z_{bal} + R8} = \frac{Z_{line}}{Z_{line} + R1} \qquad (2)$$

If fixed values are chosen for R1, R2, R3 and R9, then condition (1) will always be fulfilled when $|R8//Z_{bal}| << R3$.

To obtain optimum sidetone suppression, condition (2) has to be fulfilled which results in:

$$Z_{bal} = \frac{R8}{R1} \times Z_{line} = k \times Z_{line}$$

Where k is a scale factor; $k = \frac{R8}{R1}$

The scale factor k, dependent on the value of R8, is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| << R3$ fulfilling condition (a) and thus ensuring correct anti-sidetone bridge operation
- $|Z_{bal} + R8| >> R9$ to avoid influencing the transmit gain.

In practise Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

EXAMPLE

The balance impedance Z_{bal} at which the optimum suppression is present can be calculated by:

Suppose Z_{line} = 210 Ω + (1265 Ω//140 nF) representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).

When k = 0.64 then R8 = 390 Ω;
Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig.4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Figure 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication *"TEA1060 Family versatile speech transmission ICs for electronic telephone sets, order number 9398 341 10011"*).

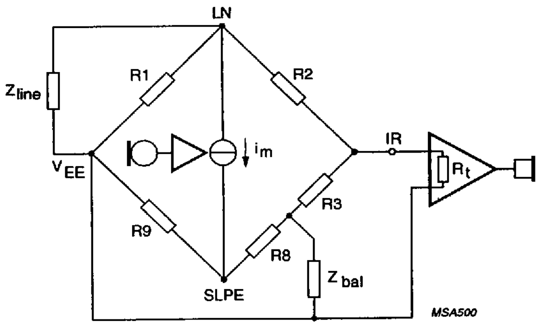


Fig.4 Equivalent circuit of TEA1060 family anti-sidetone bridge.

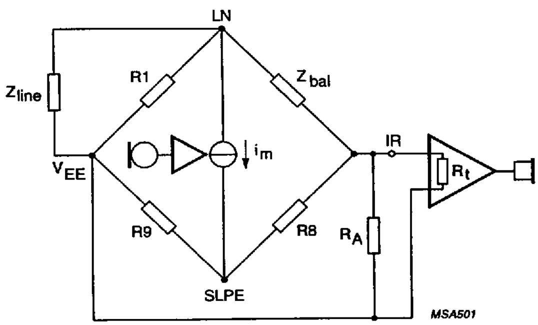


Fig.5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		–	12	V
$V_{LN(R)}$	repetitive line voltage during switch-on or line interruption		–	13.2	V
$V_{LN(RM)}$	repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω; see Fig.18	–	28	V
I_{line}	line current	R9 = 20 Ω; note 1			
	TEA1062; TEA1062A		–	140	mA
	TEA1062T; TEA1062AT		–	140	mA
V_I	input voltage on all other pins	positive input voltage	–	VCC + 0.7	V
		negative input voltage	–	–0.7	V
P_{tot}	total power dissipation	R9 = 20 Ω; note 2			
	TEA1062 (DIP16); TEA1062A		–	666	mW
	TEA1062 (IDF16)		–	617	mW
	TEA1062T; TEA1062AT		–	454	mW
T_{amb}	operating ambient temperature		–25	+75	°C
T_{stg}	storage temperature		–40	+125	°C
T_j	junction temperature		–	+125	°C

Notes

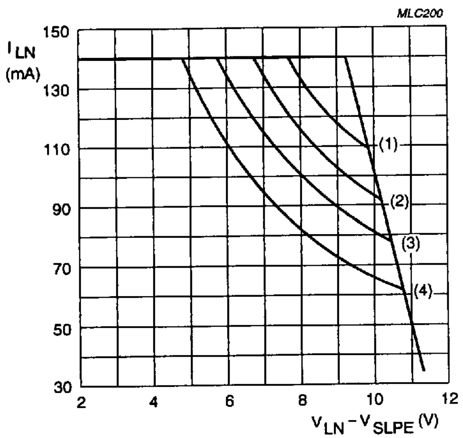
1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE (see Figs 6, 7 and 8).
2. Calculated for the maximum ambient temperature specified (T_{amb} = 75 °C) and a maximum junction temperature of 125 °C.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	TEA1062 (DIP16); TEA1062A	75	K/W
	TEA1062 (IDF16)	81	K/W
	TEA1062T; TEA1062AT (note 1)	110	K/W

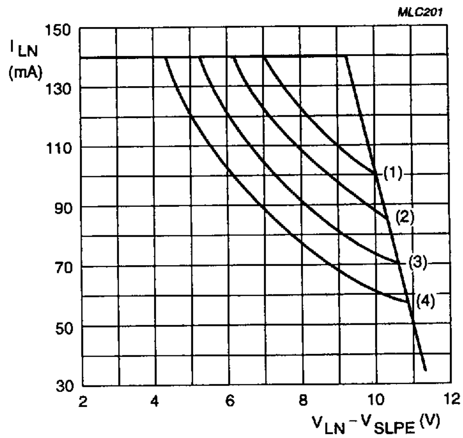
Note

1. Mounted on glass epoxy board 28.5 × 19.1 × 1.5 mm.



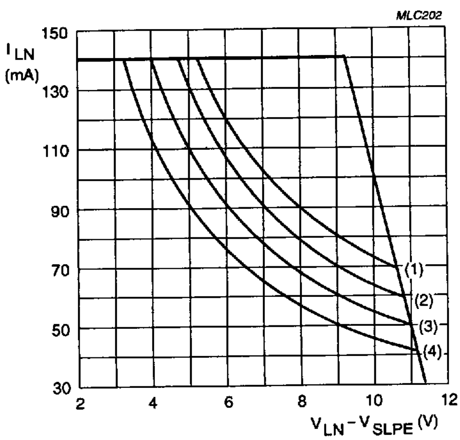
(1) T_{amb} = 45 °C; P_{tot} = 1068 mW.
(2) T_{amb} = 55 °C; P_{tot} = 934 mW.
(3) T_{amb} = 65 °C; P_{tot} = 800 mW.
(4) T_{amb} = 75 °C; P_{tot} = 666 mW.

Fig.6 TEA1062 (DIP16) and TEA1062A safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 988 mW.
(2) T_{amb} = 55 °C; P_{tot} = 864 mW.
(3) T_{amb} = 65 °C; P_{tot} = 741 mW.
(4) T_{amb} = 75 °C; P_{tot} = 617 mW.

Fig.7 TEA1062 (IDF16) safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 727 mW.
(2) T_{amb} = 55 °C; P_{tot} = 636 mW.
(3) T_{amb} = 65 °C; P_{tot} = 545 mW.
(4) T_{amb} = 75 °C; P_{tot} = 454 mW.

Fig.8 TEA1062T and TEA1062AT safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies LN and V_{CC} (pins 1 and 13)						
V_{LN}	voltage drop over circuit between LN and V_{EE}	MIC inputs open-circuit				
		I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	1.9	–	V
		I_{line} = 15 mA	3.55	4.0	4.25	V
		I_{line} = 100 mA	4.9	5.7	6.5	V
		I_{line} = 140 mA	–	–	7.5	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	–	−0.3	–	mV/K
V_{LN}	voltage drop over circuit between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA				
		R_{VA} (LN to REG) = 68 kΩ	–	3.5	–	V
		R_{VA} (REG to SLPE) = 39 kΩ	–	4.5	–	V
I_{CC}	supply current	V_{CC} = 2.8 V	–	0.9	1.35	mA
V_{CC}	supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH				
	TEA1062	I_p = 1.2 mA	2.2	2.7	–	V
		I_p = 0 mA	–	3.4	–	V
V_{CC}	supply voltage available for peripheral circuitry	I_{line} = 15 mA; $\overline{MUTE}$ = LOW				
	TEA1062A	I_p = 1.2 mA	2.2	2.7	–	V
		I_p = 0 mA	–	3.4	–	V
Microphone inputs MIC− and MIC+ (pins 6 and 7)						
$\lvert Z_i \rvert$	input impedance					
	differential	between MIC− and MIC+	–	64	–	kΩ
	single-ended	MIC− or MIC+ to V_{EE}	–	32	–	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain MIC+ or MIC− to LN	I_{line} = 15 mA; R7 = 68 kΩ	50.5	52.0	53.5	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 and +75 °C	–	±0.2	–	dB
DTMF input (pin 11)						
$\lvert Z_i \rvert$	input impedance		–	20.7	–	kΩ
G_v	voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	24.0	25.5	27.0	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	I_{line} = 50 mA; T_{amb} = −25 and +75 °C	–	±0.2	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain adjustment inputs GAS1 and GAS2 (pins 2 and 3)						
ΔG_v	transmitting amplifier gain variation by adjustment of R7 between GAS1 and GAS2		−8	−	0	dB
Sending amplifier output LN (pin 1)						
$V_{LN(rms)}$	output voltage (RMS value)	THD = 10%				
		I_{line} = 4 mA	−	0.8	−	V
		I_{line} = 15 mA	1.7	2.3	−	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC− and MIC+; psophometrically weighted (P53 curve)	−	−69	−	dBmp
Receiving amplifier input IR (pin 10)						
$\lvert Z_i \rvert$	input impedance		−	21	−	kΩ
Receiving amplifier output QR (pin 4)						
$\lvert Z_o \rvert$	output impedance		−	4	−	Ω
G_v	voltage gain from IR to QR	I_{line} = 15 mA; R_L = 300 Ω (from pin 9 to pin 4)	29.5	31	32.5	dB
ΔG_{vf}	gain variation with frequency referenced to 800 Hz	f = 300 and 3400 Hz	−	±0.2	−	dB
ΔG_{vT}	gain variation with temperature referenced to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 and +75 °C	−	±0.2	−	dB
$V_{o(rms)}$	output voltage (RMS value)	THD = 2%; sine wave drive; R4 = 100 kΩ; I_{line} = 15 mA; I_p = 0 mA				
		R_L = 150 Ω	0.22	0.33	−	V
		R_L = 450 Ω	0.3	0.48	−	V
$V_{o(rms)}$	output voltage (RMS value)	THD = 10%; R4 = 100 kΩ; R_L = 150 Ω; I_{line} = 4 mA	−	15	−	mV
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted (P53 curve); R_L = 300 Ω	−	50	−	μV
Gain adjustment input GAR (pin 5)						
ΔG_v	receiving amplifier gain variation by adjustment of R4 between GAR and QR		−11	−	0	dB
Mute input (pin 12)						
V_{IH}	HIGH level input voltage		1.5	−	V_{CC}	V
V_{IL}	LOW level input voltage		−	−	0.3	V
I_{MUTE}	input current		−	8	15	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reduction of gain						
ΔG_v	MIC+ or MIC– to LN					
	TEA1062	MUTE = HIGH	–	70	–	dB
	TEA1062A	$\overline{MUTE}$ = LOW	–	70	–	dB
G_v	voltage gain from DTMF to QR	R4 = 100 kΩ; R_L = 300 Ω				
	TEA1062	MUTE = HIGH	–	–17	–	dB
	TEA1062A	$\overline{MUTE}$ = LOW	–	–17	–	dB
Automatic gain control input AGC (pin 15)						
ΔG_v	controlling the gain from IR to QR and the gain from MIC+, MIC– to LN gain control range	R6 = 110 kΩ (between AGC and V_{EE}) I_{line} = 70 mA	–	–5.8	–	dB
I_{lineH}	highest line current for maximum gain		–	23	–	mA
I_{lineL}	lowest line current for minimum gain		–	61	–	mA

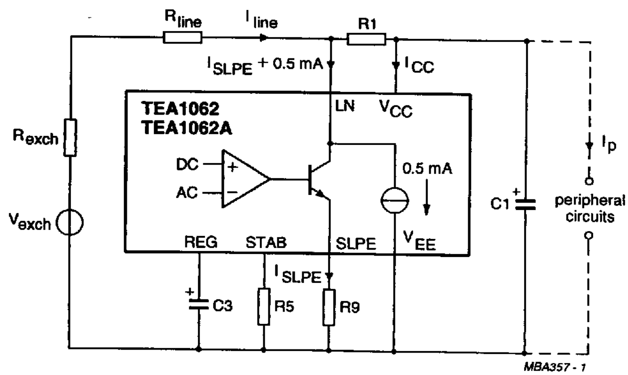
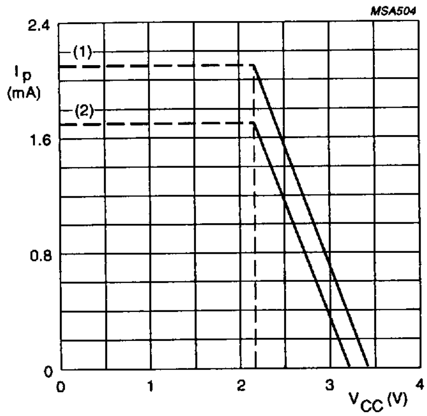


Fig.9 Supply arrangement.



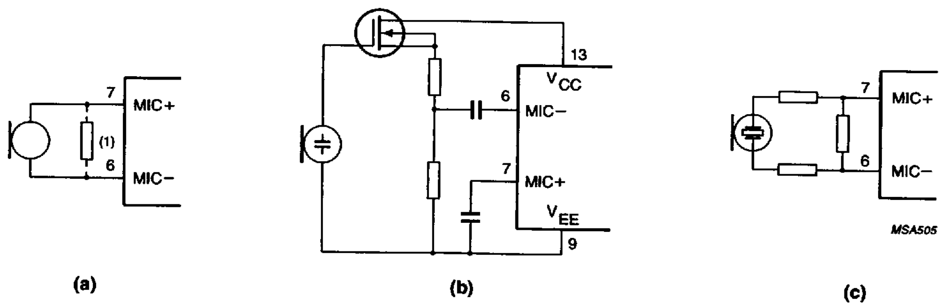
The supply possibilities can be increased by setting the voltage drop over the circuit V_{LN} to a higher value by resistor R_{VA} connected between REG and SLPE.

$V_{CC} > 2.2$ V; $I_{line} = 15$ mA at $V_{LN} = 4$ V; R1 = 620 Ω; R9 = 20 Ω.

(1) $I_p = 2.1$ mA. Curve (1) is valid when the receiving amplifier is not driven or when MUTE = HIGH (TEA1062), $\overline{MUTE}$ = LOW (TEA1062A).

(2) $I_p = 1.7$ mA. Curve (2) is valid when MUTE = LOW (TEA1062), $\overline{MUTE}$ = HIGH (TEA1062A) and the receiving amplifier is driven; $V_{o(rms)} = 150$ mV, $R_L = 150$ Ω.

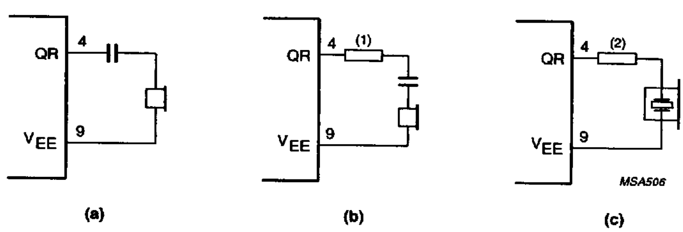
Fig.10 Typical current I_p available from V_{CC} for peripheral circuitry.



(a) Magnetic or dynamic microphone.
(b) Electret microphone.
(c) Piezo-electric microphone.

(1) Resistor may be connected to reduce the terminating impedance.

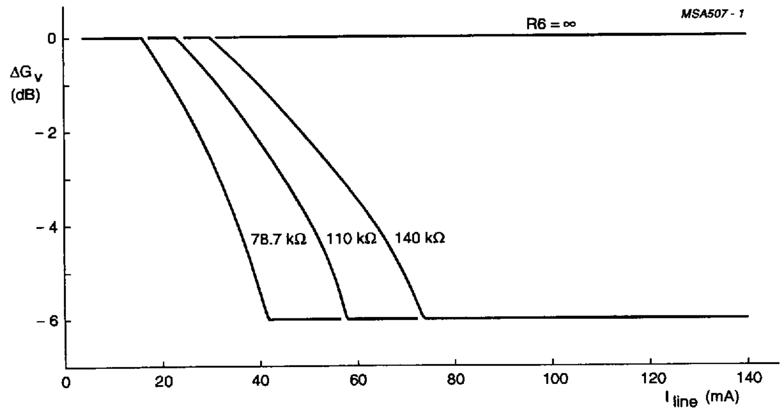
Fig.11 Alternative microphone arrangements.



(a) Dynamic earpiece.
(b) Magnetic earpiece.
(c) Piezo-electric earpiece.

(1) Resistor may be connected to prevent distortion (inductive load).
(2) Resistor is required to increase the phase margin (capacitive load).

Fig.12 Alternative receiver arrangements.

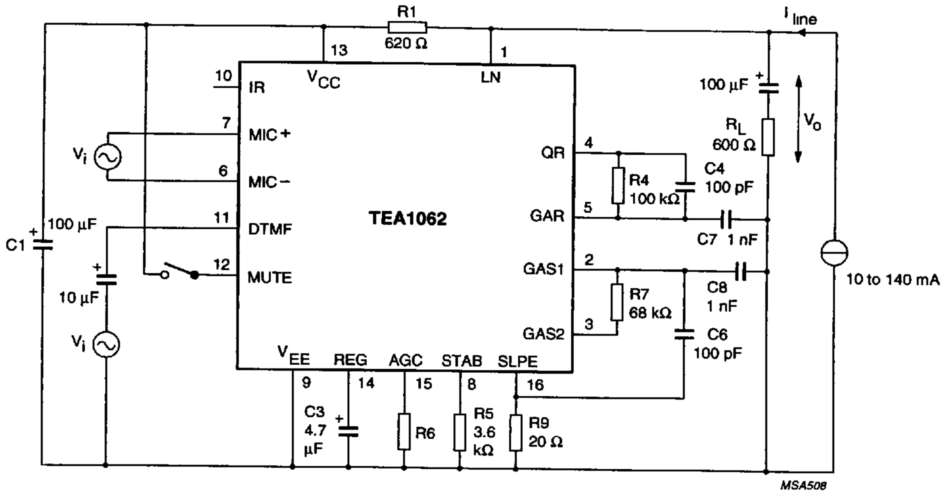


R9 = 20 Ω.

Fig.13 Variation of gain as a function of line current with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

V_{exch} (V)	400 R_{exch} (Ω)	600 R_{exch} (Ω)	800 R_{exch} (Ω)	1 000 R_{exch} (Ω)
	R6 (kΩ)			
36	100	78.7	–	–
48	140	110	93.1	82
60	–	–	120	102



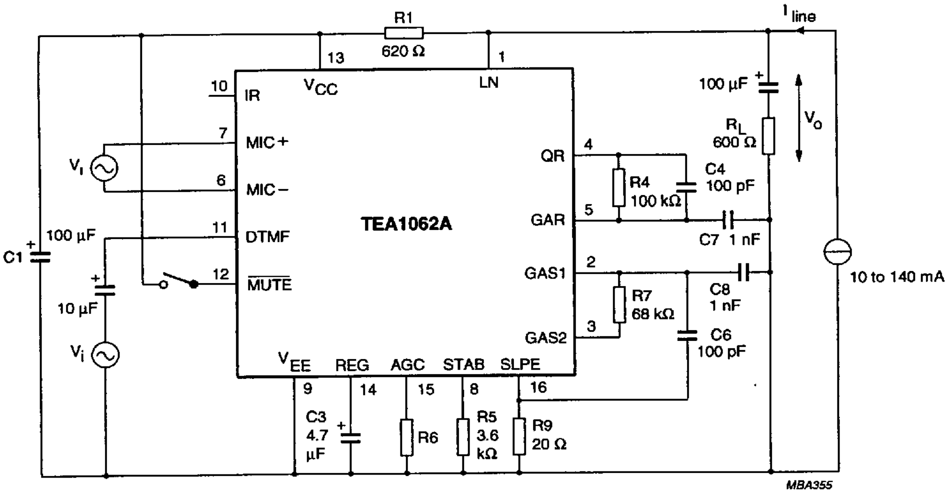
Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.

For measuring gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit.

For measuring the DTMF input, the MUTE input should be HIGH.

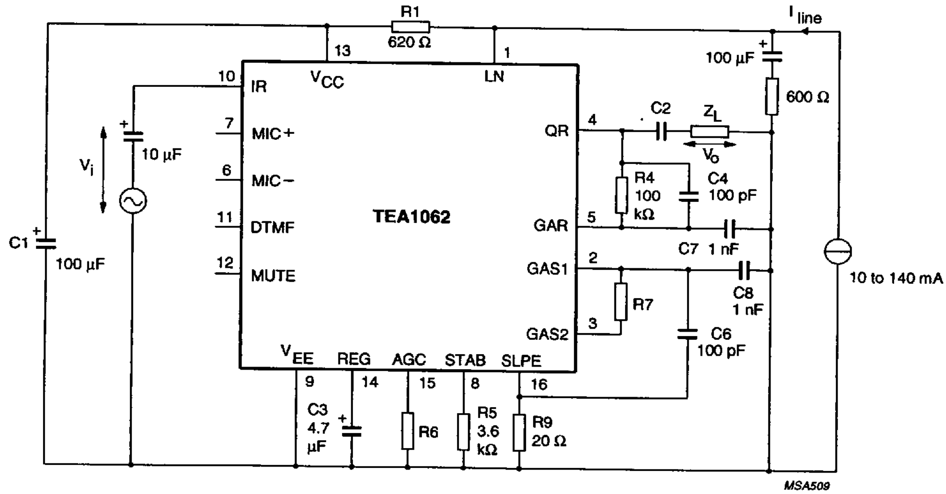
Inputs not being tested should be open-circuit.

Fig.14 Test circuit for defining TEA1062 voltage gain of MIC+, MIC− and DTMF inputs.



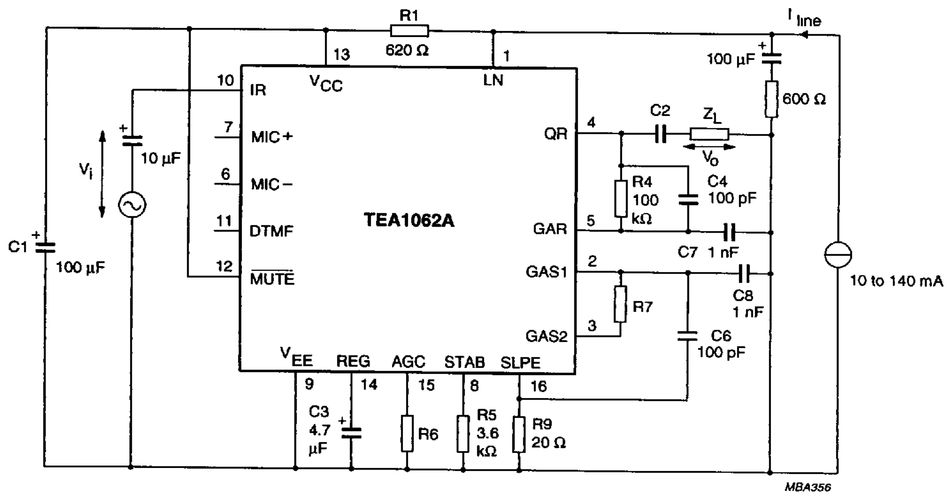
Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.
For measuring gain from MIC+ and MIC− the $\overline{\text{MUTE}}$ input should be HIGH.
For measuring the DTMF input, the $\overline{\text{MUTE}}$ input should be LOW or open-circuit.
Inputs not being tested should be open-circuit.

Fig.15 Test circuit for defining TEA1062A voltage gain of MIC+, MIC− and DTMF inputs.



Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.

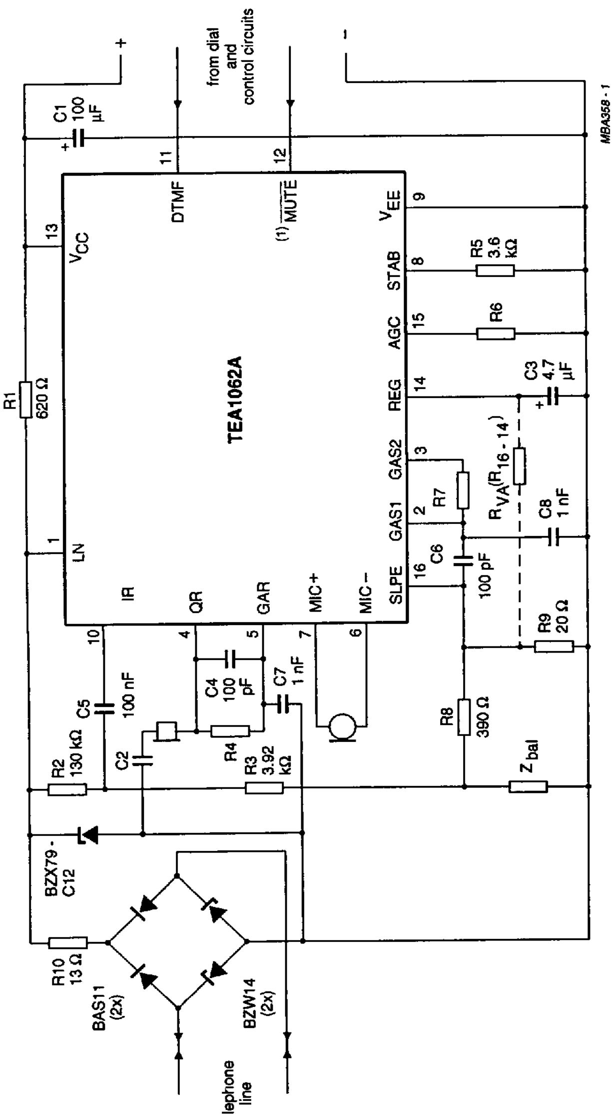
Fig.16 Test circuit for defining TEA1062 voltage gain of the receiving amplifier.



Voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.

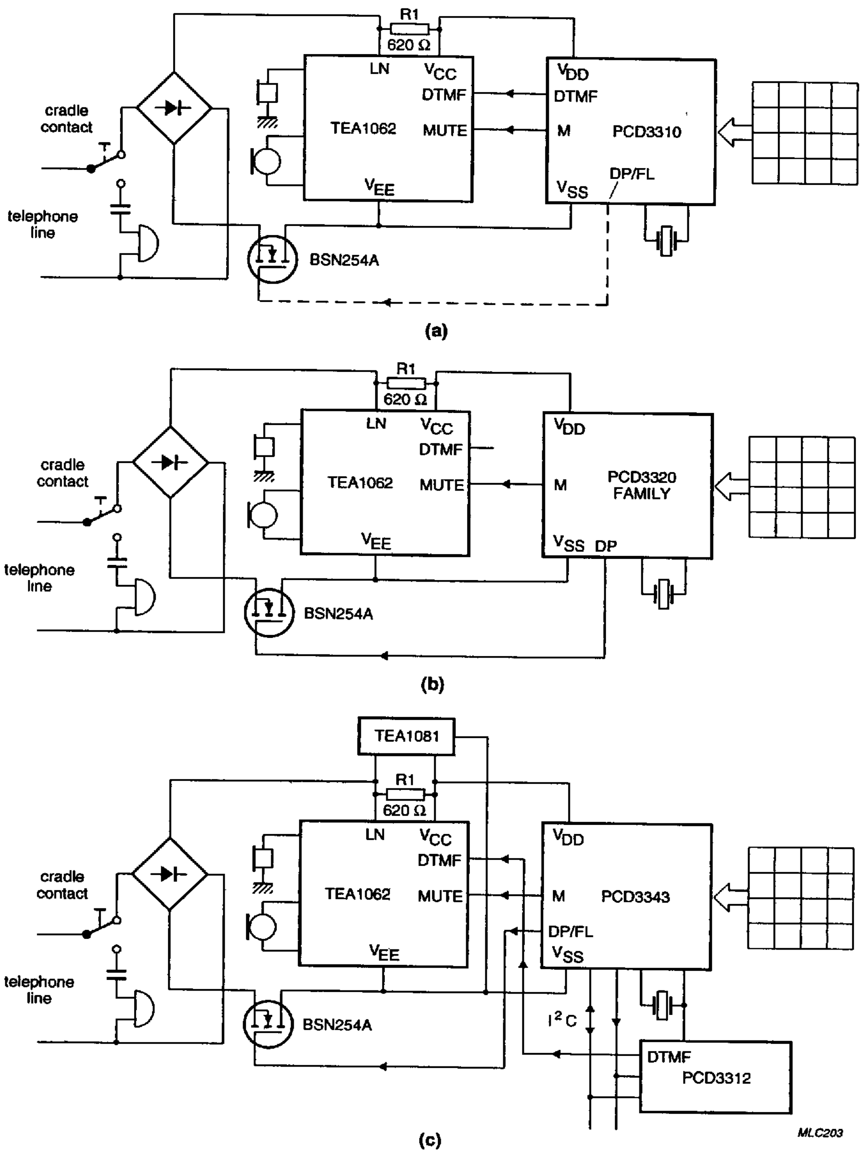
Fig.17 Test circuit for defining TEA1062A voltage gain of the receiving amplifier.

APPLICATION INFORMATION



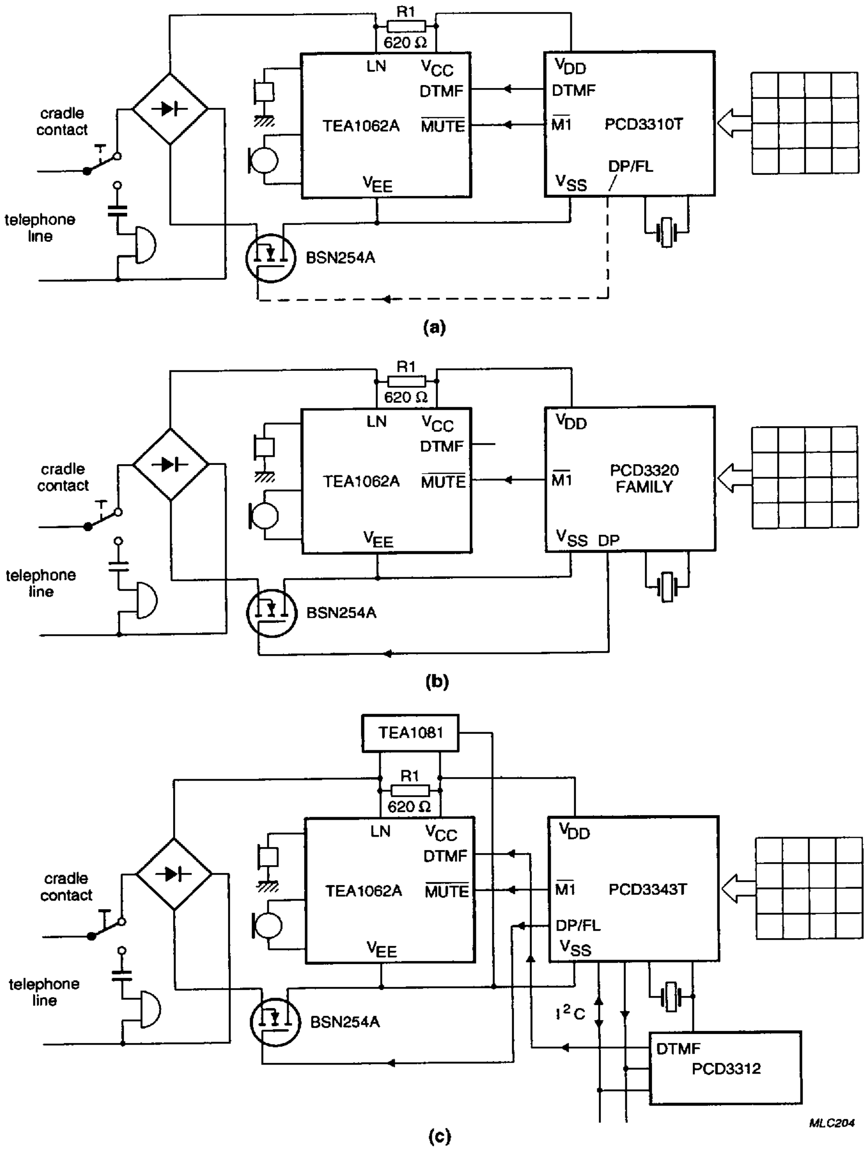
The diode bridge, the Zener diode and R10 limit the current into, and the voltage across, the circuit during line transients.
A different protection arrangement is required for pulse dialling or register recall.
The DC line voltage can be set to a higher value by the resistor R_{VA} (REG to SLPE).
Further application information can be found in Application note *ETT/AN 89008*.
(1) Pin 12 is active HIGH (MUTE) for TEA1062.

Fig.18 Typical application of TEA1062A, with piezo-electric earpiece and DTMF dialling.



(a) DTMF pulse set with CMOS bilingual dialling circuit PCD3310. The dashed line shows an optional flash (register recall by timed loop break).
(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.
(c) Dual standard (pulse and DTMF) feature phone with the PCD3343 CMOS controller and the PCD3312 CMOS DTMF generator with I^2C-bus. Supply is provided by the TEA1081 supply circuit.

Fig.19 Typical simplified applications of the TEA1062.



(a) DTMF pulse set with CMOS bilingual dialling circuit PCD3310T. The dashed line shows an optional flash (register recall by timed loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual standard (pulse and DTMF) feature phone with the PCD3343T CMOS controller and the PCD3312 CMOS DTMF generator with I^2C-bus. Supply is provided by the TEA1081 supply circuit.

Fig.20 Typical simplified applications of the TEA1062A.