ZETEX SEMICONDUCTORS

N-channel enhancement mode vertical DMOS FET

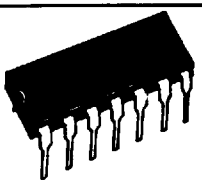
ZVN2106

FEATURES

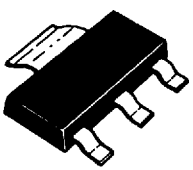
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

E-LINE (TO-92)
SUFFIX A

TO-39
SUFFIX B



14 LEAD MOULDED DIL
SUFFIX E



SOT-223
SUFFIX G

DESCRIPTION

A compact interdigitated geometry forms the basis of this Zetex MOSFET. Optimised for low on-resistance, low capacitance and fast switching, this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN2106A*	60V	0.45A	2Ω
ZVN2106B*	60V	1.2A	2Ω
ZVN2106E	60V	0.45A	2Ω
ZVN2106G	60V	0.7A	2Ω

*BS-CECC approved

ZVN2106

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	DIL	SOT-223	Units
V_{DS}	Drain-source voltage	60	60	60	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.45	0.45	0.45	0.7	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	1.2	–	–	A
I_{DM}	Pulsed drain current	8	8	3	8	A
V_{GS}	Gate-source voltage	±20	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	0.85	2	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150				°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	–	2.4	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	0.5	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	0.1	mA	$V_{DS} = 0.8 \times$ Max. rating, $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	2	3	–	A	$V_{DS} = 18V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	2	Ω	$I_D = 1A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	0.3	0.4	–	S	$V_{DS} = 18V$, $I_D = 1A$
C_{iss}	Input capacitance (2)	–	60	75	pF	$V_{DS} = 18V$, $V_{GS} = 0V$, f = 1MHz
C_{oss}	Common source output capacitance (2)	–	30	45	pF	
C_{rss}	Reverse transfer capacitance (2)	–	15	20	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	4	7	ns	$V_{DD} \approx 18V$, $I_D = 1A$
t_r	Rise time (2) (3)	–	5	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	8	12	ns	
t_f	Fall time (2) (3)	–	10	15	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.82	V	$V_{GS}=0V$, $I_S=0.45A$
t_{rr}	Reverse recovery time	50	ns	$V_{GS}=0V$, $I_F=0.45A$ $I_R=0.1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

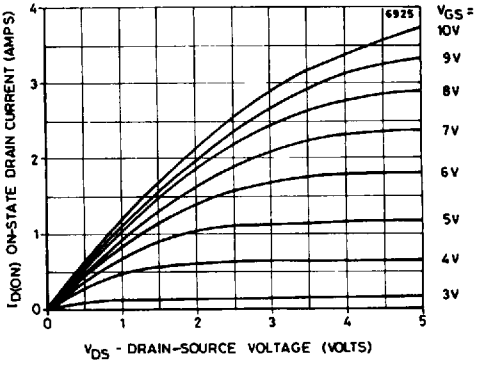


Fig. 1 Typical saturation characteristics

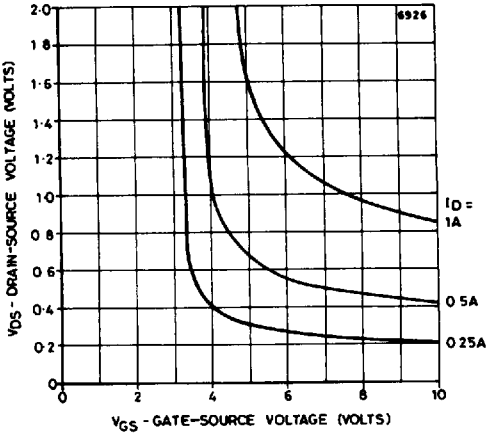


Fig. 2 Typical voltage saturation characteristics

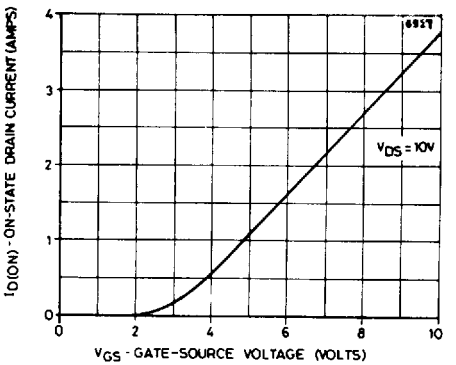


Fig. 3 Typical transfer characteristics

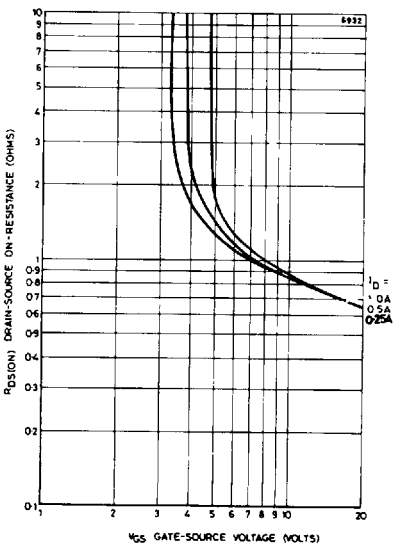


Fig. 4 Typical on-resistance v gate-source voltage

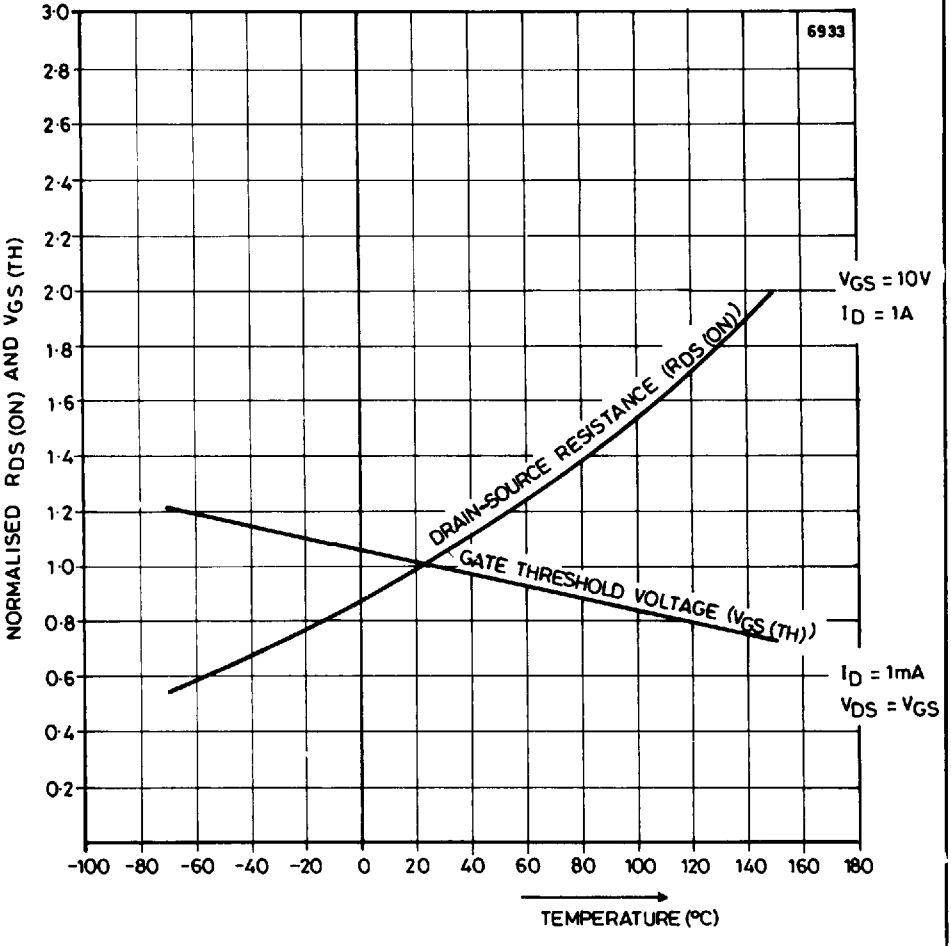


Fig. 5 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

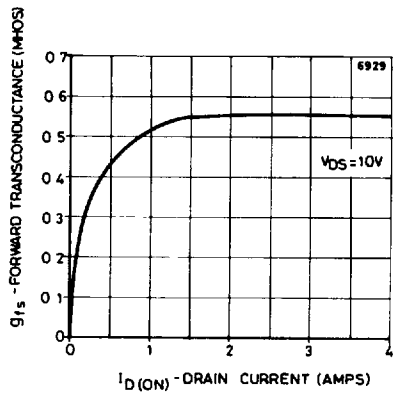


Fig. 6 Typical transconductance v drain current

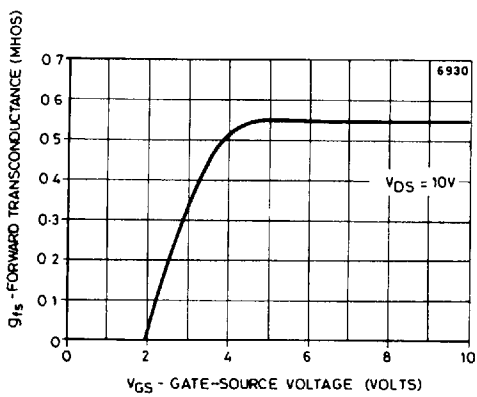


Fig. 7 Typical transconductance v gate-source voltage

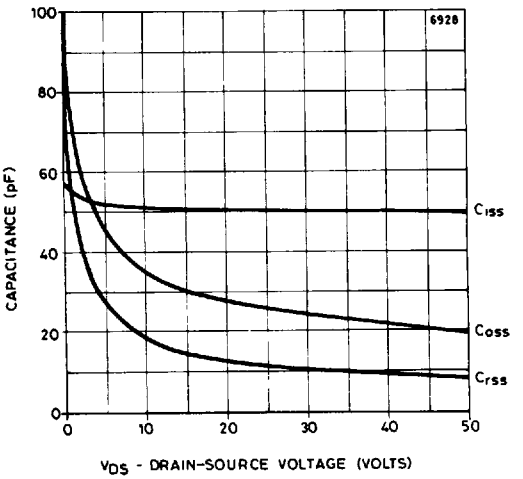


Fig. 8 Typical capacitance v drain-source voltage

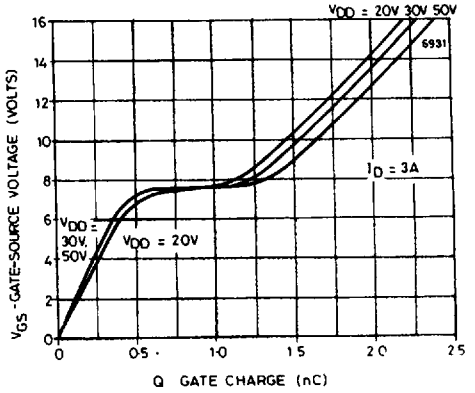


Fig. 9 Typical gate charge v gate-source voltage

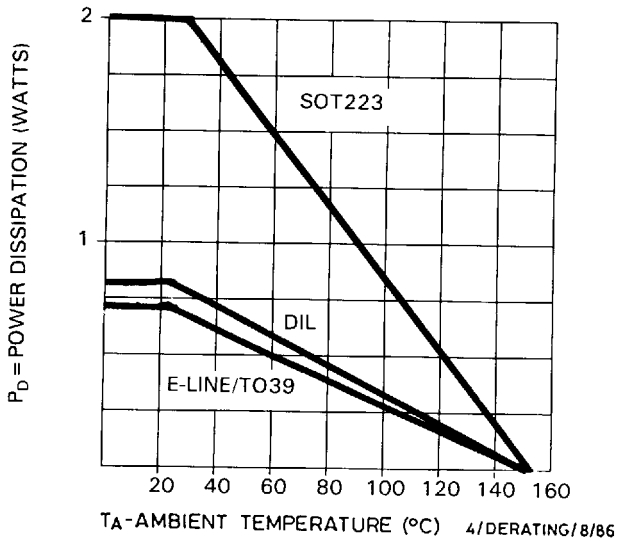


Fig. 10 Power v temperature derating curve (ambient)

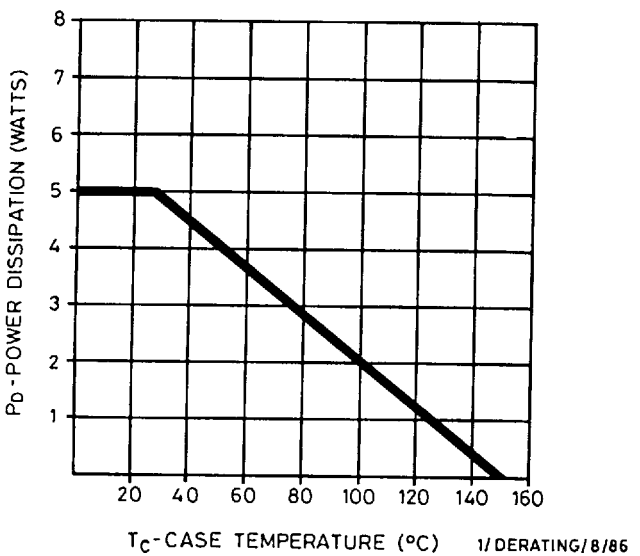


Fig. 11 Power v temperature derating curve (case)