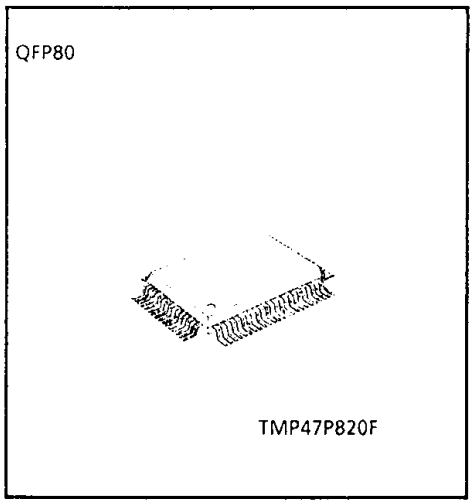
CMOS 4-BIT MICROCONTROLLER

TMP47P820F

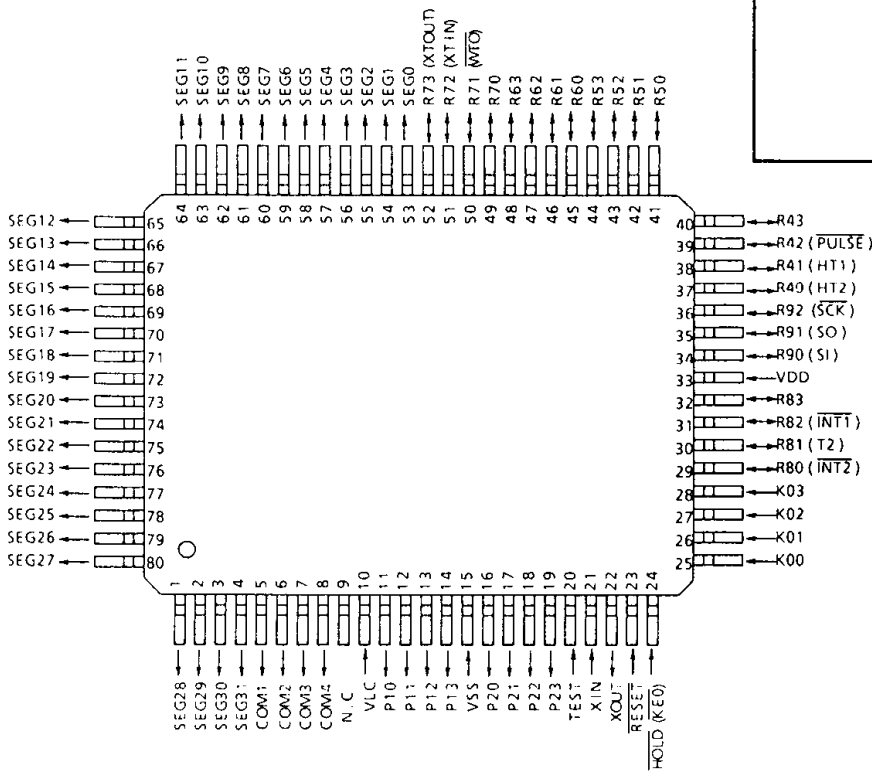
The 47P820 is the OTP microcontroller with 64kbits PROM. For program operation, the programming is achieved by using with EPROM programmer (TMM2764AD type) and adapter socket (BM1112).
A.C./D.C characteristics are equivalent to Mask-programed ROM device.

PART No.	ROM	RAM	PACKAGE
TMP47P820F	OTP 8192 × 8-bit	512 × 4-bit	QFP80

PIN ASSIGNMENT (TOP VIEW)



QFP80



PIN FUNCTION

The 47P820 has MCU mode and PROM mode.

(1) MCU mode

The 47C820 and the 47P820 are pin compatible (TEST pin for out-going test, Be fixed to low level).

(2) PROM mode

PIN NAME	Input/Output	FUNCTIONS	PIN NAME (MCU MODE)
A12 - A9	Input	Address inputs	P10 - P13
A8 - A5			P20 - P23
A4			R50
A3 - A0			R80 - R83
I7 - I4	I/O	Data inputs / outputs	R73 - R70
I3 - I0			K03 - K00
$\overline{PGM}$	Input	Program control input	R92
$\overline{CE}$		Chip Enable input	R91
$\overline{OE}$		Output Enable input	R90
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
VSS		0V	VSS
SEG31 - SEG0	Output	Open	
COM4 - COM1			
VLC	Power supply		
N.C.			
R53 - R51	I/O	Be fixed to low level	
R63 - R60			
R43 - R42			
R41 - R40		PROM mode setting pins. Be fixed to low level.	
$\overline{RESET}$	Input		
$\overline{HOLD}$	Input		
XIN	Input	Resonator connecting pins	
XOUT	Output		

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P820.
The 47P820 is the same as the 47C620 / 820 except that an EPROM or OTP is used instead of a Mask ROM.

1. OPERATION MODE

The 47P820 has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST / VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C620 / 820, except that the TEST / VPP pin does not have pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C820. Data conversion tables must be set in two locations when using the 47P820 to check 47C620 operation.

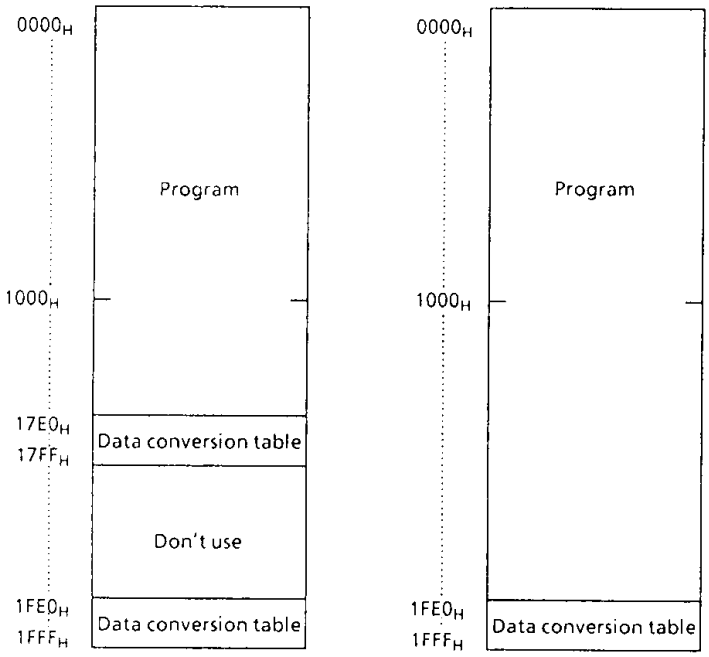


Figure 1-1. Program area

1.1.2 Data Memory

The 47P820 has two 256x4-bit data memory banks (DMB0, DMB1).
When using the 47P820 as a 47C620 evaluator, do not write data to address 80_H and following, even though the DMB1 addresses are 00-FF_H. There is no necessary to take into consideration a special function Shared area because one is built in DMB0.

1.1.3 Input/Output Circuitry

(1) Control pins
This is the same as for the 47C620/820 except that there is no built-in pull-down resistance for the TEST pin.

(2) I/O Ports
The input/output circuit of the 47P820 is the same as I/O code GA of the 47C620/820.
External resistance, for example, is required when using as evaluator of other I/O codes (GB~GF) (Refer to Figure 1-3).

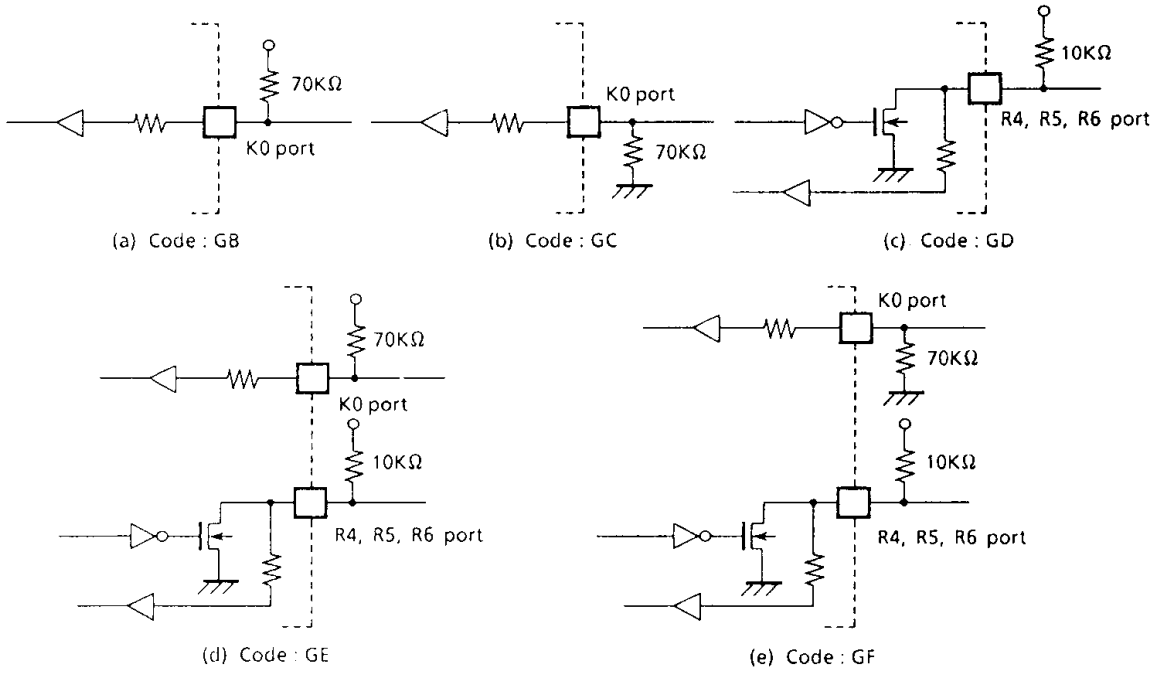


Figure 1-2. I/O code and external circuitry

1.2 PROM mode

The PROM mode is set by setting the $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$, K00 and K01 pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM2764AD).

An adapter socket (part No. BM1112) is available for connecting a PROM writer.

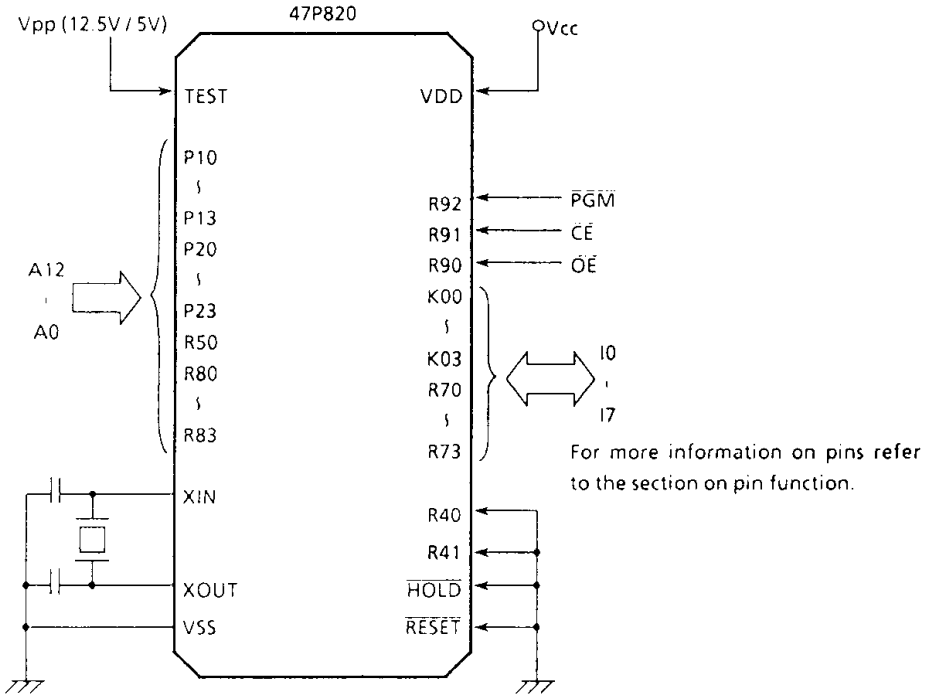


Figure 1-3. Setting for PROM mode

1.2.1 High Speed Programming Mode

The device is set up in the high speed programming mode when the programming voltage (12.5V) is applied to the Vpp terminal with Vcc = 6V and $\overline{PGM}$ = V_{IH4}. The programming is achieved by applying a Single TTL low level 1 msec, pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using program Verify Mode. If the programmed data is not correct, another program pulse of 1 msec is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 15 times). After correctly programming the selected address, one additional program pulse with pulse width 4 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5V.

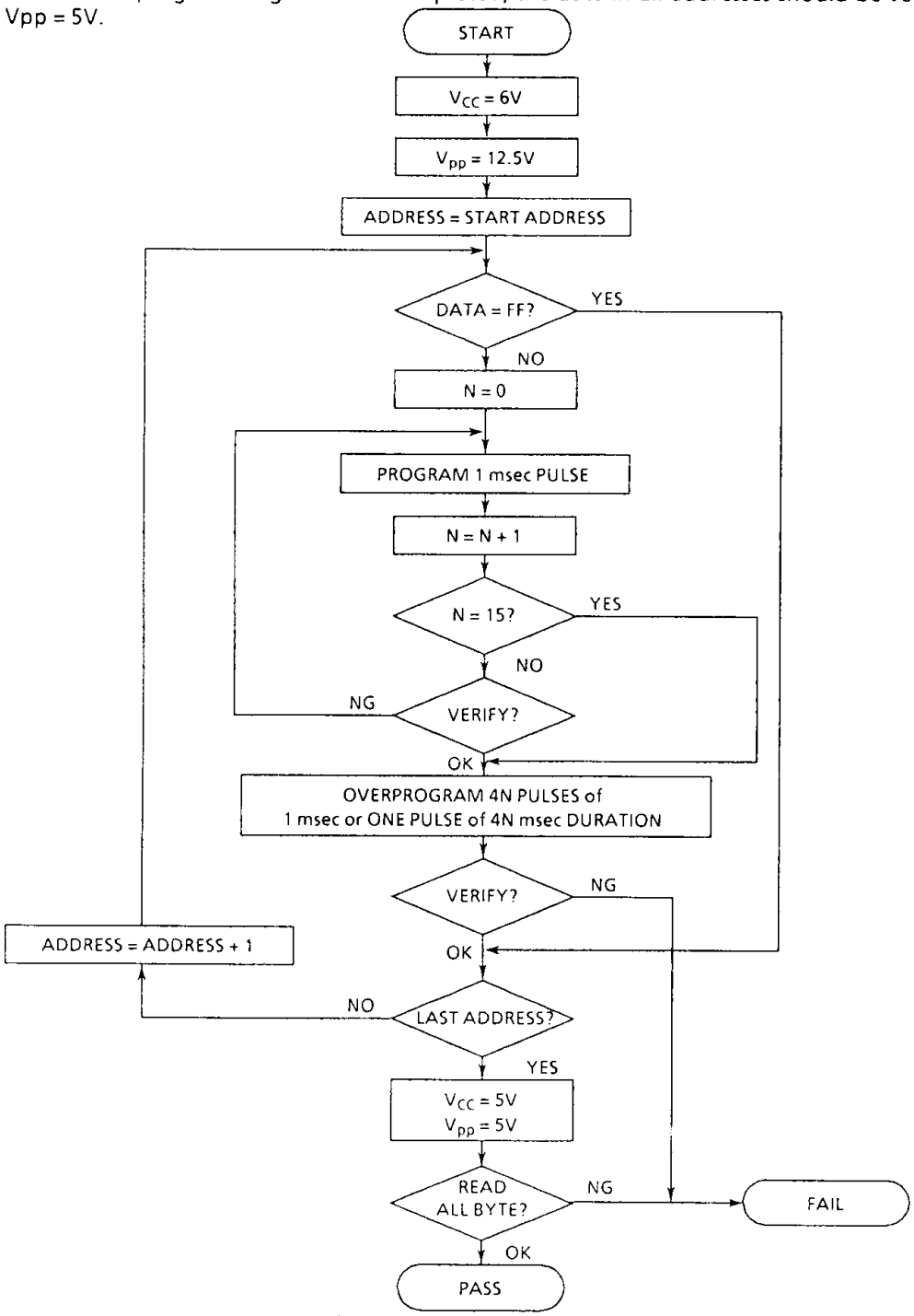


Figure1-4. FLOW CHART

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		− 0.3 to 7	V
Program Voltage	V_{PP}		− 0.3 to 14.0	V
Supply Voltage (LCD drive)	V_{LC}		− 0.3 to V_{DD} + 0.3	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.3 to V_{DD} + 0.3	mA
	V_{OUT2}	Sink open drain pin	− 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2	15	mA
	I_{OUT2}	Ports R4 to R9	3.2	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2	60	mA
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 40 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	6.0	MHz
	fs	XTIN, XTOUT		30.0	34.0	KHz

Note. Input Voltage V_{IH3}, V_{IL3} : in the SLOW and HOLD mode.

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = −40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	−	−	±2	μA
	I_{IN2}	Open drain R port					
Input Registance	R_{IN2}	$\overline{RESET}$		100	220	450	KΩ
Output Leakage Current	I_{LO}	Open drain ports P, R	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	−	2	μA
Output Low Voltage	V_{OL2}	Except XOUT XTOUT and ports P1, P2	V_{DD} = 4.5V, I_{OL} = 1.6mA	−	−	0.4	V
Output Low Current	I_{OL1}	Ports P1, P2	V_{DD} = 4.5V, V_{OL} = 1.0V	−	10	−	mA
Segment Output Registance	R_{OS}	SEG pin	V_{DD} = 5V, V_{DD} − V_{LC} = 3V	−	20	−	KΩ
Common Output Registance	R_{OC}	COM pin					
Segment/Common Output Registance	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	−	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0V, fs = 32.768KHz	−	30	−	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	−	0.5	10	μA

Note 1. *Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.*

Note 2. *Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.*

Note 3. *Output Resistance R_{OS}, R_{OC} ; Shows on-resistance at the level switching.*

Note 4. *$V_{O2/3}$; Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.*
$V_{O1/2}$; Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.
$V_{O1/3}$; Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 5. *Supply Current I_{DD} ; V_{IN} = 5.3V/0.2V*
The K0 port is open when the input resistor is contained.
The voltage applied to the R port is within the valid range.

Note 6. *Supply Current I_{DDS} ; V_{IN} = 2.8V/0.2V. Only low frequency clock is only osillated (connecting XTIN, XTOUT).*

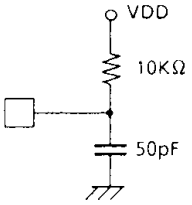
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70°C)

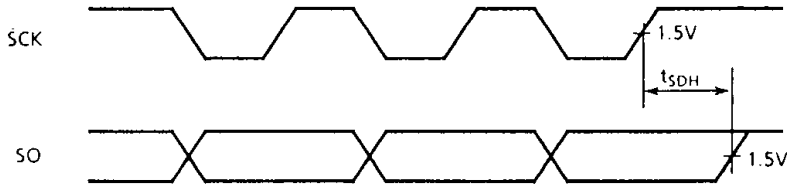
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	in the Normal mode	1.9	–	20	μs
		in the SLOW mode	235	–	267	μs
High Level Clock Pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	–	–	ns
High Speed Timer/Counter input frequency	f_{HT}		–	–	fc	MHz

Note. Shift data Hold time :

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70°C)

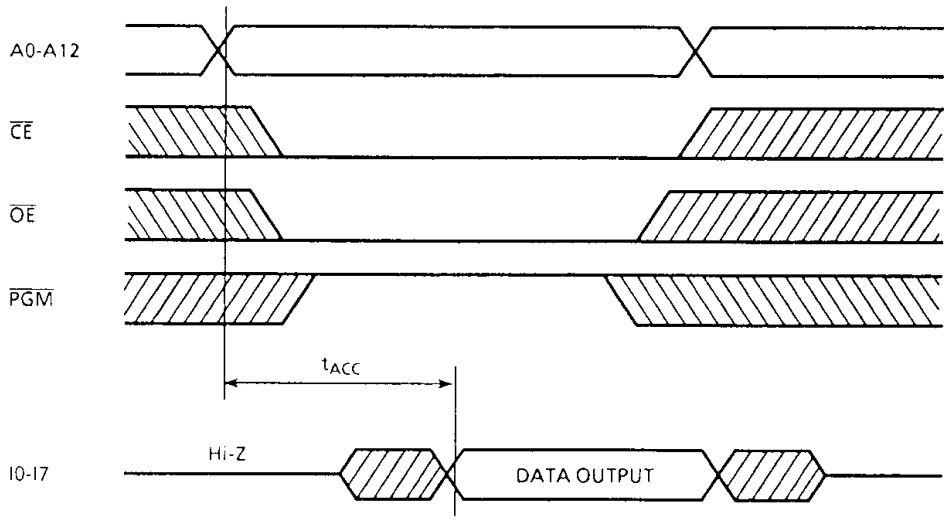
Recommended oscillating conditions of the 47P820 are equal to the 47C820's.

D.C./A.C. CHARACTERISTICS

(V_{SS} = 0V)

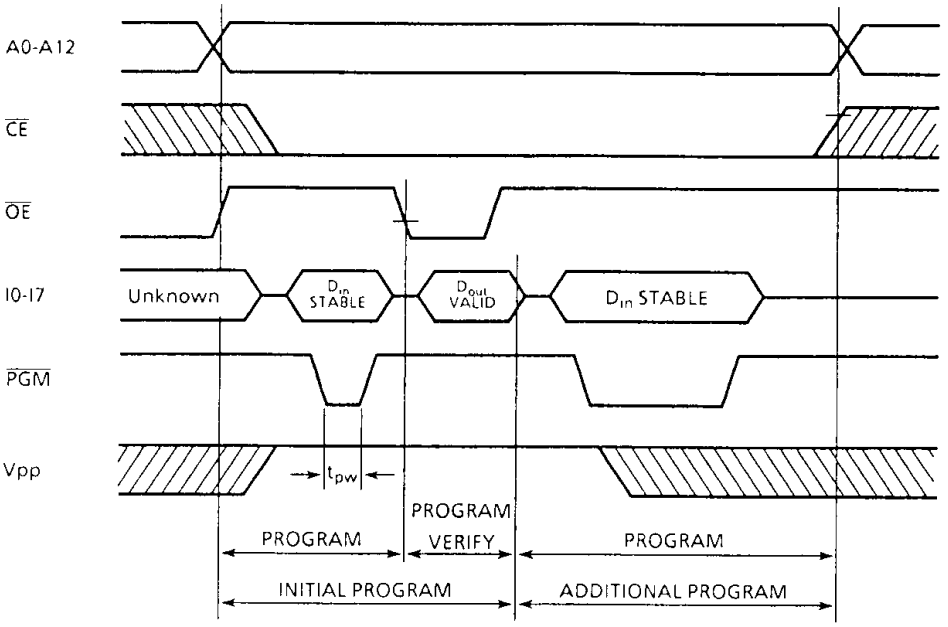
(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.1$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25V	0	–	350	ns

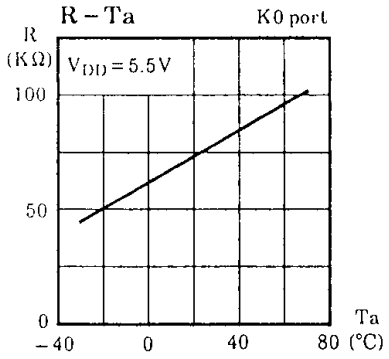


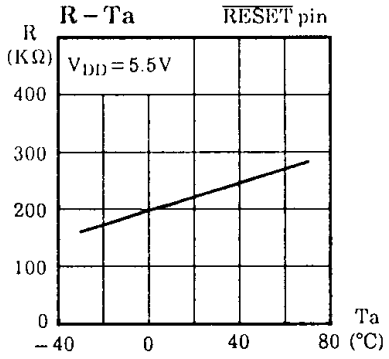
(2) High Speed Programming Operation

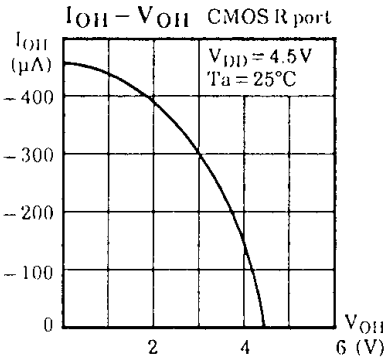
PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	-	V_{CC}	V
Input Low Voltage	V_{IL4}		0	-	$V_{CC} \times 0.1$	V
Supply Voltage	V_{CC}		4.75	-	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.25	12.50	12.75	V
Programming Pulse Width	t_{PW}	$V_{CC} = 6.0 \pm 0.25V$	0.95	1.0	1.05	ms

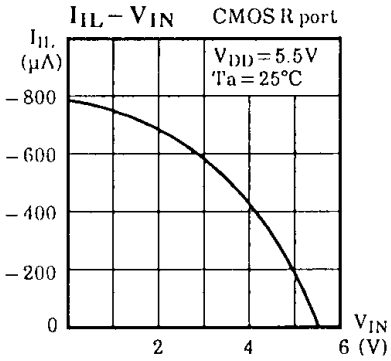


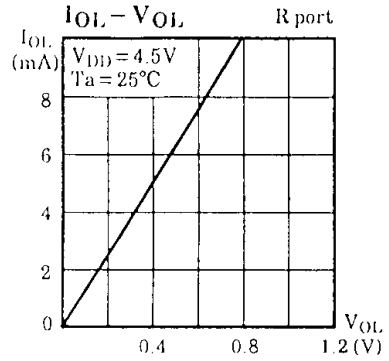
TYPICAL CHARACTERISTICS

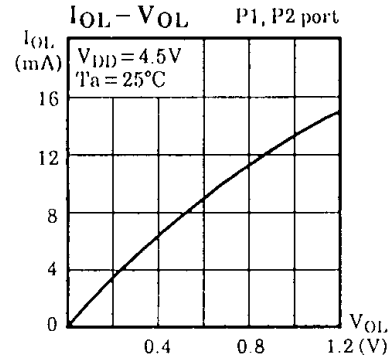


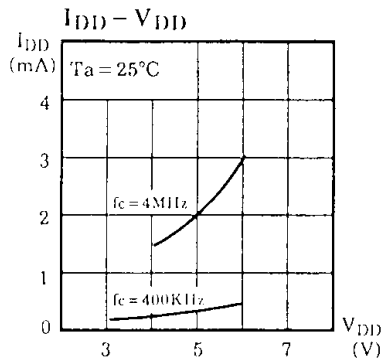


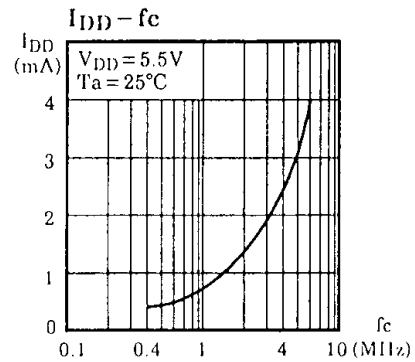












Note. Be fixed low level at MCU mode because TEST pin does not built in pull-down resistor.