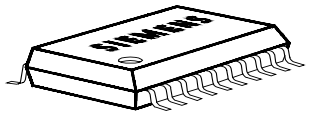
# Smart High-Side Power Switch
# Two Channels: 2 x 40mΩ
# Status Feedback

## Product Summary

| | | | |
|---|---|---|---|
| Operating Voltage | $V_{bb(on)}$ | 4.75...41V | |
| Active channels | | one | two parallel |
| On-state Resistance | $R_{ON}$ | 40mΩ | 20mΩ |
| Nominal load current | $I_{L(NOM)}$ | 4.8A | 7.3A |
| Current limitation | $I_{L(SCr)}$ | 30A | 30A |

## Package

**P-DSO-20-9**



## General Description

- N channel vertical power MOSFET with charge pump, ground referenced CMOS compatible input and diagnostic feedback, monolithically integrated in Smart SIPMOS® technology.
- Fully protected by embedded protection functions

## Applications

- µC compatible high-side power switch with diagnostic feedback for 5V, 12V and 24V grounded loads
- All types of resistive, inductive and capacitve loads
- Most suitable for loads with high inrush currents, so as lamps
- Replaces electromechanical relays, fuses and discrete circuits

## Basic Functions

- Very low standby current
- CMOS compatible input
- Fast demagnetization of inductive loads
- Stable behaviour at undervoltage
- Wide operating voltage range
- Logic ground independent from load ground

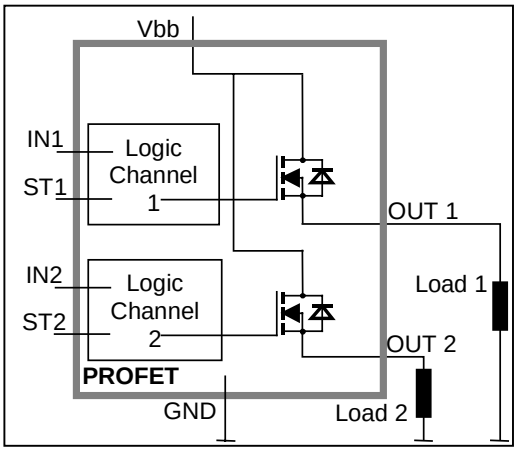
## Protection Functions

- Short circuit protection
- Overload protection
- Current limitation
- Thermal shutdown
- Overvoltage protection (including load dump) with external resistor
- Reverse battery protection with external resistor
- Loss of ground and loss of $V_{bb}$ protection
- Electrostatic discharge protection (ESD)

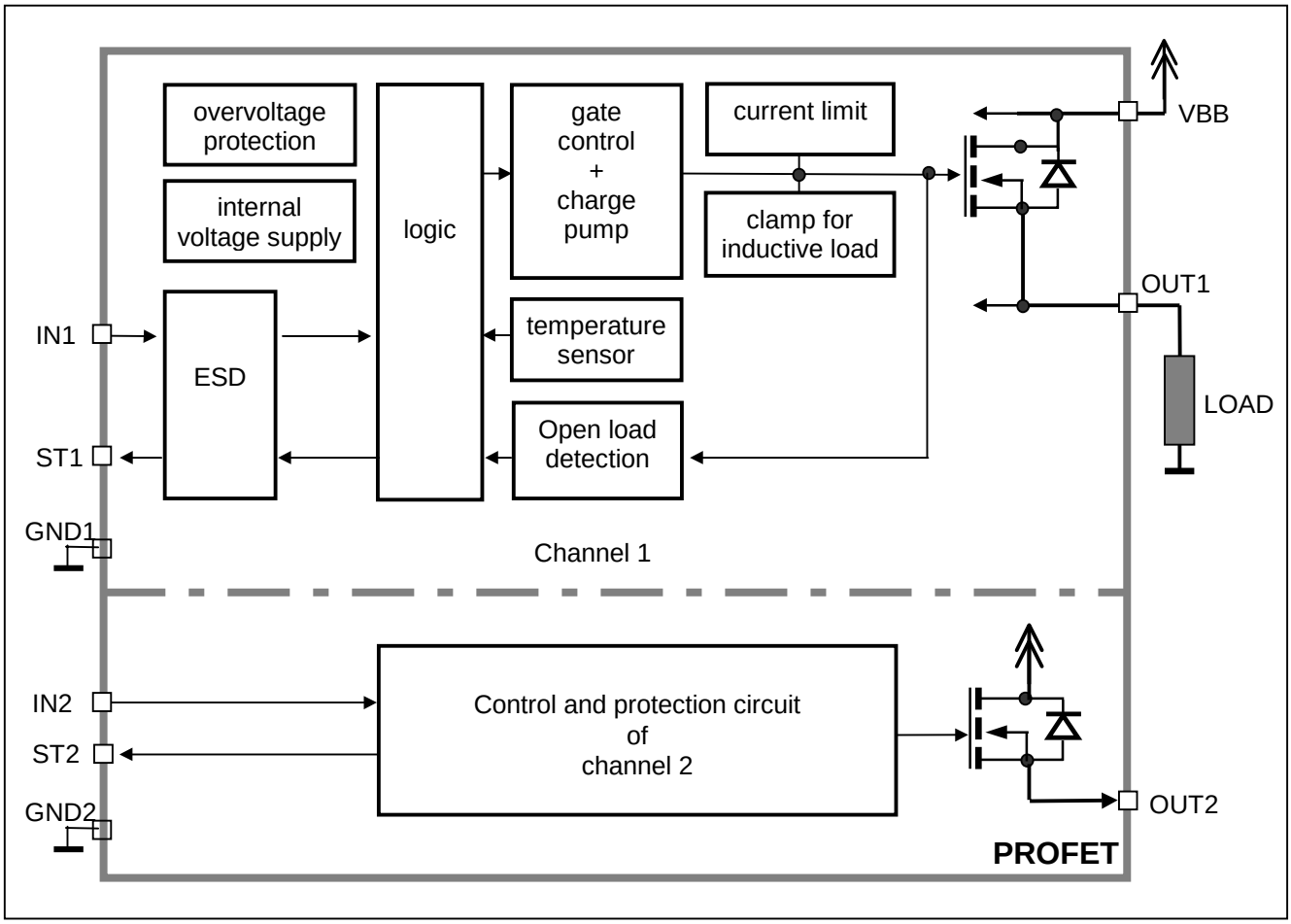
## Diagnostic Function

- Diagnostic feedback with open drain output
- Open load detection in ON-state
- Feedback of thermal shutdown in ON-state

## Block Diagram



## Functional diagram

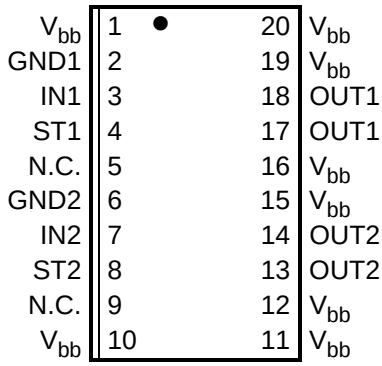



## Pin Definitions and Functions

| Pin | Symbol | Function |
|---|---|---|
| 1,10, 11,12, 15,16, 19,20 | $V_{bb}$ | **Positive power supply voltage**. Design the wiring for the simultaneous max. short circuit currents from channel 1 to 2 and also for low thermal resistance |
| 3 | IN1 | **Input 1,2**, activates channel 1,2 in case of logic high signal |
| 7 | IN2 | |
| 17,18 | OUT1 | **Output 1,2**, protected high-side power output of channel 1,2. Design the wiring for the max. short circuit current |
| 13,14 | OUT2 | |
| 4 | ST1 | **Diagnostic feedback 1,2** of channel 1,2, open drain, low on failure |
| 8 | ST2 | |
| 2 | GND1 | **Ground 1** of chip 1 (channel 1) |
| 6 | GND2 | **Ground 2** of chip 2 (channel 2) |
| 5,9 | N.C. | **Not Connected** |

## Pin configuration

(top view)



## Maximum Ratings at $T_j$ = 25°C unless otherwise specified

| Parameter | Symbol | Values | Unit |
|---|---|---|---|
| Supply voltage (overvoltage protection see page 4) | $V_{bb}$ | 43 | V |
| Supply voltage for full short circuit protection<br>$T_{j,start}$ = -40 ...+150°C | $V_{bb}$ | 24 | V |
| Load current (Short-circuit current, see page 5) | $I_L$ | self-limited | A |
| Load dump protection[1] $V_{LoadDump} = V_A + V_s$, $V_A$ = 13.5 V<br>$R_I$[2] = 2 Ω, $t_d$ = 200 ms; IN = low or high,<br>each channel loaded with $R_L$ = 9.0 Ω, | $V_{Load\,dump}$[3] | 60 | V |
| Operating temperature range | $T_j$ | -40 ...+150 | °C |
| Storage temperature range | $T_{stg}$ | -55 ...+150 | |
| Power dissipation (DC)[4] $T_a$ = 25°C: | $P_{tot}$ | 3.8 | W |
| (all channels active) $T_a$ = 85°C: | | 2.0 | |
| Maximal switchable inductance, single pulse<br>$V_{bb}$ = 12V, $T_{j,start}$ = 150°C[4],<br>$I_L$ = 4.0 A, $E_{AS}$ = 296 mJ, 0 Ω one channel: | $Z_L$ | 19.0 | mH |
| $I_L$ = 6.0 A, $E_{AS}$ = 631 mJ, 0 Ω two parallel channels: | | 17.5 | |
| see diagrams on page 9 | | | |
| Electrostatic discharge capability (ESD) IN: | $V_{ESD}$ | 1.0 | kV |
| (Human Body Model) ST: | | 4.0 | |
| out to all other pins shorted: | | 8.0 | |
| acc. MIL-STD883D, method 3015.7 and ESD assn. std. S5.1-1993<br>R=1.5kΩ; C=100pF | | | |
| Input voltage (DC) | $V_{IN}$ | -10 ... +16 | V |
| Current through input pin (DC) | $I_{IN}$ | ±2.0 | mA |
| Current through status pin (DC) | $I_{ST}$ | ±5.0 | |
| see internal circuit diagram page 8 | | | |

## Thermal Characteristics

| Parameter and Conditions | Symbol | Values | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | Max | |
| Thermal resistance | | | | | |
| junction - soldering point[4],[5] each channel: | $R_{thjs}$ | -- | -- | 12 | K/W |
| junction - ambient[4] one channel active: | $R_{thja}$ | -- | 40 | -- | |
| all channels active: | | -- | 33 | -- | |

1) Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GND and status pins (a 150Ω resistor for the GND connection is recommended.

2) $R_I$ = internal resistance of the load dump test pulse generator

3) $V_{Load\,dump}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

4) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for $V_{bb}$ connection. PCB is vertical without blown air. See page 14

5) Soldering point: upper side of solder edge of device pin 15. See page 14

## Electrical Characteristics

| **Parameter and Conditions,** each of the two channels at $T_j$ = -40...+150°C, $V_{bb}$ = 12 V unless otherwise specified | **Symbol** | **Values** | | | **Unit** |
|---|---|---|---|---|---|
| | | min | typ | Max | |
| **Load Switching Capabilities and Characteristics** | | | | | |
| On-state resistance ($V_{bb}$ to OUT); $I_L$ = 2 A, $V_{bb} \geq$ 7V<br>each channel, $T_j$ = 25°C:<br>$T_j$ = 150°C:<br>two parallel channels, $T_j$ = 25°C:<br>see diagram, page 10 | $R_{ON}$ | -- | 36<br>67<br>18 | 40<br>75<br>20 | mΩ |
| Nominal load current one channel active:<br>two parallel channels active:<br>Device on PCB[6], $T_a$ = 85°C, $T_j \leq$ 150°C | $I_{L(NOM)}$ | 4.4<br>6.7 | 4.8<br>7.3 | -- | A |
| Output current while GND disconnected or pulled up; Vbb = 30 V, $V_{IN}$ = 0,<br>see diagram page 8; (not tested specified by design) | $I_{L(GNDhigh)}$ | -- | -- | 2 | mA |
| Turn-on time[7] IN ⌐‾ to 90% $V_{OUT}$:<br>Turn-off time IN ‾⌐ to 10% $V_{OUT}$:<br>$R_L$ = 12 Ω | $t_{on}$<br>$t_{off}$ | 50<br>50 | 100<br>120 | 200<br>250 | µs |
| Slew rate on[7]<br>10 to 30% $V_{OUT}$, $R_L$ = 12 Ω $T_j$ = -40°C:<br>$T_j$ = 25°C...150°C: | $dV/dt_{on}$ | 0.15<br>0.15 | --<br>-- | 1<br>0.8 | V/µs |
| Slew rate off[7]<br>70 to 40% $V_{OUT}$, $R_L$ = 12 Ω $T_j$ = -40°C:<br>$T_j$ = 25°C...150°C: | $-dV/dt_{off}$ | 0.15<br>0.15 | --<br>-- | 1<br>0.8 | V/µs |
| **Operating Parameters** | | | | | |
| Operating voltage Tj=-40<br>$T_j$=25...150°C: | $V_{bb(on)}$ | 4.75 | --<br>-- | 41<br>43 | V |
| Overvoltage protection[8] $T_j$ =-40°C:<br>$I_{bb}$ = 40 mA $T_j$ =25...150°C: | $V_{bb(AZ)}$ | 41<br>43 | --<br>47 | --<br>52 | V |
| Standby current[9] $T_j$ =-40°C...25°C:<br>$V_{IN}$ = 0; see diagram page 10 $T_j$ =150°C: | $I_{bb(off)}$ | --<br>-- | 10<br>-- | 16<br>50 | µA |
| Leakage output current (included in $I_{bb(off)}$)<br>$V_{IN}$ = 0 | $I_{L(off)}$ | -- | 1 | 10 | µA |
| Operating current [10], $V_{IN}$ = 5V,<br>$I_{GND}$ = $I_{GND1}$ + $I_{GND2}$, one channel on:<br>two channels on: | $I_{GND}$ | --<br>-- | 0.8<br>1.6 | 1.4<br>2.8 | mA |

6) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for $V_{bb}$ connection. PCB is vertical without blown air. See page 14

7) See timing diagram on page 11.

8) Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GND and status pins (a 150Ω resistor for the GND connection is recommended). See also $V_{ON(CL)}$ in table of protection functions and circuit diagram on page 8.

9) Measured with load; for the whole device; all channels off

10) Add $I_{ST}$, if $I_{ST}$ > 0

| **Parameter and Conditions,** each of the two channels at $T_j$ = -40...+150°C, $V_{bb}$ = 12 V unless otherwise specified | **Symbol** | **Values** | | | **Unit** |
|---|---|---|---|---|---|
| | | min | typ | Max | |
| **Protection Functions** | | | | | |
| Current limit, (see timing diagrams, page 12) | | | | | |
| $T_j$ =-40°C: | $I_{L(lim)}$ | 40 | 49 | 60 | A |
| $T_j$ =25°C: | | 33 | 41 | 48 | |
| $T_j$ =+150°C: | | 23 | 29 | 35 | |
| Repetitive short circuit current limit, | | | | | |
| $T_j = T_{jt}$ each channel | $I_{L(SCr)}$ | -- | 30 | -- | A |
| two parallel channels | | -- | 30 | -- | |
| (see timing diagrams, page 12) | | | | | |
| Initial short circuit shutdown time $T_{j,start}$ =25°C: | $t_{off(SC)}$ | -- | 1.7 | -- | ms |
| (see timing diagrams on page 12) | | | | | |
| Output clamp (inductive load switch off)[11] | | | | | V |
| at $V_{ON(CL)} = V_{bb} - V_{OUT}$, $I_L$= 40 mA $T_j$ =-40°C: | $V_{ON(CL)}$ | 41 | -- | -- | |
| $T_j$ =25°C...150°C: | | 43 | 47 | 52 | |
| Thermal overload trip temperature | $T_{jt}$ | 150 | -- | -- | °C |
| Thermal hysteresis | $\Delta T_{jt}$ | -- | 10 | -- | K |
| **Reverse Battery** | | | | | |
| Reverse battery voltage [12] | $-V_{bb}$ | -- | -- | 32 | V |
| Drain-source diode voltage ($V_{out} > V_{bb}$) $I_L$ = - 4.0 A, $T_j$ = +150°C | $-V_{ON}$ | -- | 600 | -- | mV |

11) If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest $V_{ON(CL)}$

12) Requires a 150 Ω resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Power dissipation is higher compared to normal operating conditions due to the voltage drop across the drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 3 and circuit page 8).

| **Parameter and Conditions,** each of the two channels at $T_j$ = -40...+150°C, $V_{bb}$ = 12 V unless otherwise specified | **Symbol** | **Values** | | | **Unit** |
|---|---|---|---|---|---|
| | | min | typ | Max | |
| **Diagnostic Characteristics** | | | | | |
| Open load detection current, (on-condition) each channel | $I_{L\ (OL)}$ | 100 | -- | 900 | mA |
| **Input and Status Feedback**[13)] | | | | | |
| Input resistance (see circuit page 8) | $R_I$ | 2.5 | 3.5 | 6 | kΩ |
| Input turn-on threshold voltage | $V_{IN(T+)}$ | 1.7 | -- | 3.2 | V |
| Input turn-off threshold voltage | $V_{IN(T-)}$ | 1.5 | -- | -- | V |
| Input threshold hysteresis | $\Delta\ V_{IN(T)}$ | -- | 0.5 | -- | V |
| Off state input current $V_{IN}$ = 0.4 V: | $I_{IN(off)}$ | 1 | -- | 50 | µA |
| On state input current $V_{IN}$ = 5 V: | $I_{IN(on)}$ | 20 | 50 | 90 | µA |
| Delay time for status with open load after switch off; (see diagram on page 13) | $t_{d(ST\ OL4)}$ | 100 | 520 | 900 | µs |
| Status invalid after positive input slope (open load) | $t_{d(ST)}$ | -- | -- | 500 | µs |
| Status output (open drain) | | | | | |
| Zener limit voltage $I_{ST}$ = +1.6 mA: | $V_{ST(high)}$ | 5.4 | 6.1 | -- | V |
| ST low voltage $I_{ST}$ = +1.6 mA: | $V_{ST(low)}$ | -- | -- | 0.4 | |

13) If ground resistors $R_{GND}$ are used, add the voltage drop across these resistors.

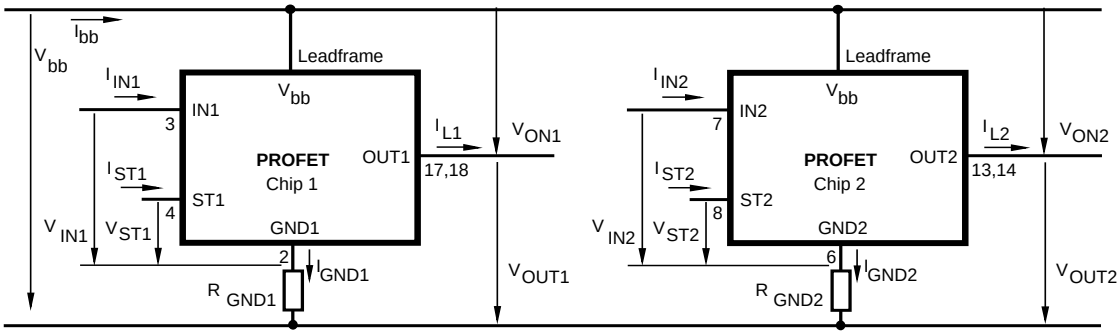
## Truth Table

| Channel 1 | Input 1 | Output 1 | Status 1 |
|---|---|---|---|
| Channel 2 | Input 2 | Output 2 | Status 2 |
| | level | level | BTS 736L2 |
| Normal operation | L<br>H | L<br>H | H<br>H |
| Open load | L<br>H | Z<br>H | H<br>L |
| Overtem-perature | L<br>H | L<br>L | H<br>L |

L = "Low" Level X = don't care Z = high impedance, potential depends on external circuit
H = "High" Level Status signal valid after the time delay shown in the timing diagrams

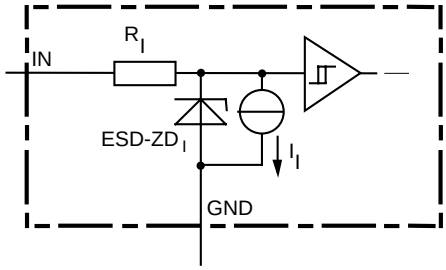
Parallel switching of channel 1 and 2 is easily possible by connecting the inputs and outputs in parallel. The status outputs ST1 and ST2 have to be configured as a 'Wired OR' function with a single pull-up resistor.

## Terms



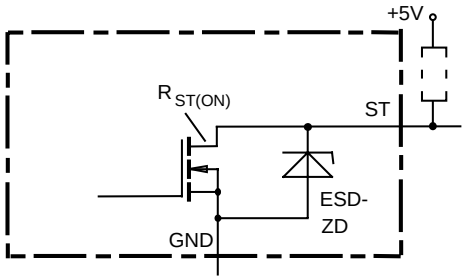

Leadframe ($V_{bb}$) is connected to pin 1,10,11,12,15,16,19,20
External $R_{GND}$ optional; two resistors $R_{GND1}$, $R_{GND2}$ = 150 Ω or a single resistor $R_{GND}$ = 75 Ω for reverse battery protection up to the max. operating voltage.

## Input circuit (ESD protection), IN1 or IN2



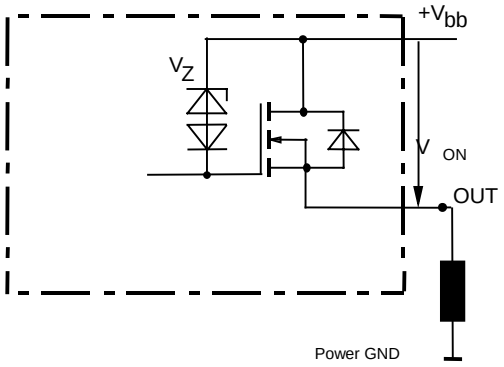

The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

## Status output, ST1 or ST2



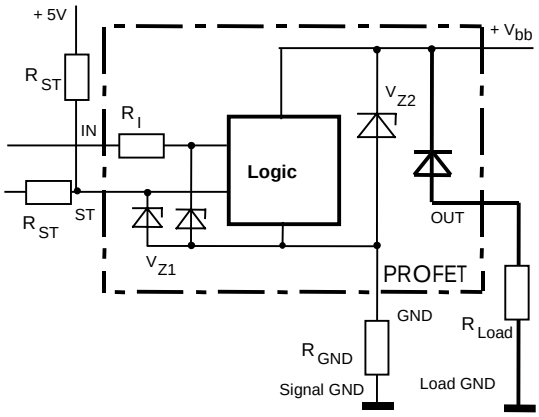

ESD-Zener diode: 6.1 V typ., max 5.0 mA; $R_{ST(ON)}$ < 375 Ω at 1.6 mA. The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

## Inductive and overvoltage output clamp, OUT1 or OUT2




$V_{ON}$ clamped to $V_{ON(CL)}$ = 47 V typ.

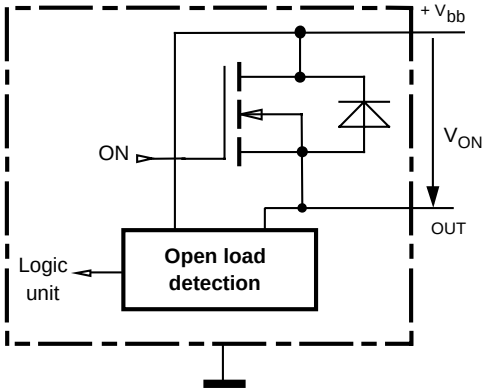
## Overvolt. and reverse batt. protection



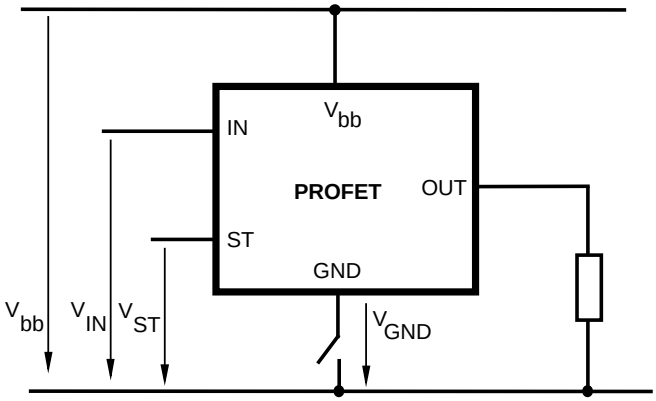

$V_{Z1}$ = 6.1 V typ., $V_{Z2}$ = 47 V typ., $R_{GND}$ = 150 Ω, $R_{ST}$= 15 kΩ, $R_I$= 3.5 kΩ typ.
In case of reverse battery the load current has to be limited by the load. Temperature protection is not active

## Open-load detection OUT1 or OUT2

ON-state diagnostic
Open load, if $V_{ON} < R_{ON} \cdot I_{L(OL)}$; IN high

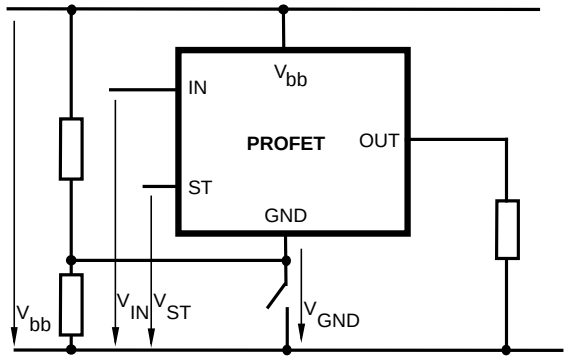



## GND disconnect



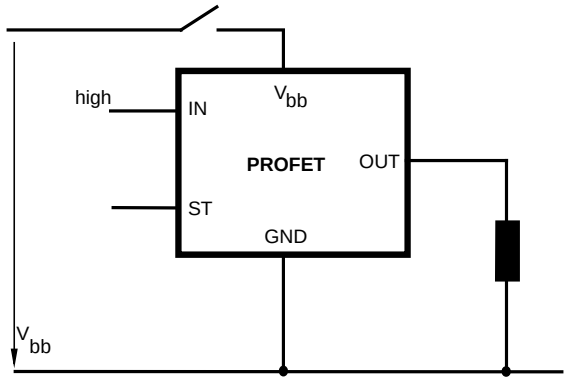

Any kind of load. In case of IN = high is $V_{OUT} \approx V_{IN} - V_{IN(T+)}$.
Due to $V_{GND} > 0$, no $V_{ST}$ = low signal available.

## GND disconnect with GND pull up




Any kind of load. If $V_{GND} > V_{IN} - V_{IN(T+)}$ device stays off
Due to $V_{GND} > 0$, no $V_{ST}$ = low signal available.

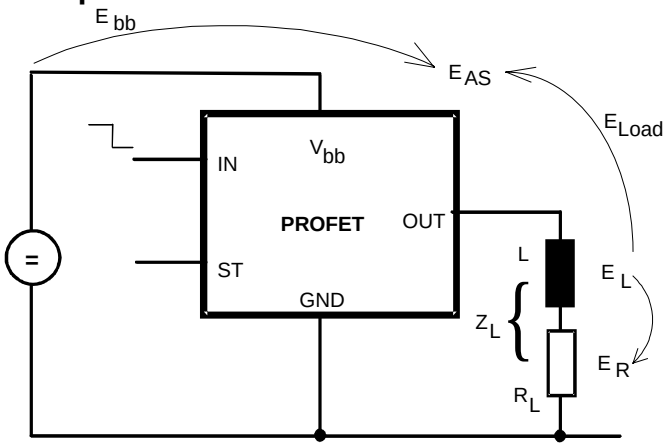
## $V_{bb}$ disconnect with energized inductive load




For inductive load currents up to the limits defined by $Z_L$ (max. ratings and diagram on page 9) each switch is protected against loss of $V_{bb}$.

Consider at your PCB layout that in the case of Vbb disconnection with energized inductive load all the load current flows through the GND connection.

## Inductive load switch-off energy dissipation




Energy stored in load inductance:

$$E_L = {}^1/_2 \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

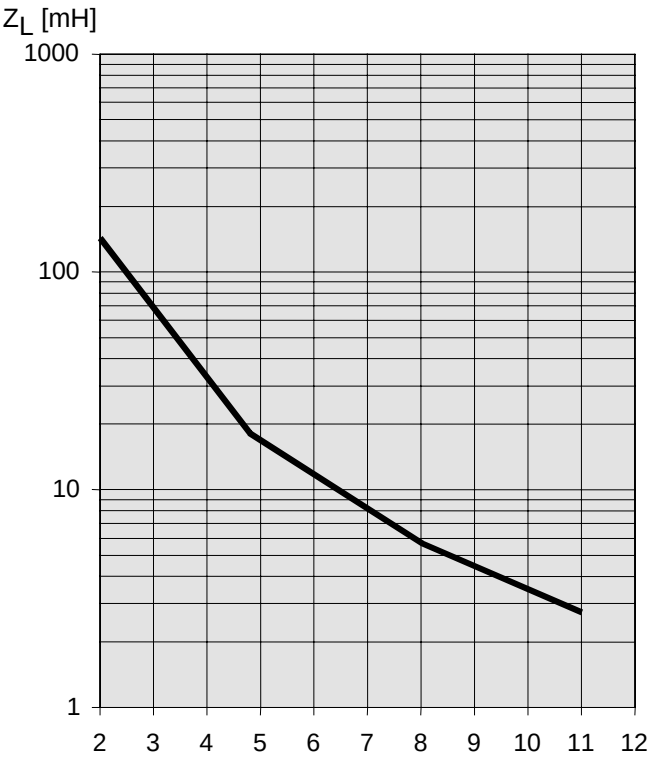
$$E_{AS} = E_{bb} + E_L - E_R = \int V_{ON(CL)} \cdot i_L(t)\, dt,$$

with an approximate solution for $R_L > 0\,\Omega$:

$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L}\left(V_{bb} + |V_{OUT(CL)}|\right)\ ln\ \left(1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|}\right)$$

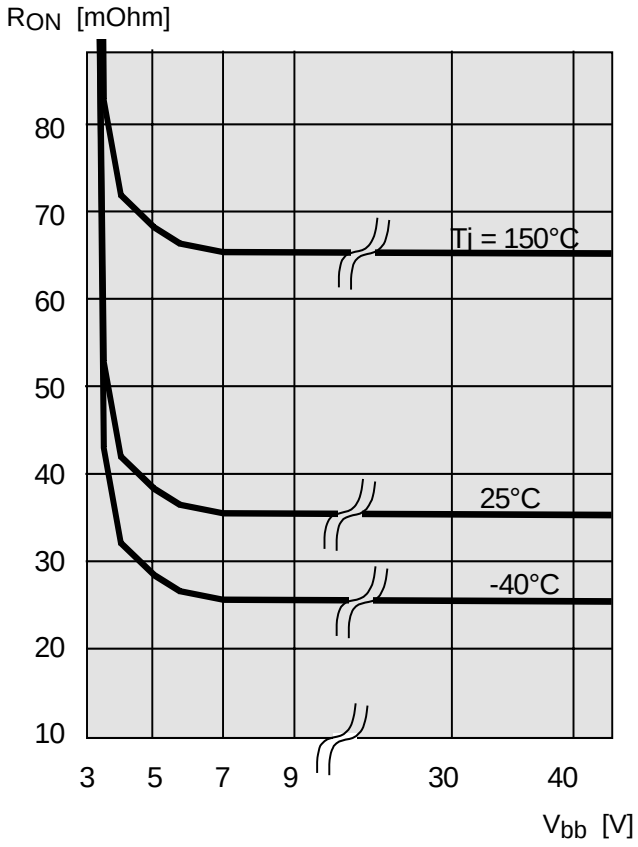
## Maximum allowable load inductance for a single switch off (one channel)[4)]

$L = f(I_L)$; $T_{j,start} = 150°C$, $V_{bb} = 12\,V$, $R_L = 0\,\Omega$



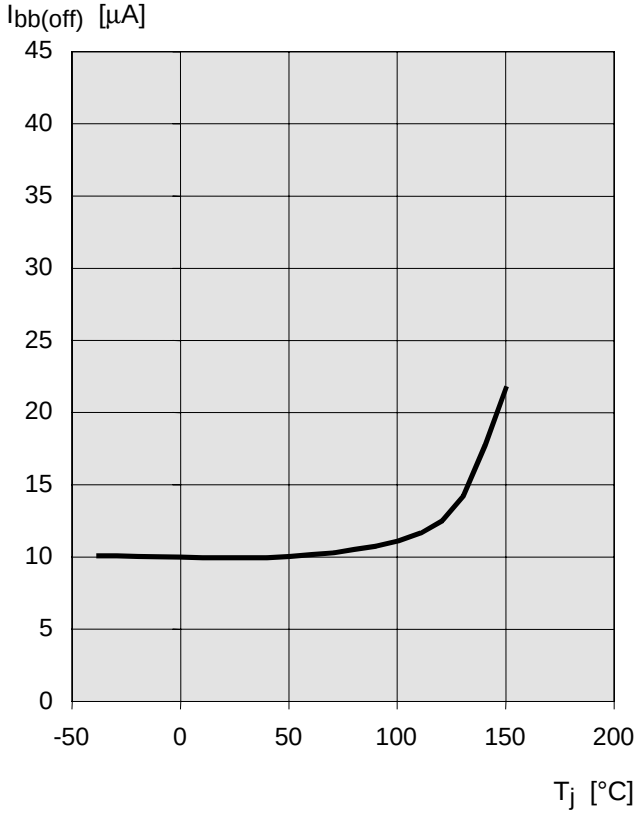
**Typ. on-state resistance**

$R_{ON} = f(V_{bb}, T_j)$; $I_L$ = 2 A, IN = high




**Typ. standby current**

$I_{bb(off)} = f(T_j)$; $V_{bb}$ = 9...34 V, IN1,2 = low



## Timing diagrams

Both channels are symmetric and consequently the diagrams are valid for channel 1 and channel 2

**Figure 1a:** $V_{bb}$ turn on:

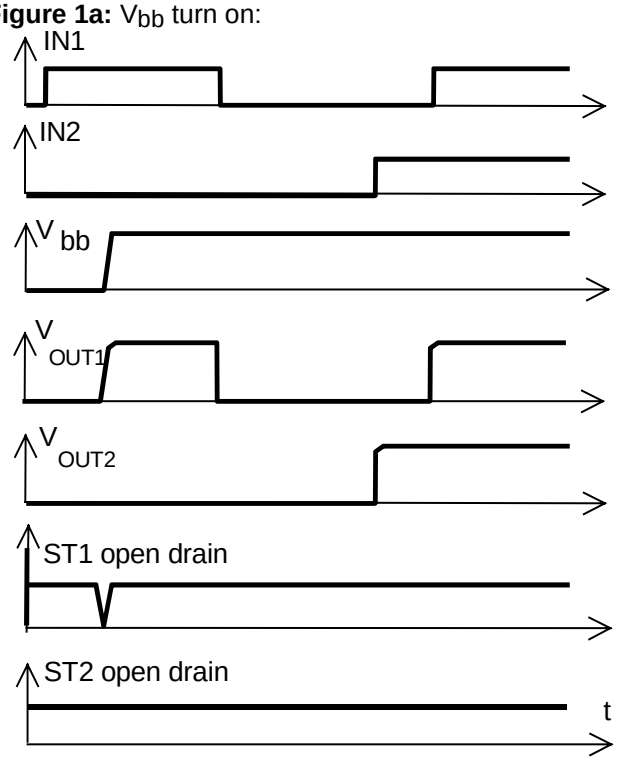



**Figure 2a:** Switching a resistive load, turn-on/off time and slew rate definition:

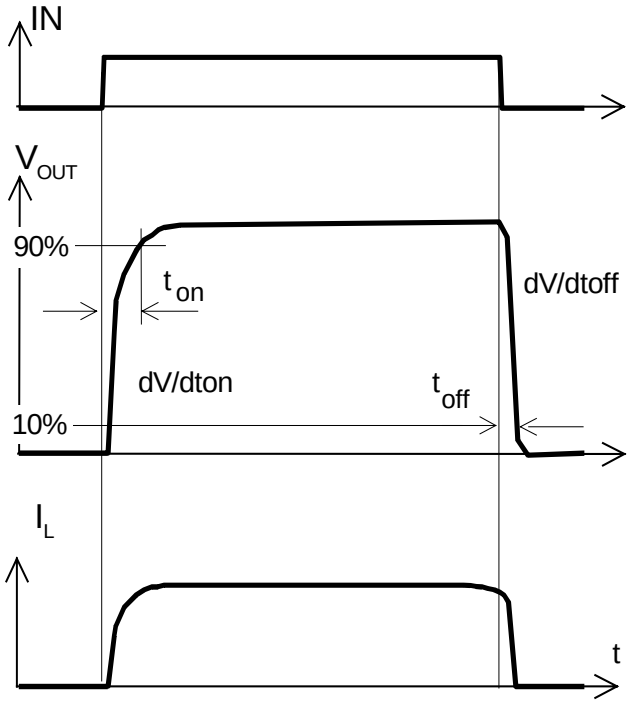
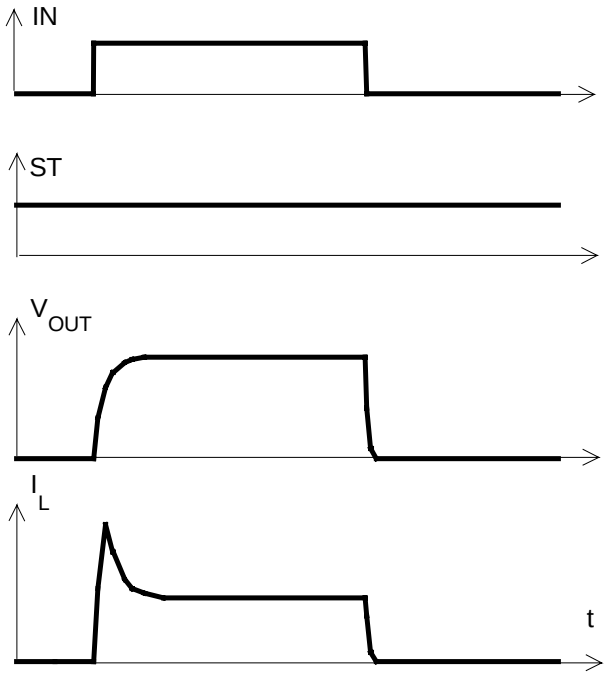
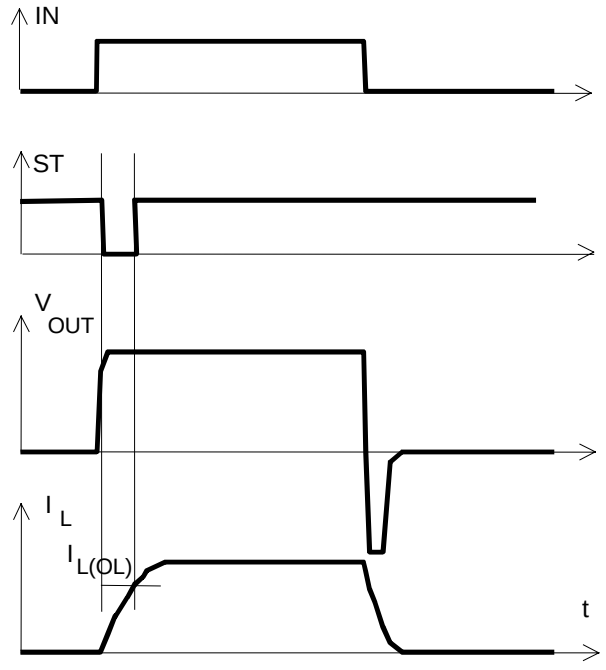



**Figure 2b:** Switching a lamp:



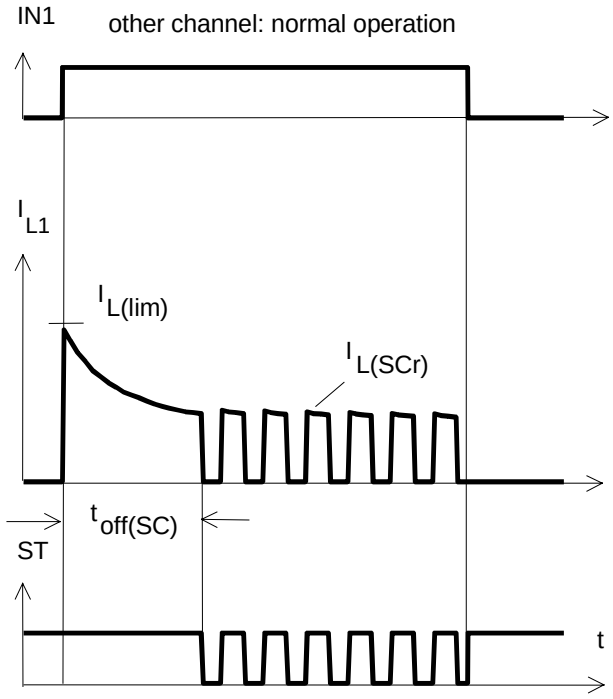

The initial peak current should be limited by the lamp and not by the current limit of the device.

**Figure 2c:** Switching an inductive load



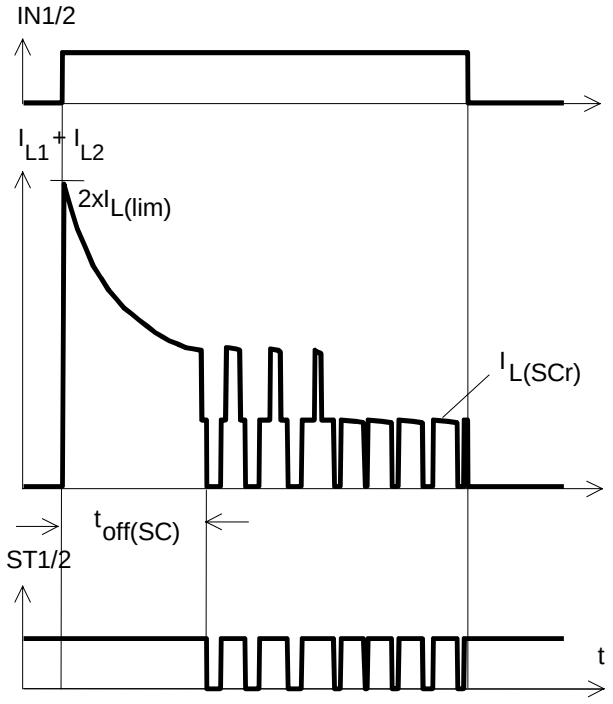

*) if the time constant of load is too large, open-load-status may occur

**Figure 3a:** Turn on into short circuit:
shut down by overtemperature, restart by cooling




Heating up of the chip may require several milliseconds, depending on external conditions

**Figure 3b:** Turn on into short circuit:
shut down by overtemperature, restart by cooling
(two parallel switched channels 1 and 2)




ST1 and ST2 have to be configured as a 'Wired OR' function ST1/2 with a single pull-up resistor.

**Figure 4a:** Overtemperature:
Reset if $T_j < T_{jt}$

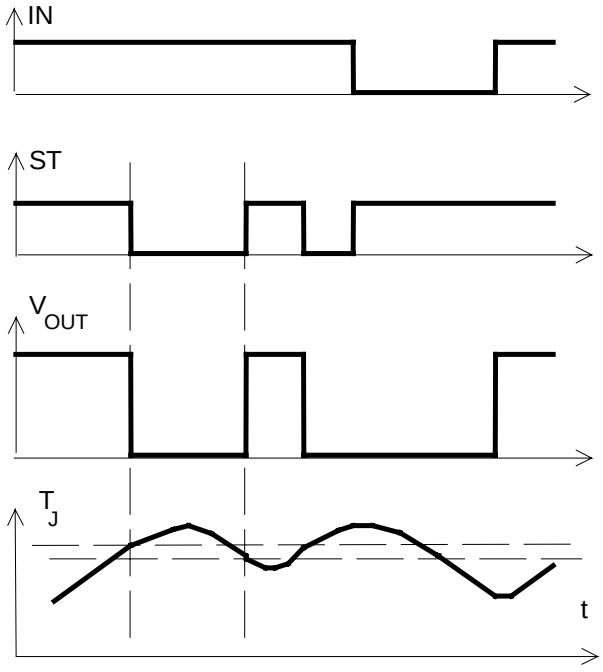
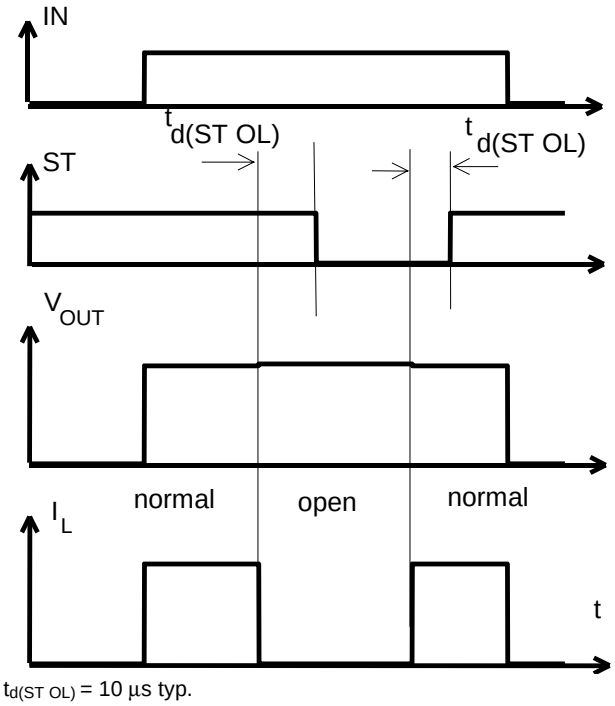
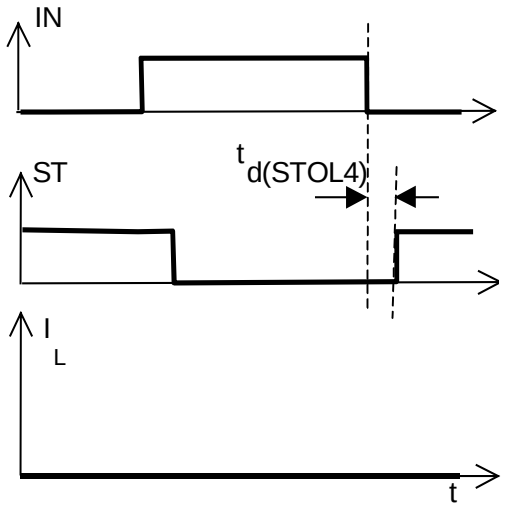



**Figure 5a:** Open load: detection in ON-state, open load occurs in on-state




$t_{d(ST\ OL)}$ = 10 µs typ.

**Figure 5b:** Open load: turn on/off to open load

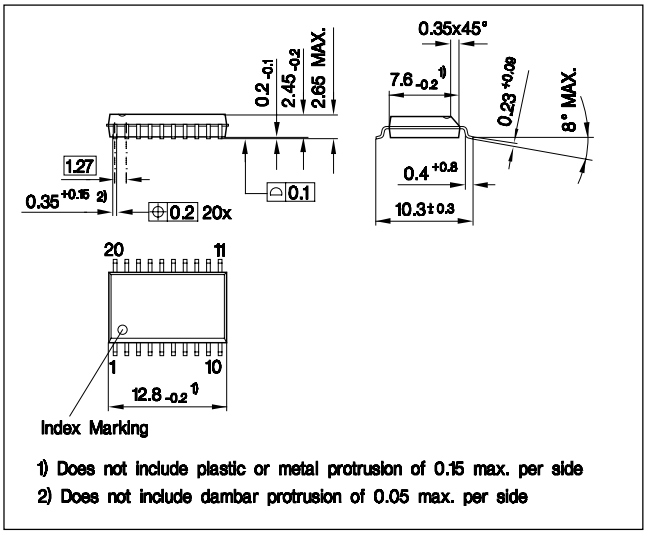


# Package and Ordering Code

## Standard: P-DSO-20-9

| Sales Code | BTS 736 L2 |
|---|---|
| Ordering Code | Q67060-S7011-A2 |

All dimensions in millimetres

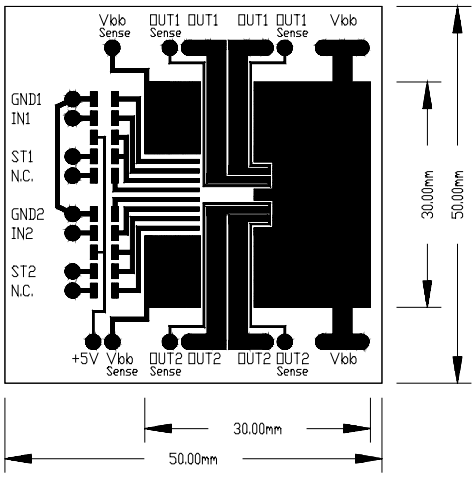



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

Definition of soldering point with temperature $T_S$: upper side of solder edge of device pin 15.


Pin 15

Printed circuit board (FR4, 1.5mm thick, one layer 70µm, 6cm² active heatsink area) as a reference for max. power dissipation $P_{tot}$, nominal load current $I_{L(NOM)}$ and thermal resistance $R_{thja}$

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